High Order Cascade Multibit ΣΔ Modulator for Wide Bandwidth Applications

S. Zouari, H. Daoud, M. Loulou, P. Loumeau, N. Masmoudi

Abstract—A wideband 2-1-1 cascaded ΣΔ modulator with a single-bit quantizer in the two first stages and a 4-bit quantizer in the final stage is developed. To reduce sensitivity of digital-to-analog converter (DAC) nonlinearities in the feedback of the last stage, dynamic element matching (DEM) is introduced. This paper presents two modelling approaches: The first is MATLAB description and the second is VHDL-AMS modelling of the proposed architecture and exposes some high-level-simulation results allowing a behavioural study. The detail of both ideal and non-ideal behaviour modelling are presented. Then, the study of the effect of building blocks nonidealities is presented; especially the influences of nonlinearity, finite operational amplifier gain, amplifier slew rate limitation and capacitor mismatch. A VHDL-AMS description presents a good solution to predict system's performances and can provide sensitivity curves giving the impact of nonidealities on the system performance.

Keywords—behavioural study, DAC nonlinearity, DEM, ΣΔ modulator, VHDL-AMS modelling.

I. INTRODUCTION

THE new wireless communications standards demand high performance analog to digital converters (ADCs) [1][2][3]. This paper presents a fourth-order 2-1-1 cascade sigma delta modulator, employing 4-b quantizer in last stage, which can be used as an ADC to receive base band I and Q channels, targeting the WCDMA standard. The main goal was to develop a high resolution high speed ADC which can relaxes the specifications of the preceding analog filters reducing the overall cost of the analog front end. The target performance of an ADC aimed at such application is 90-dB signal-to-noise ratio (SNR) with a bandwidth over 2 MHz.

In this paper we show how a high level language can be used to model a system including digital and analogue domains. Each domain must be described at the appropriate level of abstraction taking into account the desired level of results. We show in this paper how this approach can be applied to the proposed ΣΔ modulator in order to analyse the impact of nonidealities on the system performances according to the characterisation of each building block.

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II. ARCHITECTURE SELECTION

Given the high input bandwidths in WCDMA standard, only low-oversampling ratio (OSR) sigma delta modulators are feasible. To achieve high SNR with these low values of OSR, the known formula for the dynamic range given by (1) impose to increase the sigma-delta modulator order (L) or the resolution of the quantizer (B), or both simultaneously.

$$DR_{dB} = 10 \log \left[\frac{3}{2} \left(2^B - 1 \right)^2 \frac{(2L+1)OSR^{2L+1}}{\Pi^{2L}} \right] \quad (1)$$

Cascaded sigma delta modulator structures with multibit quantization are the most suitable architectures for high speed high resolution ADCs with low oversampling ratio [1][2][4][5][6]. They perform high order noise shaping by cascading sigma-delta stages of second order or lower to avoid instability [1]. In a cascaded structure, each stage converts the quantization error of the previous stage. A digital filter then uses the output of each loop to construct a signal that has noise shaping on the order of the overall modulator [7]. As a result, the quantization errors of all stages except the last one can be cancelled. The only quantization error that remains visible at the output is the quantization noise of the last stage, which is shaped by the total number of integrators in the cascaded sigma delta modulator. Several sigma delta modulators have been successfully built using cascaded topologies with multibit quantization in one or more loops [1] [6-11].

Our proposed Sigma Delta Modulator is a 2-1-1 cascaded architecture with low OSR of 16. The fourth-order modulator oversampling at 16 is implemented using a cascade of second-order sigma–delta loop and two first-order loops. The cascade architecture recombines the outputs of each stage in the digital domain to achieve fourth-order noise shaping. Inherently linear single-bit D/A converters are employed in the first two stages while a four-level D/A converter is employed in the lower resolution third stage to improve dynamic range. The proposed topology overcomes the influence of mismatch-induced errors in the multibit DAC on the 2-1-1 modulator performance of [11] by introducing a DEM algorithm; data weighted averaging (DWA) to correct DAC mismatch nonlinearity.

The new architecture is shown below in Figure 1. Based on [11], the coefficients were optimised in such a manner that analog coefficients could be constructed with small integer

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ratios in order to achieve a compact layout and good matching in the switched-capacitor (SC) implementation. The value of the integrator weights are given by Table 1.

This selection of coefficients nicely bounds the integrator outputs ± 1 for a reasonable input range and offer a stable converter with a high resolution of 90dB for an oversampling ratio of 16.

TABLE I
COEFFICIENT VALUES

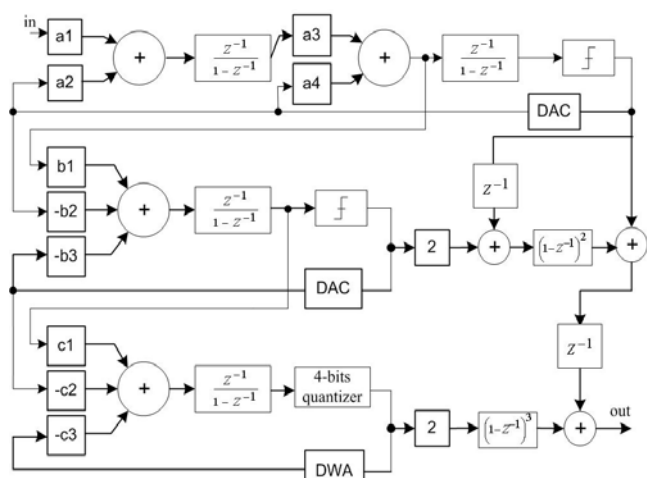| a1	0.25	b2	0.5
a2	0.25	b3	0.5
a3	1	c1	2
a4	0.5	c2	1
b1	1	c3	1

Fig. 1 Fourth order 2-1-1 cascade modulator with
4-bits quantization and DWA in the last stage.

III. DAC LINEARISATION

As mentioned above, at low OSR, the use of multibit quantizer in cascaded modulator is an attractive way to reach a high-band-width, high resolution converter. However, the performance of such sigma-delta modulator is limited by the internal DAC nonlinearity. In our work, the 4-bit DAC inside a sigma delta modulator is composed of 15 unit elements. Each of these elements can be used to generate a positive or negative feedback signal. The contributions of all the elements are summed to construct the feedback signal for the sigma delta converter. Due to process variations, the values of these unit elements will not be equal to the ideal value and the DAC will introduce errors. As illustrated in Figure. 2, in practical switched-capacitor implementation, the four-bit DAC in the feedback of the last stage of our 2-1-1 modulator can be built with 15 capacitors to determine the analog feedback signal. Due to process tolerances and variations, the values of these unit elements will deviate from the ideal weight Cu, resulting in errors in the DAC. The matching error can be considered to have a Gaussian distribution [12].

Several DEM techniques have been developed to address the linearity of the feedback DAC in a multibit sigma-delta modulator and obtain a shaping in frequency of the mismatch noise [13], but usually the simplest techniques can generate idle tones in the signal bandwidth, while the ones that present tones immunity are generally quite complex with costs in term of silicon area and power consumption. A good compromise can be achieved by the Data Weighted Averaging DWA
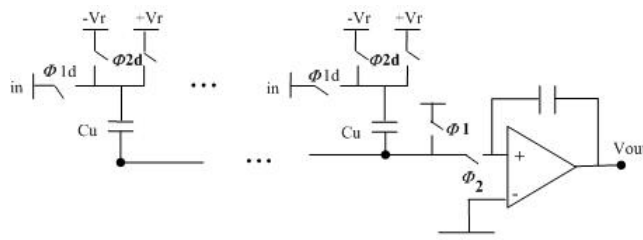

Fig. 2 DAC switched-capacitor implementation

algorithm [14]. This algorithm uses all the DAC elements at the maximum possible rate while ensuring that each element is used the same number of times. This is done by sequentially selecting elements an array, beginning with the next available unused element. Using elements at the maximum possible rate ensures that the DAC errors will quickly sum to zero, moving distortion to high frequencies.

IV. SIMULINK MODEL

In the first time, a low level SIMULINK model of the switched capacitor ADC is proposed in order to characterize the sigma-delta modulator. Simulation results show the efficiency of the employed algorithm to cancel the whole DAC non-linearities. The architecture permits to reach the target SNR of 90 dB at a 16 OSR suitable for WCDMA application.

Figure 3 and Figure 4 show respectively the block diagram of MATLAB SIMULINK model of an ideal 4-bit DAC and that of a non ideal 4-bit DAC linearized by DWA algorithm. In these models, the DAC unit elements are built in such a way to be near to these physically achieved in switched-capacitor implementation. The DWA is fully implemented in a digital domain, when a DAC input sequence is received from the 4-bits quantizer, an adding block is used to generate tow pointers which indicate the first element and the last element used in a conversion cycle. After the adding function, decoding functions are activated to produce DWA control signals [15].

In our case, the values of the unit elements are given by (2).

$$C_i = C + e_i \qquad (2)$$

Where C is the ideal value of the unit element and e_i is a deviation of each element given by Gaussian distribution.

In our work, the DAC unit elements are built by 15 SIMULINK subsystems. Each of them is composed of an element gain connecting to either $+Vr$ or $-Vr$. So, for each DAC input code, the elements selected by the DWA contribute positively and are summed, while the contributions

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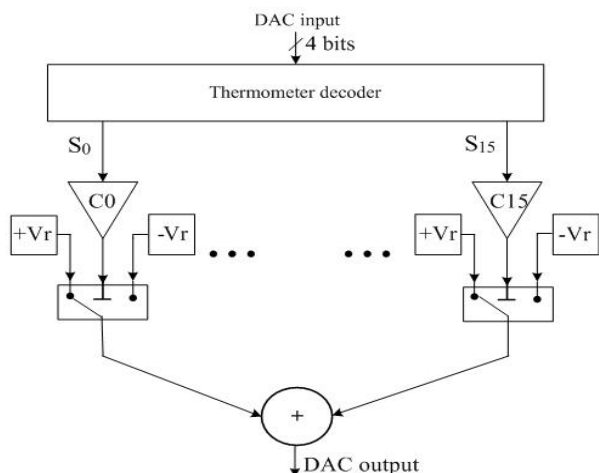from the other elements are subtracted to generate the output of the DAC.

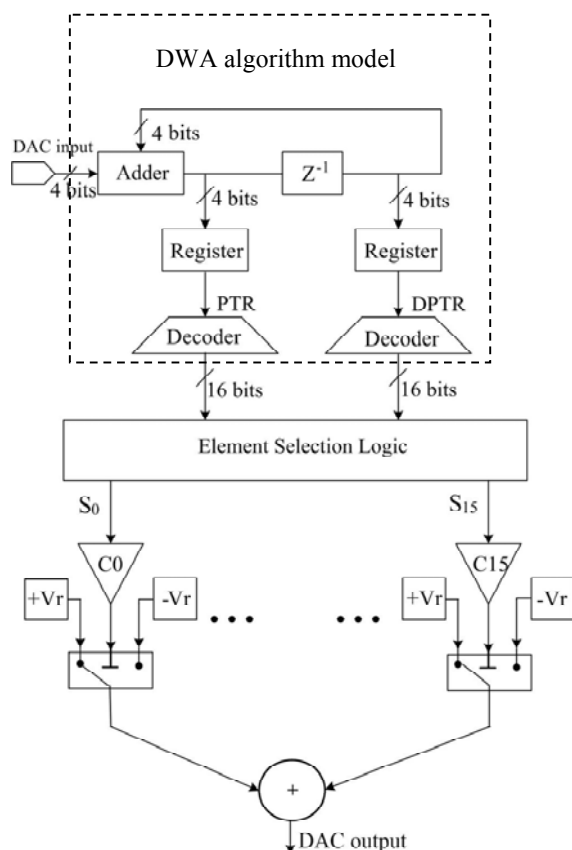Fig. 3 SIMULINK model of 4-bit DAC with unit elements.

Fig. 4 SIMULINK model of a non ideal 4-bits DAC with DWA implementation unit elements.

The evaluation of the performance of the proposed modulator has been done with MATLAB SIMULINK software. To show the advantage of the use of DWA if compared to the solution without this algorithm, three 4-bits DAC are implemented. The first is an ideal DAC using a thermometer decoder and 15 unit elements. In the second, the non ideal 4-bits DAC, the values of these unit elements are deviated from the ideal weight. The third is a non ideal 4-bit DAC with dynamic element matching (Figure 4).

In the first time, we have simulated the SNR as a function of the relative input magnitude of the 2-1-1 modulator using ideal 4-bits DAC in the feedback of the final stage. It was found, as shown in Figure 5, that the proposed modulator achieves the target SNR of 90dB.

This performance is limited by the non-ideality of the DAC. In deed the use of non ideal 4-bit DAC in the same architecture shows clearly that mismatch of the unit elements of the DAC can completely degrade the SNR when the DWA is not introduced. Figure 6 shows the SNR versus input level of the 2-1-1 modulator using 4-bits quantizer and non-ideal DAC in the last stage for tow cases: with and without introducing DWA algorithm. This figure illustrates the large sensitivity of this architecture to the error of the DAC in the feedback. Note that in the case of without DWA, an important degradation of the SNR is produced in the presence of DAC non-linearity. For an integral non-linearity (INL) equal to 1% full scale (FS) [equivalent to 0.15 last significant bit (LSB) of four bits], the SNR is 17dB lower than the ideal case, and for a 0.5% FS of INL [equivalent to 0.075 LSB], the SNR is degraded by 10dB.
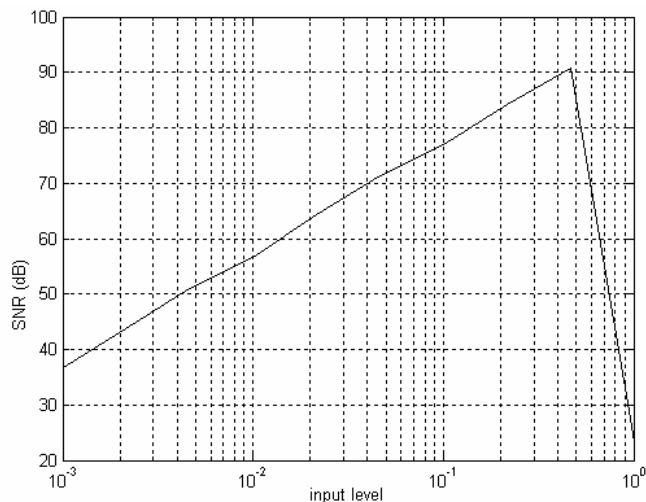

Fig. 5 Simulation of 2-1-1 modulator with 4-bits quantizer and an ideal 4-bit DAC in the final stage.

Using DWA algorithm in the feedback loop of the modulator suppresses the errors of the DAC (Figure 6). The algorithm allows us to reach the target 90dB SNR with INL equal to 0.5% FS, and 89dB for INL equal to 1%FS. Also in this case it is observed that a higher DAC error is tolerable, which renders the performance of the proposed architecture superior to those of previous cascade modulators with multibit quantizer in the last stage.

Except for the DAC-induced errors, the architecture study based on Simulink model assumes ideal conditions.

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Nevertheless, circuit imperfections degrading the ΣΔ modulator performances must be taken into account in practice. Then, the behavioral approach has been used to investigate the overall circuit non-idealities effects, to optimize the system parameters and establish the specifications of the analog blocks. A description level using VHDL-AMS and Simplorer schematic facilities has been performed.
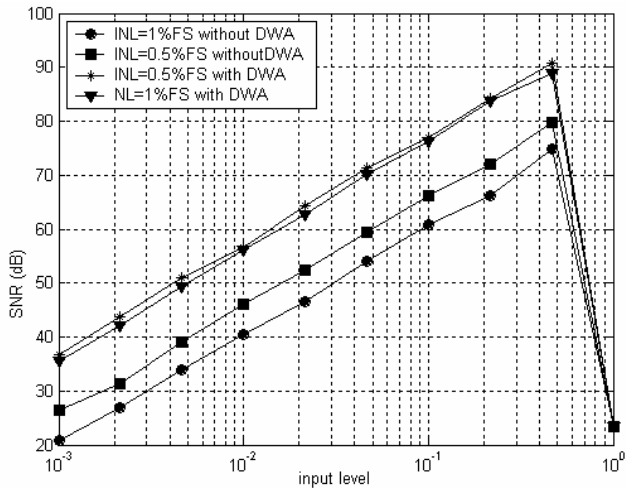

Fig. 6 The SNR as function of the input power of a
2-1-1 modulator using a non-ideal DAC with and without DWA

V. VHDL-AMS MODEL

Each block of the ΣΔ modulator has been modeled using VHDL-AMS descriptions or Simplorer schematic models allowing parameter setting according to the non-idealities. The obtained blocks were connected in Simplorer Software environment to obtain a behavioral description of the 2-1-1 multibit architecture.

A. Switched capacitor integrator model

The switched capacitor integrator model is developed using schematic level description as show in figure 7. Several nonidealities of the integrator have been included in the behavioural model: finite OTA DC gain, slew rate and gain bandwidth limitations, capacitor mismatch, OTA noise and thermal noise. Using the behavioural simulations we have estimated the OTA requirements for a specified dynamic range. Simulation results show that the proposed modulator can tolerate an OTA dc gain of 70 dB, the OTA bandwidth needs to be at least 200MHz and the slew rate at least 150V/μs. Switches thermal noise and the OTAs noise are the main noise sources affecting the modulator performance. These effects have been considered in the simulation by using a noisy integrator model as shown in figure 7.

The specifications determined previously have been used to select an appropriate circuit topology for the OTAs. The goal is to select a topology, which can meet the integrator performance requirements at minimum power dissipation. The fully differential folded cascade OTA has been chosen. Fig.8

shows the schematic of the fully differential folded cascade OTA. This allows us to reach best high operating speed over power consumption ratio. The OTA parameters are set referring to a design sample developed in our laboratory [16]. It is sized using gm/Id method allowing to reach high Gain Bandwidth product operating at a power supply voltage set to ± 2Vand designed using AMS CMOS 0.35μm.. The simulated parameters of the front-end OTA are summarized in table 2 and reported on Simplorer OTA model.

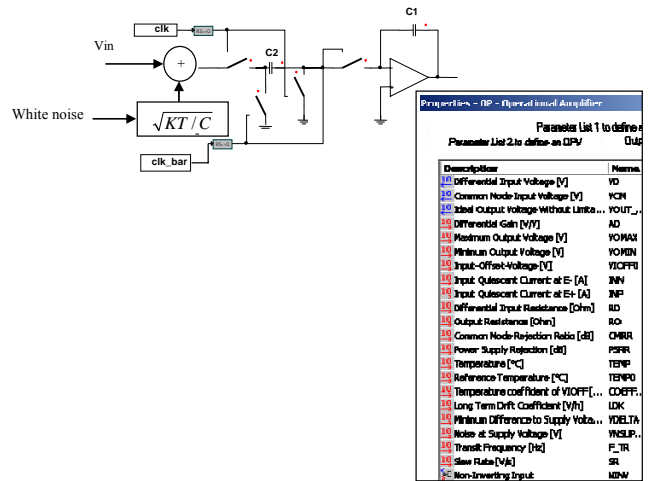The switch is mainly modeled by its ON/OFF resistances.

Fig. 7 SC Integrator model

This is suppose a charge injection cancellation using CMOS transmission gate with dummy transistors. However deviation from ideal values are introduced to take into account mismatch errors between switched and feedback capacitors.

The thermal noise introduced by switches can be modeled, as described in [17], as an additive white noise source of variance KT/C to the input signal as shown in figure 8.

B. Multibit quantizer model

The 4-bit quantizer is implemented by differential flash ADC with 16 parallel comparators and a resistor divider to generate the reference voltage of the comparators. Figure 8 shows the schematic model of the 4-bit quantizer circuit. It should be noted that the cascade structure modulator performance is very tolerant to flash converter nonlinearity, such as comparator offset and hysterisis. In a single-loop sigma delta modulator, the effect of nonlinearity is only suppressed by the amount of noise shaping provided by the loop, and may exhibit undesirable tones, which degrade SFDR [18]. In case of 2-1-1 cascade, the first stage quantizer nonlinearity only appears at the modulator output as a second-order noise-shaped leakage, which is completely negligible [1].
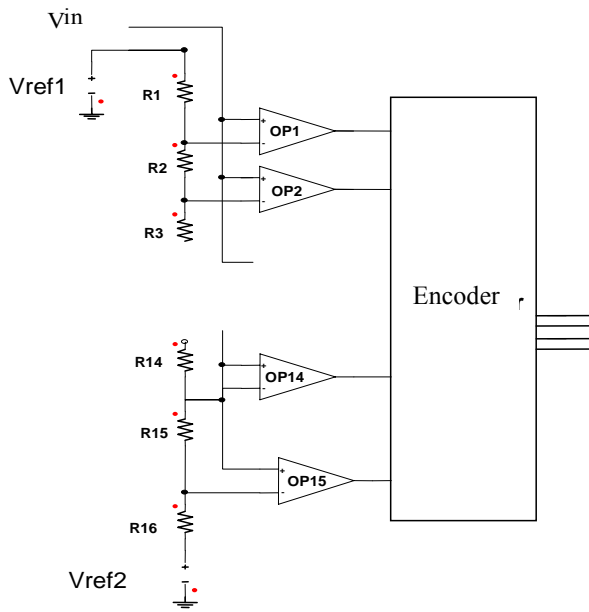
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Fig. 8 Four bit quantizer model

C. Multibit DAC model

The multibit D/A converter from the feedback path is implemented as a thermometer coded unit-elements converter. Figure 9 shows the schematic model of the 4-bit DAC.
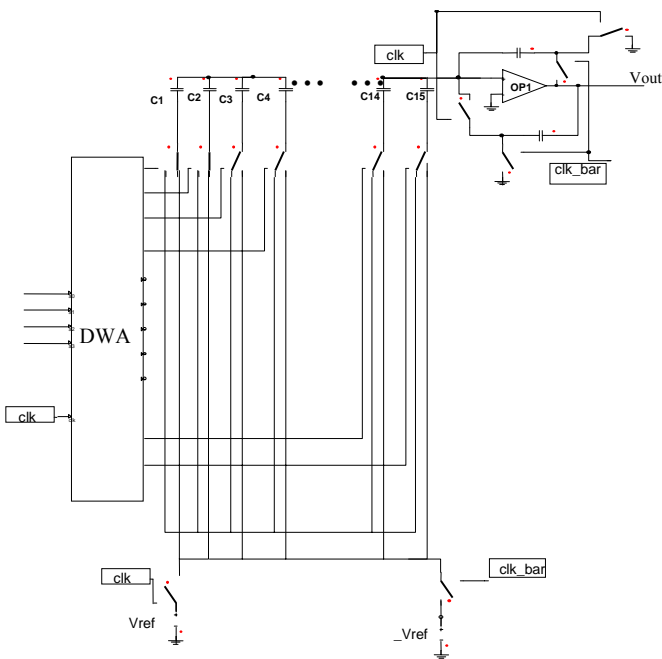

Fig. 9 Four- bit DAC model (with DWA)

VI. VHDL-AMS SIMULATION RESULTS

The proposed topology, shown in Figure 1, was simulated and performances were evaluated using VHDL-AMS language. The behavioural models for several nonidealities, such as OTA parameters (finite DC gain, nonlinear DC transfer characteristic, finite bandwidth and slew rate), D/A converter mismatches, were used to determine the specifications limits for the sigma-delta building blocks.

A. Ideal case

A first validation of the developed model has been done with ideal case, which means a cancelling of blocks nonidealities by using default model's parameter. We have simulated the SNR as a function of the input amplitude of the ideal case. It was found that similar results are obtained with both MATLAB and Simplorer simulators, as shown in Figure 10, so simulation results show Peak SNR of 88 dB.

B. Non-idealities analysis

1) DAC nonlinearity

Mismatches affecting the unit-elements are included in the behavioural model of the non-ideal D/A converter. A zero median Gaussian distribution is assumed for the unit elements

The performance of the proposed architecture is limited by the non-ideality of the DAC. Indeed the use of non ideal 4-bit DAC shows clearly that mismatch of the unit elements of the DAC can strongly degrades the SNR when the DWA is not
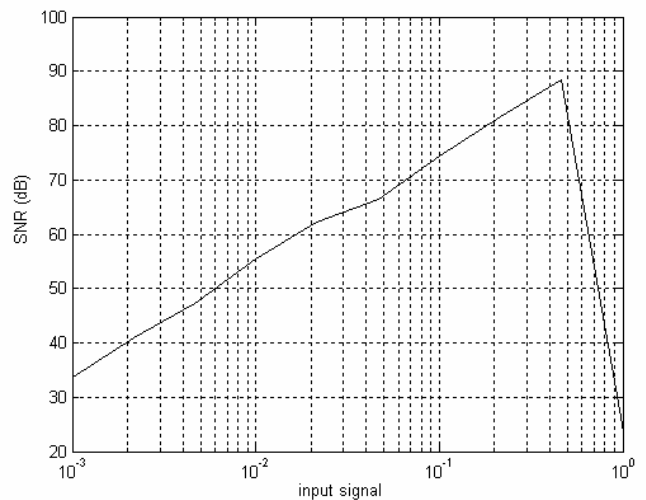

Fig. 10 SNR of ideal 2-1-1 4 bits modulator

introduced. In the behavioural model of DAC we assumed that the integral non-linearity (INL) is equal to 0.5 % full scale (FS). For the behavioural simulation results in fig 11, the DWA algorithm has been used in feedback to correct SNR degradation.

Figure12 shows the simulated output spectrum for a 100kHz input signal in WCDMA mode (2MHz bandwidth), using a 64MHz sampling frequency for an oversampling ratio of 16 under the condition of 0.5 % random mismatch among the feedback D/A converter elements

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2) Others nonidealities

Circuit imperfections degrading the $\Sigma\Delta$ modulator performance must be taken into account in practice. Then, the behavioural approach has been used to investigate the overall circuit nonidealities effects, to optimise the system parameters
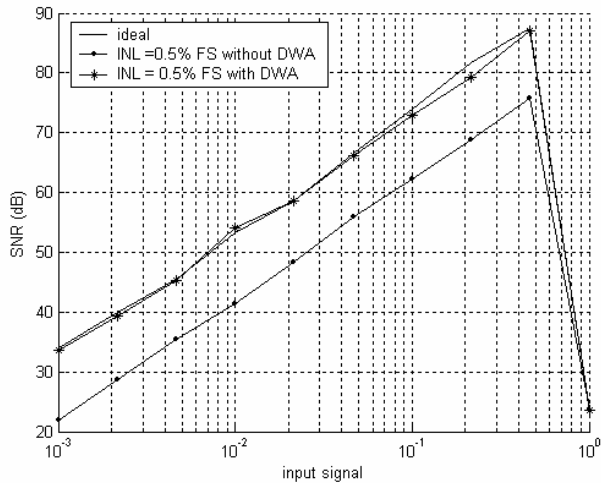

Fig. 11 Effect of DAC non-linearity and DWA correction (Simplorer simulation results)

and to establish the specifications of the analog blocks. Simulation has been performed using VHDL-AMS.

Several nonidealities of the SC integrator have been included in the behavioural model: finite OTA DC gain, slew rate and gain-bandwidth limitations, capacitor mismatch.

Figure13 shows the modulator putput spectrum obtained when simulated without (ideal modulator) and with the switches
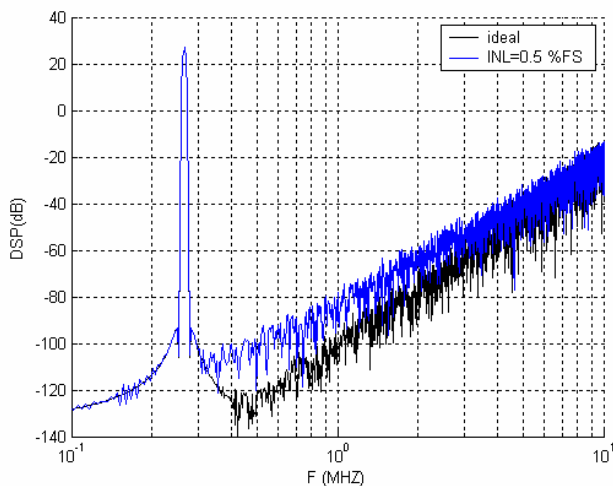

Fig. 12 DAC non-linearity effect on the output spectrum

thermal noise (KT/C) and the OTA noise considered in the SC integrators. theses nonidealities degrade the performance of the sigma delta modulator, so the behaviour of the converter deviate from its ideal one.

The integrator transfer function is multiplied by the gain

defined by the ratio of the sampling and the integration capacitors in a switched-capacitor implementation (see figure 2). A mismatch of the capacitor values resulting in an error of the integrator gain can be modelled by adjusting their ratio at the high level. Note that a capacitance ratio has a much higher precision than the absolute value of the respective capacitors.
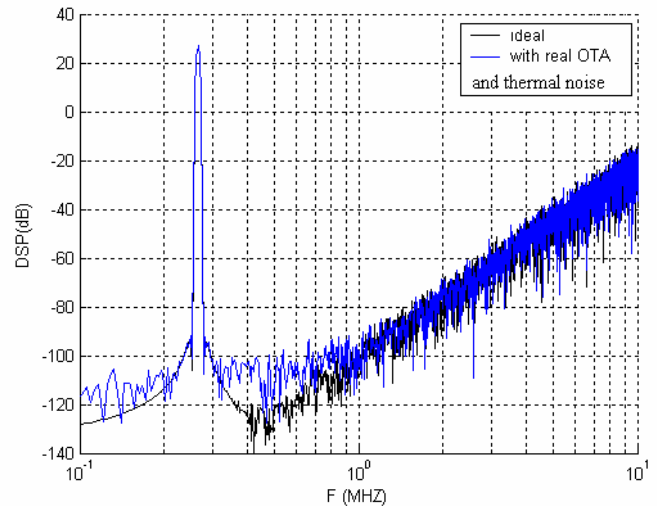

Fig. 13 Effect of noisy integrator on the output spectrum

As a result, this effect is normally not a problem for single-loop topologies. But the requirement for cascade structures is stricter due to the effect of incomplete noise cancellation.

In SC implementations of our modulator, capacitor mismatch precludes exact realization of the analog coefficient values. Then values of integrator weights differ from nominal ones due to mismatch in capacitors ratios. In the behavioral model integrators we assume that the mismatch error of integrator weights (capacitors) has Gaussian distribution with Standard deviation "sigma". For the behavioral simulation results in figure 14 a 0.1% of sigma causes 1.7 dB SNR degradation.

VII. CONCLUSION

A high bandwidth sigma-delta modulator for high-data-rate wireless applications was proposed. The modulator employs 4-bits quantization in the final stage of a 2-1-1 cascaded architecture and operates at low OSR of 16. The drawback of this architecture is very sensitive to DAC nonlinearities caused by capacitors mismatch. In order to increase the SNR at presence of internal multibit DAC error, a DWA algorithm is introduced. A behavioural model of the switched capacitor ADC is proposed in order to characterize the sigma-delta modulator. Simulation results show the efficiency of the employed algorithm to cancel the whole nonlinearities. The architecture permits to reach 88 dB of SNR at a 16 OSR suitable for WCDMA application.

The evaluation of the performance of the proposed modulator has been done with VHDL-AMS language suitable

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for time-domain behavioural simulations of SC $\Sigma\Delta$ modulators. The proposed set of building blocks models takes into account at the behavioural level most of SC $\Sigma\Delta$ modulator nonidealities, such as DAC non-linearity, OTA parameters (finite DC gain, finite bandwidth, slew rate and saturation voltages), thermal noise and capacitor mismatch, thus permit us to obtain a good estimation of the $\Sigma\Delta$ modulator performance with a short simulation time. The simulation results indicate that the proposed architecture has a good tolerance to circuit imperfections.

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