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Effect of Curing Profile to Eliminate the Voids / Black Dots Formation in Underfill Epoxy for Hi-CTE Flip Chip Packaging

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Abstract**—**Void formation in underfill is considered as failure in flip chip manufacturing process. Void formation possibly caused by several factors such as poor soldering and flux residue during die attach process, void entrapment due moisture contamination, dispense pattern process and setting up the curing process. This paper presents the comparison of single step and two steps curing profile towards the void and black dots formation in underfill for Hi-CTE Flip Chip Ceramic Ball Grid Array Package (FC-CBGA). Statistic analysis was conducted to analyze how different factors such as wafer lot, sawing technique, underfill fillet height and curing profile recipe were affected the formation of voids and black dots. A C-Mode Scanning Aqoustic Microscopy (C-SAM) was used to scan the total count of voids and black dots. It was shown that the 2 steps curing profile provided solution for void elimination and black dots in underfill after curing process.

Keywords**—**black dots formation, curing profile, FC-CBGA, underfill, void formation,

I. INTRODUCTION

UNDERFILL development accelerated with the introduction of epoxy-based laminates as substrates for flip chip assemblies [1]. A large CTE mismatch between the laminate and silicon (typically 12ppm/°C or greater) made underfill a necessity to prevent very rapid solder fatigue. The underfill spreads the stresses caused by the CTE mismatch over the entire area of the die and the substrate [2]. As with many packaging assemblies, the dominant causes of early failure of flip chip devices are assembly related, either interfacial delamination between the underfill and the die or voids in the underfill encapsulant [3].

In obtaining a stable reliability, it is important to prevent voids when encapsulating with underfill. It is especially easy to generate voids with organic substrates. Conventionally, some papers reported that the leaving time after pre-baking of a substrate and the pre-bake conditions have an influence on voids [4]. However, it is difficult to manage the leaving time strictly during the actual process. Moreover, processes, such as plasma cleaning; are also added after pre-bake process, and this tends to lengthen the leaving time. Voids are considered as failure factor for flip chip underfill encapsulant process. The existence of void will deteriorate the reliability of the package. Others factors affecting void formation in underfill especially in using capillary dispensing technique are air entrapment during dispensing process, flux residue of no clean flux after die attach or solder reflow process, cleaning solvent residue used to wash away the clean flux after die attach process, underfill dispensing method (weight, rate and pattern) and void entrapment caused by moisture contamination [5-8]. Bump arrangement and surface of substrate condition also induced voids formation especially during underfill flow and curing process.

It was reported that the size of the filler in the underfill material affects flow speed and void in flip chip packages with a narrow gap. Package contamination, like organic matter and flux, causes poor flow-ability and void. Concerning the area bump arrangement of a flip chip package, there are so many bumps under the die that the flow speed of the underfill material under the die is slower than that around the die [9]. The underfill material is filled around the die before it is completely filled under the die. As a result, there are unfilled parts under the die. These parts do not come out at curing time and remain as voids. Although a void may not exist before the underfill material is cured, a void may exist after the underfill material is cured [10]. This phenomenon was investigated in terms of package structure, especially the surface condition of the substrate[10].

Nowadays the factor of curing profile was found as main issue to the void formation in underfill for ceramic flip chip package in industry. The analysis have been performed to identify the root cause of curing process as a factor of void generation. Instead of voids, other abnormal phenomena occurred in underfill during curing process were black dots. Even though industry not considered this phenomena as not to deteriorate the performance of flip chip package, but their existence become interesting issue need to be investigated. The formation of black dots appeared along with voids. Its may be happened due to improper curing profile during curing process. Nevertheless, in this paper the reduction of voids and black dots are getting more attention to be

discussed rather than explanations of physical condition of them.

This paper is to present the implementation of two step curing profile method in order to reduce or eliminate voids and black dots in underfill during curing process. Statistic analysis is used to observe the effect of different curing profile, fillet geometry and wafer lots to optimize suitable curing profile of underfill for 90 nm CMOS technology, low-K HiCTE Flip Chip Ceramic Ball Grid Array (HiCTE FC CBGA).

II. Methods of Experiement

A commercial underfill epoxy was supplied by Ablestik, USA so called UF8829. The material properties is shown in Table 1.

TABLE I
MATERIAL PROPERTIES FOR UNDERFILL

Appearance	Off- White
Filler Particle Size (Ave, Max) and Type	1.2 um, 7um Silica
Filler Loading	60%
Viscosity at 25°C	13000 cP
Glass Transition Temperature Tg	122 °C
CTE 1/2	25C/80 °C
Young's Modulus (< Tg)	6.45 GPa
Moisture absorption (after PCT 20 Hrs	0.9 %
Dispensing condition	90-100°C

The test vehicle was HiCTE ceramic package composing 12 x 15 mm^2 active silicon die. The product is a high speed and high power microprocessor device for automotive application. The die was developed with CMOS 90 nm technology, internally engineered low-k dielectric and polyimide (PI) passivation. The bump was high lead Pb90Sn10 and reflowed up to 65 um maximum height with pitch size of 150 um. The die was placed to ceramic substrate with size of 33 x 33 mm^2 using automatic die placement machine namely ESEC Micron 5003. Washable flux from Senju Corporation was used for die attachment before solder reflow process. The package was then put in reflow oven with nitrogen flow rate of 430LPM, maximum oxygen content not more than 50 ppm and maximum H_2O permitted not more than 3GPM and then flux residue was washed away by using mix DI water and organic solvent.

The package was underwent plasma cleaning process for one minute to remove any unwanted contaminant prior to underfilling process. Underfill was capillary dispensed to into the gap between die and substrate using Asymtek DS-9000 Underfill Dispenser with preheating temperature of 90-100 ^{O}C and then final cured at certain temperature and time as shown in Table 3. The dispenser was set-up so that the package has full and half underfill fillet height. Finally, the assembly is inspected using acoustic microscopy. A Sonoscan model D6000 C-SAM is used to inspect the assemblies for underfill void and black dots formation. Fig. 2 shows the basic of process flow using conventional capillary force dispensing technique.

The output products were classified into several run order which consist of different parameters/factors. Two design of experiment (DOE) were managed in such away the root cause of voids can be analyzed and indentified. Several process factors were affected void/black dots formation ; different wafer lot, fillet height geometry, air blow process before underfill's dispensing and curing profile. Fig. 3 is example of sample for different fillet height. By controlling the needle gage epoxy volume, dispense pattern and needle placaement while underfilling process, the target to obtain different fillet type is accomplished.

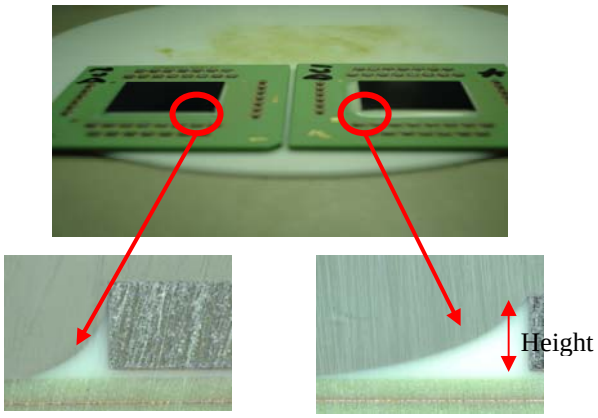


Fig. 3 Underfill fillet with full height (right) and reduced height

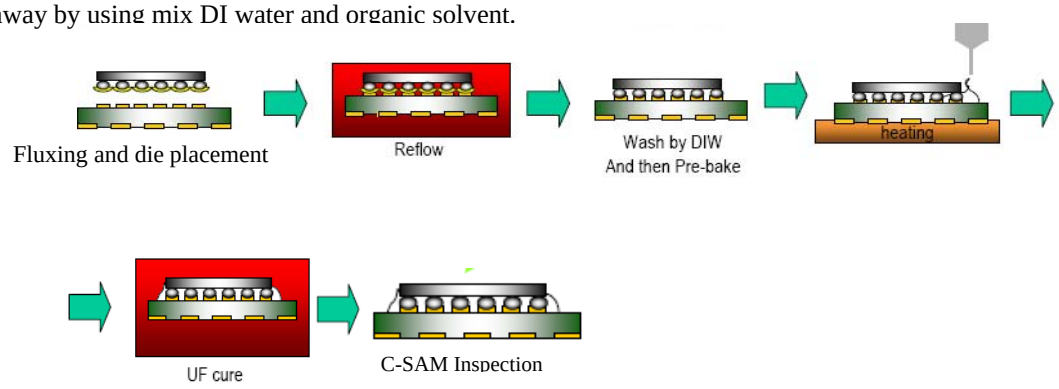


Fig. 2 Basic process flow of Flip Chip Packaging using capillary dispensing technique

Three Design of Experiments (DOE) were managed in order to study the effect of different curing profile, underfill fillet height, laser groove and wafer lots and air blow cleaning. DOE was arranged as follows;

A. DOE 1

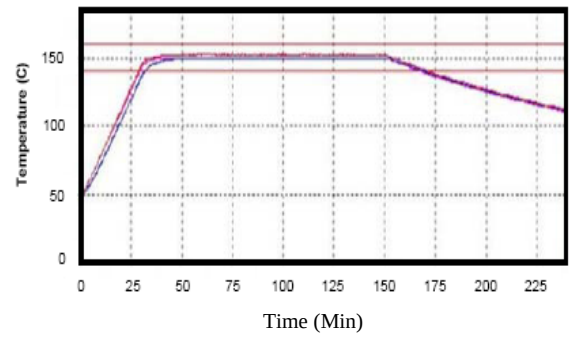
To study the effect of clean air blow before dispensing (to remove foreign material), UF recipe (full fillet/reduced fillet) and wafer lot on the void/black dots issue. Eight run orders were designed to obtained the conclusion. The single step curing profile of 150 °C @ 2 hours was used. For each run order, 50 units test sample were used.

B. DOE 2

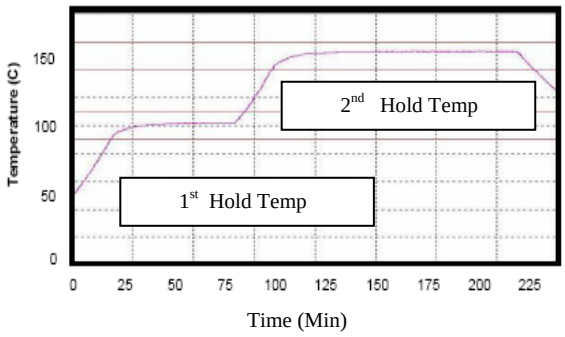
To study the effect UF recipe and cure profile on the void/black dots issue. seven run orders were designed to obtained the conclusion. The single step curing profile of 150 °C @ 2 hours and two steps curing profile (100°C for 1 hour + 150°C for 2 hours**)** was used. Figure 4 shows the curing profile to be used during curing process. For each RunOrder, 50 units test sample were used.

C. DOE 3

To study the effect of different 2-step curing profile on the void/black dots formation. Instead of two profiles used in DOE 2, another one 2-steps profile is added which is 120°C for 2 hours + 150°C for 2 hour as shown in Figure 4. For each RunOrder, 50 units test sample were used.



(a)



(b)

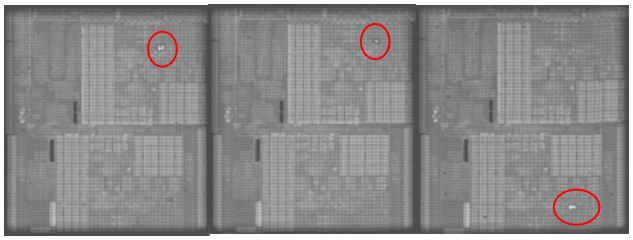
Fig. 4 (a) Single Step curing profile (b) Two steps curing profile

III. Results and Discussions

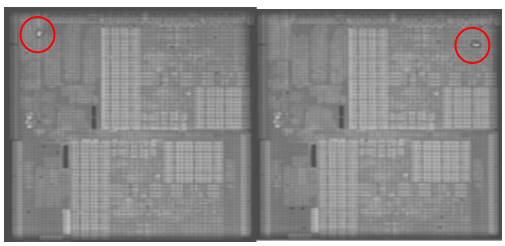
From the Table 2, the units from wafer lots 2 with reduced fillet height shows the voids formations and highest number of black dots. To confirm this correlation, statistic analysis for main effect plot and interaction plot was conducted using Minitab Statistic Software. Figure 5 depicts the void condition for Run Order 4 and 8 scanned by C-SAM.

Table II Result of Voids and Black Dots Formation for DOE 1

Run Order	Wafer Lot	Blow	UF Fillet	Quantity	Voids	Black dots
1	1	No	Reduced	50	0	96
2	2	Yes	Full	50	0	343
3	1	Yes	Full	50	0	128
4	**2**	**No**	**Reduced**	**50**	**3**	**472**
5	1	Yes	Reduced	50	0	179
6	1	No	Full	50	0	135
7	2	No	Full	50	0	319
8	**2**	**Yes**	**Reduced**	**50**	**2**	**483**



(a)



(b)

Fig. 5 C-SAM detected voids in (a) RunOrder 4 (b) RunOrder 8

From Figure 6, Main effects plots show that the wafer lot 2 and reduced fillet recipe are the main effects that contribute to the void counts while the blow process giving less significant as a factor to void formation. The units from wafer lot 1 regardless the condition of air blow or underfill fillet height. The interaction plot shows how fillet height and wafer lot having good interaction in inducing the void formation.

In the DOE 2 all units taken from Wafer Lot 1 since the result from previous DOE 1 exhibits this lot has void free and less no of black dots formation. From the Table 3, the RunOrder 1 and 6 (single step and reduced fillet) having voids and high number of black dots while. Two steps cure profile shows no voids formation and excellently reduced the blacks dot regardless laser gloove application and underfill fillet geometry. To confirm the main factor of voids and black dots formation, statistic analysis for main effect plot was conducted using Minitab Statistic Software. Fig. 6 depicts the void condition for RunOrder 1 and 6 scanned by C-SAM.

TABLE III RESULT OF VOIDS AND BLACK DOTS FORMATION FOR DOE 2

Run Order	Cure Profile	UF Fillet	Quantity	Voids	Black dots
1	**Single Step**	**Reduced**	**50**	**5**	**779**
2	Two Steps	Reduced	50	0	106
3	Single Step	Full	50	0	707
4	Two Steps	Full	50	0	189
5	Two Steps	Full	50	0	117
6	Two Steps	Reduced	50	0	297
7	Single Steps	Full	50	0	496

From the main plot effect depicted in Fig. 6, its shows reduced fillet and cure profile is the most significant factor for voids. With reduced fillet and 1-step cure the voids is obviously formed. The interesting result also shown, with the full height fillet geometry, the voids did not form during curing process. With DOE 2 result, 2-steps curing process is confirmed to help the elimination of voids and reduction the number of blacks dots tremendously

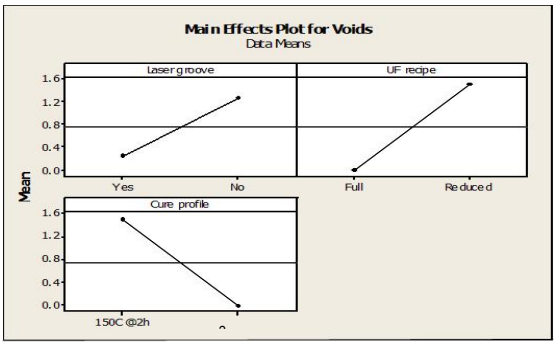
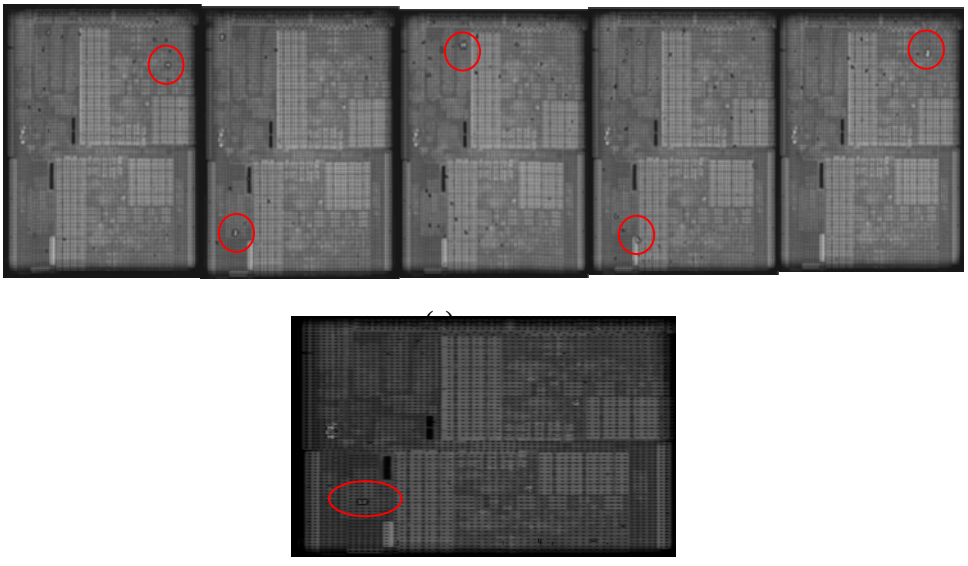


Fig. 7 Main effect plot for voids for DOE 2



(b)

Fig. 6 C-SAM detected voids in (a) RunOrder 1 (b) RunOrder 6

Table 4 summarized DOE 3 that for wafer lot 1, there is no voids observed in 1-Step_150C@2h and 2-Step_hold at 100C@1h, 150C@2h. However, voids showed at 2-Step_hold at120C@1h, 150C@2h and this 3 voids is not encompass two bumps. For wafer lot 2, both 1-step cure profile was having the voids which encompassed two bumps, while for both 2-step cure profile, the cured underfill are voidless. The C-SAM photo in Fig. 8, shows the condition of voids formation for both wafer lot. As a result, the first recipe of 2 steps curing profile (100C@1h, 50C@2h) is the best option due to no voids exist for both wafer lots.

TABLE IV EFFECT OF CURING PROFILE TOWARD VOID FORMATION

Cure Profile	Wafer Lot 1		Wafer Lot 2	
	Black Dots	Voids	Black Dot	Voids
1 Step _150C @ 2h	491	0	548	7
2 Step_hold 100C@1h, 150C@2h	31	0	71	0
2 Step_hold 120C@2h, 150@2h	31	3	20	0

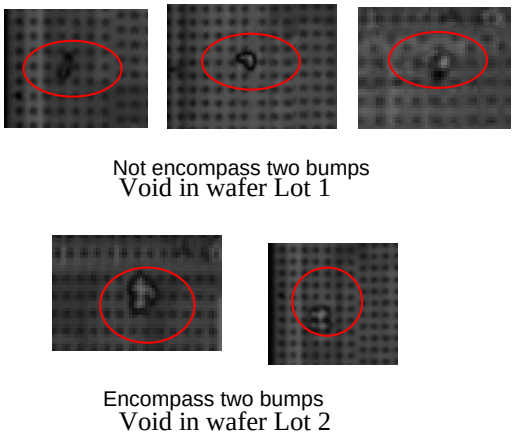


Fig. 8 Void condition for different wafer lot

Periodic observation of void formation during curing process was conducted for 2-steps curing process. Fig. 8 shows the summary of the observation process. At every intervals of 5 minutes during the cure, the units were taken out from oven and C-SAM inspection was executed. Two units were used for every read point and the unit re-loaded into oven to continue curing process until it complete.

There was no void observed during 1st ramp up and first hold temperature. It was interesting to see voids formed during 2nd ramp up. The voids were disappeared after 2nd hold temperature but blacks dots were obviously formed. Fig. 8 shows the sequence of void condition during ramp up time from 100°C until 150°C.

IV. Conclusion

This paper was presented how the factor of curing profile recipe helping to eliminate voids issue and reducing black dots formation in underfill for ceramic flip chip package in industry. Instead of that, factor of wafer cutting method, wafer lots, contamination cleaning using air blow and fillet geometry also gave impact to voids and black dots formations. It was found that 2 steps curing profile (100C@1h, 50C@2h) has significant impact to eliminate the voids and reduction the total counts of black dots in underfill during curing process. This new recipe was tremendously improved the voids issue occurred in FC-CBGA.

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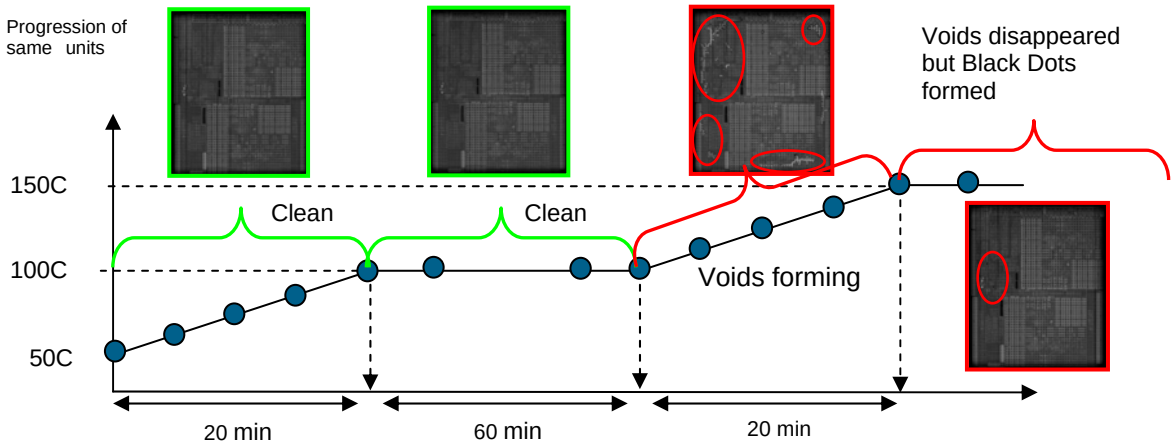

Fig. 9 : Progress of void and black dots formation during 2-steps curing

REFERENCES

[1] K. Kotaka, O. Suzuki and Y. Homma, " The Latest Underfill Materials for Flipchip Applications" *in Proc. 4th International Symposium in Material Packaging* , 2002, pp. 43-48

[2] M. Ying, A. Tengh, Y. C. Chea, and A. Mohtar, "Pb-free Solder Bump Reliability Evaluation for Flip-Chip-on Board", *in Proc. SEMI Technology Symposium*, Singapore, 2006, pp. 46-52

[3] T. Wang, J. M. Ling, M. Ying, et al, "The Effect of Underfill Materials on Lead-free Flip Chip Package Reliability", *Topical Workshop and Exhibition on Flip Chip Technology, IMAPS*, USA, 2004. pp. 57-62

[4] S. B. Park, S. W. Chung and Z. Tang, "Experimental Evidence of Underfill Voiding and Delamination during Board Level Assembly of Pb-free Solders", in Proc. 11th International Symposium on Advance Packaging Material, Processes, Properties and Interface, Atlanta, 2006, pp. 43-50

[5] S. Lee; M. J. Yim, R. N. Master, C. P. Wong, D. F. Baldwin, "Near Void-Free Assembly Development of Flip Chip Using No-Flow Underfill", *IEEE Trans. Electronics Packaging Manufacturing*, vol. 32, 2009, pp. 106-114

[6] M. Ying, A. Tengh, Y.C. Chea, "Process Development of Void Free Underfilling for Flip-chip-on-board", *in Proc. 9th IEEE Electronics Packaging Technology Conference*, Singapore, 2007, pp. 805-810

[7] M. Colella, and D. Baldwin, "Near void-free no-flow underfill flip chip on board assembly technology reliability characterization", *in Proc. International Manufacturing Technology Symposium*, USA, 2004, pp. 223-228

[8] S. L. B. Dal and N. T. Zamora "Identification of new mechanism of epoxy underfill void formation in electronic packages", in Proc. IEEE Reliability Physics Symposium, Philippines, 2005, pp. 508-512

[9] E. Goh, X. L. Zhao, Ashok Anand, and Y. C. Mui, "Mechanism of Underfill Voids Formation in Flip Chip Packaging", *in Proc. 7th IEEE Electronics Packaging Technology Conference*, Singapore ,2005, pp. 101-107

[10] P. S. Ho, Z.P. Xiong, K.H. Chua, "Study on Factors Affecting Underfill Flow and Underfill Voids in a Large-die Flip Chip Ball GridArray (FCBGA) Package", *in Proc. 9th IEEE Electronics Packaging Technology Conference*, Singapore 2007, pp 640-645