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Feed-Forward Control in Half-Bridge Resonant DC Link Inverter

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***Abstract*—**This paper proposes a feed-forward control in a half-bridge resonant dc link inverter. The configuration of feed-forward control is based on synchronous sigma-delta modulation and the half-bridge resonant dc link inverter consists of two inductors, one capacitor and two power switches. The simulation results show the proposed technique can reject non-ideal dc bus improving the total harmonic distortion.

***Keywords*—**Feed-forward control, Resonant dc link inverter, Synchronous sigma-delta modulation.

I. Introduction

THE dc bus voltage of resonant link converter techniques is resonated by an LC network and power switches. The oscillation of this network gives rise to instants of zero voltage. Therefore, the output power switches are connected to the network such that switching occurs at such zero crossing, and then switching losses are significantly reduced [1].

However, the resonant dc link system operates well under condition of an ideal dc bus (ripple-free) obtained by means of a passive dc link filter. To achieve a very low ripple, however, requires large filters. This increases the cost, size, and weight and reduces the overall efficiency of the conversion process. Furthermore, in a practical converter system, it is difficult to realize an ideal dc bus for a number of practical constraints. Most of the dc bus converter systems use a front-end diode bridge for ac–dc rectification. The ripple in the dc bus is undesirable, as it causes low-order harmonics appearing in the inverter output. These harmonics are difficult to filter out and cause deterioration in the quality of the output voltage.

This paper therefore proposes a feed forward control using synchronous sigma-delta modulation (SSDM) configuration. This control technique is used to control the new configuration of half-bridge resonant dc link (HB-RDCLI). The features of the proposed pattern generator are highlighted. The simulation results show the ripple rejection capability of the proposed control technique.

II. Resonant DC Link Equivalent Circuit

Fig. 1 shows the resonant dc link equivalent circuit. The switch Ms is turned on by the short pulse to provide initial condition of inverter operation. When Ms is opened, the dc bus oscillates and returns to zero generating, $v_d(t)$, where upon Ms is turned again. Then, this process can be repeated. So, it is possible that the power switches of inverter circuit can operate at high frequency rate without switching losses if they are turned on and turned off at zero crossing of $v_d(t)$. Therefore, the well-established modulation techniques such as pulse-width modulation (PWM) are not suitable for controlling this inverter system. But, the characteristic of zero crossing switching exists in a suitable set of integral pulse modulation techniques collectively known as delta modulation, comprise linear delta modulation, process integration, and sigma delta modulation [2]. The resonant link voltage, $v_d(t)$, is given by [1]:

$$v_d(t) = Z(i_{L(0)} - I_0)\sin(\omega t) + v_{dc} + (v_{d(0)} - v_{dc})\cos(\omega t) \quad (1)$$

where

$i_{L(0)}$ initial resonant inductor current;

$v_{d(0)}$ initial resonant capacitor voltage;

I_0 load current;

ω angular frequency = $2\pi f_c$;

Z resonant impedance = $\sqrt{L_r / C_r}$.

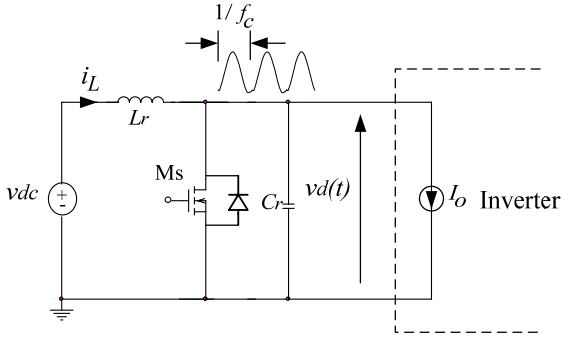

Fig. 1 Resonant dc link equivalent circuit with load I_o

Equation (1) indicates that the resonant link voltage $v_d(t)$ is a function of the dc bus voltage v_{dc} and swings to follow the variation of the v_{dc} in case of non-ideal dc bus. This causes the low order harmonics at inverter output. The feed-back control may be used to reject these harmonics. However, in case of the dc bus voltage v_{dc} is perturbed. The overshot

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voltage will be appeared at inverter output before the control process produces PWM signal. This problem can be solved by feed-forward control techniques [3] [4], however, they can not be applied in resonant dc link inverter.

III. Half Bridge Resonant DC Link Circuit

Generally, full-bridge inverter is the power output stage of resonant dc link circuit. To reduce the number of power switches, this paper uses two switches M1-2 and L_rC_r network producing the positive and negative resonant link voltages, $\pm v_{d1,2}(t)$ as shown in Fig. 2 (a). Fig. 2 (b) is the chopper output voltage, $v_h(t)$, in case of $v_i = 0\text{V}$. The average dc link voltage $\widetilde{v}_d$ can be found:

$$\widetilde{v}_d = \frac{4\text{V}_{dc}}{\pi(1+t_{on}/t_{off})} \tag{2}$$

This voltage $\widetilde{v}_d$ uses to determine the output voltage amplitude, v_o and is a function of dc bus voltage. In this control technique, the PWM signals Q and $\overline{\text{Q}}$ are modified to include the action of Ms for controlling M1 and M2. Therefore, the control logics for M1 and M2 as shown in Fig. 2 (c) are:

$$\text{M1} = \text{Q} + \overline{\text{Q}}\,\text{CLK} \tag{3}$$

$$\text{M2} = \overline{\text{Q}} + \text{QCLK} \tag{4}$$

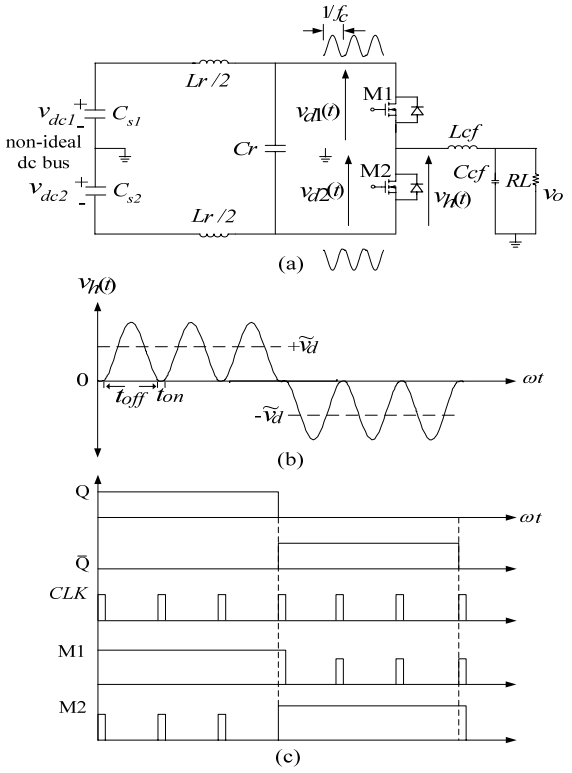

Fig. 2 (a) Half-bridge resonant dc link inverter (b) Chopper output voltage $v_h(t)$ (c) Generating gate control logics for M1and M2

IV. Feed Forward Control SSDM

Considering (2), the average dc link voltage $\widetilde{v}_d$ depends strongly on dc bus voltage. This can cause variation of output voltage in case of non-ideal dc bus. To reduce this effect, the feed forward control sigma-delta modulation (FFC-SSDM) as shown in Fig. 3 can be used. The non ideal dc bus is sent to be the control information and reduced by gain A. This voltage is controlled by the D-FF output Q and $\overline{\text{Q}}$ generating the forward voltage, $v_s(t)$. Therefore, the error signal, e, is the difference between the input voltage v_i and the forward voltage, $v_s(t)$. The $v_s(t)$ is fed to an integrator to produce the integrated error signal E. The E then is fed to a quantizer, the output of which depends on the polarity of E. For E positive an output of $+\text{V}_e$ is produced, whereas for negative values of E an output $-\text{V}_e$ is produced. The quantizer output is strobe by sample and hold (D-Flip-Flop) at a frequency f_c (the link frequency) to give the output waveforms Q and $\overline{\text{Q}}$.

In Fig. 4, assuming the input signal is dc voltage. At interval period A, the dc bus voltage sources, $v_{dc1,2}(t)$, are $\pm\text{V}_{\text{dc}}$. Therefore, the forward voltage equals to $\pm\text{V}_\text{s}$ and produces the constant slopes of integrated error signal E(t). The switching time can be determined by [5].

$$v_i = \frac{1}{T_{sn}}\int_0^{T_{sn}} \text{V}_\text{s}\,dt \tag{5}$$

$$T_{sn} = \frac{2T_c}{(1-m(t))} \tag{6}$$

where

$m(t)$ is the modulation index, $\frac{\text{V}_\text{i}}{\text{V}_\text{s}}\sin\omega t$ $(M\sin\omega t)$;

T_{sn} is the switching time;

T_c is the time period of clock signal.

In SSDM process, the pattern modulation repeats every L (number of limit cycles) modulation cycles. The T_{sn} could be different from modulation cycle to the next, although, the v_i and $v_s(t)$ are constant. This is simply because of discretized nature of output. However, this steady state error process will be not considered in this paper. Considering (7), the modulation cycle T_{sn} is proportional to $v_{dc}(t)$. When the $v_{dc}(t)$ increases T_{sn} is reduced as shown in Fig. 4 at interval period B. In other words, when the $v_{dc}(t)$ reduces, the T_{sn} increases, respectively. The T_{sn} is still corresponded with pulse number of resonant dc link voltage.

$$p_n = \frac{T_{sn}}{T_c} - 1 \tag{7}$$

where

p_n is the pulse number of positive resonant dc link voltage.

The chopper output voltage average of inverter, $\widetilde{v}_h$, can be found by integrating $v_h(t)$.

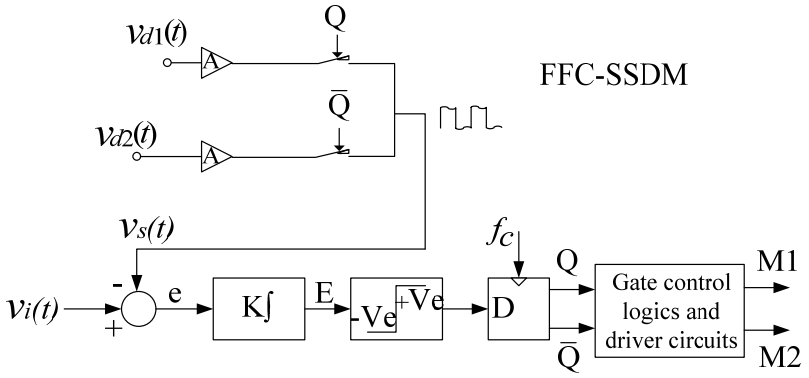

Fig. 3 Block diagram of FFC-SSDM

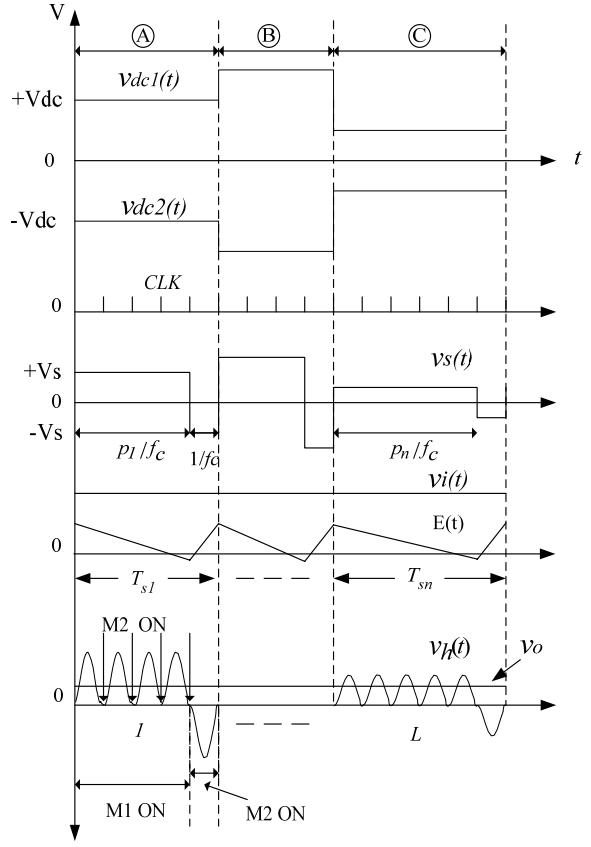

Fig. 4 Key waveforms of FFC-SSDM

$$\tilde{v}_h = \tilde{v}_d \frac{(p_n - 1)}{(p_n + 1)} \quad (8)$$

As shown in Fig. 4, p_n is varied as proportional to T_{sn} and $v_{dc}(t)$. Therefore, the chopper output voltage average is equal to v_i in each modulation cycle. The result is to reject the non-ideal dc bus voltage. This should also be true in case of sinusoidal input voltage. However, there are some parameters that affect the ripple rejection capability, which will be discussed and simulated in the next topic.

V. Simulation Results

This section shows the PSPICE simulated results using control configuration in Fig. 5. The system parameters are set as following: f_i = 50 Hz; M = 0.5; feed forward gain, A = 0.032 and f_c = 40 kHz. The rectifier circuits use small-size capacitor filters 2,000 uF causing high ripple voltage at dc bus. The resolution of Fast Fourier transform (FFT) for measuring harmonics spectrum is set at 5 Hz (sampling time 100 mS). The forty order harmonics are used to measure the distortion factor (*DF*) and total harmonic distortion (*THD*). Fig. 6 is the results of open loop control. Fig. 6 (a), the chopper output voltage $v_h(t)$ swings to follow the variation of the dc bus voltage. This results the low order harmonics appearing at $v_h(t)$ as shown in Fig. 6 (b). This causes the *THD* of output voltage is high at 3.2%. Fig. 7 shows the results of FFC-SSDM. In Fig. 7 (a), the chopper output voltage $v_h(t)$ seems containing low order harmonics. However, the number of pulse p_n in each period is proportional with the dc bus voltage source. The result is that the chopper output voltage average equals the input voltage. Therefore, there are no the low order harmonics at $v_h(t)$, which is confirmed by simulation result as shown in Fig. 7 (b). The *THD* of output voltage is low at 1.5%.

Figs. 8 and 9 show the ripple rejection capability. In Fig. 8, the various control techniques were tested under the conditions that $v_{dc1,2}$ = 155 V + v_r where $v_r = 30\sin(2\pi 100t)$ is assumed as ripple voltage. The *DF* of open loop control while $v_r = 0$ is used as a reference value. The results indicate that the *DF* of FFC-SSDM closes to the reference value. Fig. 9 shows the effect of ripple frequency, f_r and modulation index M. To measure the harmonic spectrum amplitude of $v_h(t)$, the input signal is set as dc voltage and measured at ripple frequency, f_r. The results show that when the f_r and M are increased causing the error voltage in each period. This reduces the rejection capability. However, in the most practical applications, the dc bus voltage that is generated by means of a diode rectifier has only low ripple frequency.

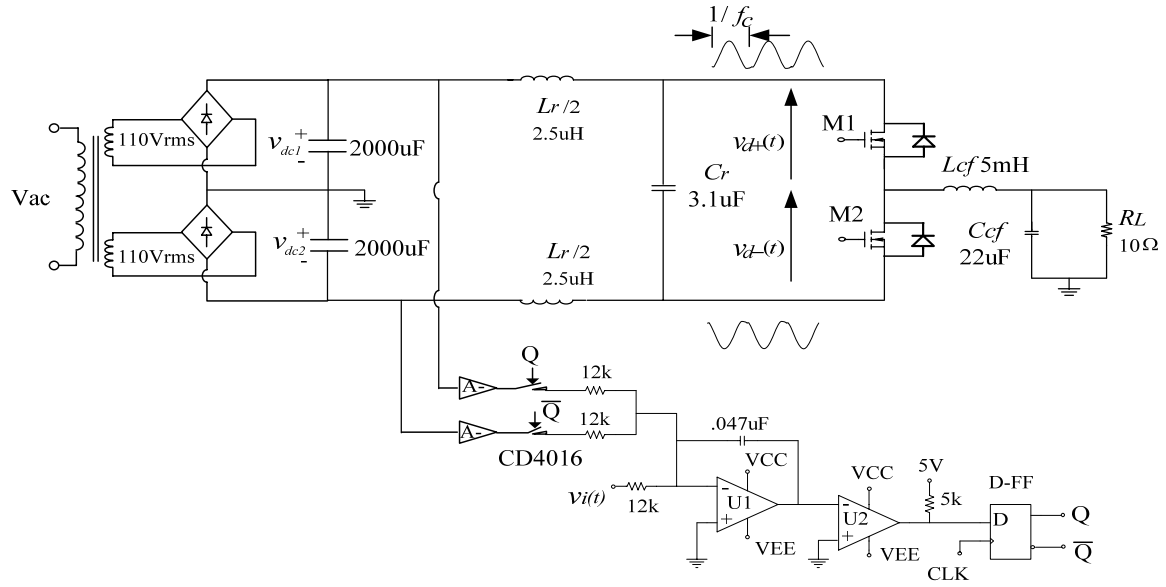

Fig. 5 FFC-SSDM Circuit implementation

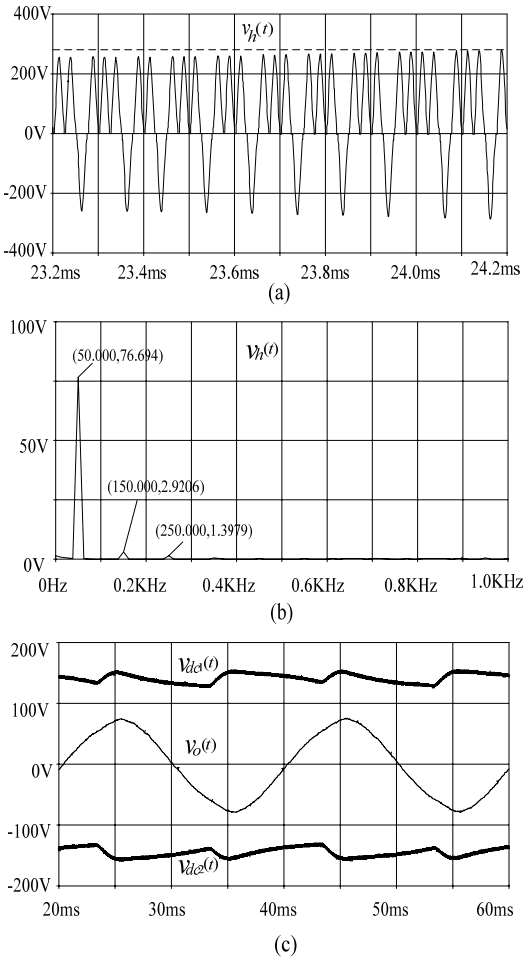

Fig. 6 Simulation results of open loop control (a) Chopper output voltage vh(t) and its harmonic spectrum (b). (c) DC bus voltage source and output voltage

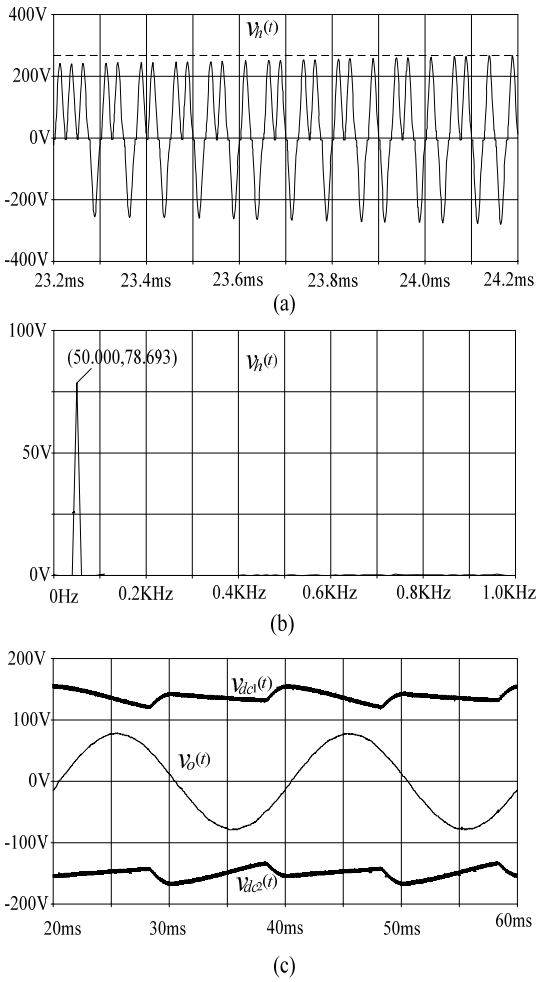

Fig. 7 Simulation results of FFC-SSDM (a) Chopper output voltage vh(t) and its harmonic spectrum (b). (c) DC bus voltage source and output voltage

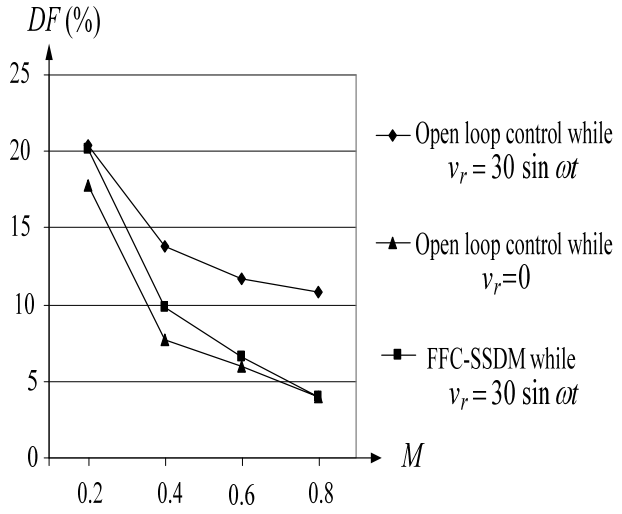

Fig. 8 Distortion factors of open loop control comparing with FFC-SSDM

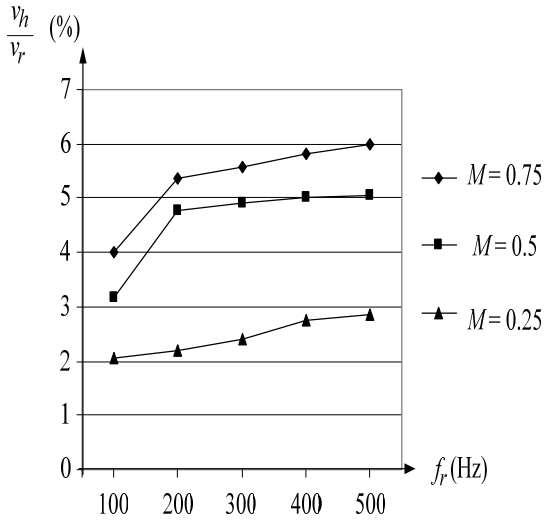

Fig. 9 Ripple rejection capability of FFC-SSDM

VI. Conclusion

This paper proposed the feed-forward control in half-bridge resonant dc link inverter. The system configuration is very simple but has efficiency in rejecting the non-ideal dc bus. The effects of parameters to rejection capability were explained and confirmed by simulation results.

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