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An Algorithm Proposed for FIR Filter Coefficients Representation

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***Abstract*—**Finite impulse response (FIR) filters have the advantage of linear phase, guaranteed stability, fewer finite precision errors, and efficient implementation. In contrast, they have a major disadvantage of high order need (more coefficients) than IIR counterpart with comparable performance. The high order demand imposes more hardware requirements, arithmetic operations, area usage, and power consumption when designing and fabricating the filter. Therefore, minimizing or reducing these parameters, is a major goal or target in digital filter design task. This paper presents an algorithm proposed for modifying values and the number of non-zero coefficients used to represent the FIR digital pulse shaping filter response. With this algorithm, the FIR filter frequency and phase response can be represented with a minimum number of non-zero coefficients. Therefore, reducing the arithmetic complexity needed to get the filter output. Consequently, the system characteristic i.e. power consumption, area usage, and processing time are also reduced. The proposed algorithm is more powerful when integrated with multiplierless algorithms such as distributed arithmetic (DA) in designing high order digital FIR filters. Here the DA usage eliminates the need for multipliers when implementing the multiply and accumulate unit (MAC) and the proposed algorithm will reduce the number of adders and addition operations needed through the minimization of the non-zero values coefficients to get the filter output.

***Keywords*—**Pulse shaping Filter, Distributed Arithmetic, Optimization algorithm.

I. Introduction

DUE to the intensive use of FIR filters in video and communication systems, high performance in speed, area and power consumption is demanded. Basically, digital filters are used to modify the characteristic of signals in time and frequency domain and have been recognized as primary digital signal processing operations [1]. They are typically implemented as multiply and accumulate (MAC) algorithms with the use of special DSP devices [2, 3, 4]. Fig. 1 shows how MAC is implemented with N multiplications and (N-1) additions per sample to compute the result.

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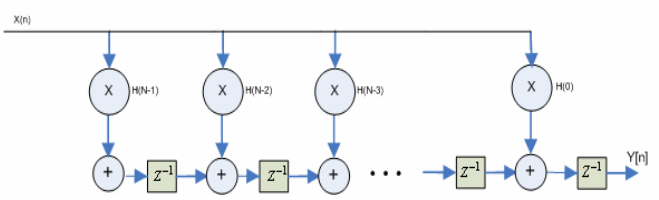

Fig. 1 MAC FIR Filter Block Diagram

In modern digital communication systems, pulse-shaping filters allow the transmission of pulses with negligible intersymbol interference. This means that, pulse-shaping digital filter is a useful means to shape the signal spectrum and avoid interference of ultra wideband (UWB) to other legacy narrow band signals [5]. The beauty of pulse-shaping filter concept is that rectangular pulses which cannot cause interference during the sampling time of other pulses can be used as an input to the filter.

However, due to increasing demand for video signal processing and transmission, high speed and high order FIR filter have frequently been applied for performing adaptive pulse-shaping and signal equalization on the received data in the real time [6]. Hence minimizing the computational complexity and the system cost in terms of power consumption and memory storage needed is a major target in digital filter design task. The computational complexity is a function of the multipliers and adders used in filter realization [7]. However, applying multiplierless techniques as in [8] will make the total number of adders in cascade a measure of its computational complexity. This paper presents an algorithm proposed to reduce the number of non-zero filter coefficients so that the number of adders required, and addition operation carried out to get the filter output will also be reduced.

II. General Background

A. FIR Filter Design

Digital finite impulse response filters have been used in signal processing as ghost cancellation and channel equalization [9]. FIR filtering of which the output is described in Equation 1 is realized by a large number of adders, multipliers and delay elements.

$$Y[n] = \sum_{k=0}^{N-1} h[k] \cdot X[n-k] \qquad (1)$$

Where $Y[n]$ is the filter output, $X[n-k]$ is input data, and $h[k]$ is the filter coefficient. Direct form of a finite word

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length FIR filter generally begins with rounding or truncating the optimum infinite precision coefficients determined by McClellan and Parks algorithm [10].

Due to the enormous occupied area of FIR filters with a large number of taps, hardware-reusing architectures such as time-multiplexing architectures as in [9] and [11] and a distributed arithmetic (DA) approach based on bit-serial access [8], have been widely adopted for implementation [12]. Canonical Signed-Digit (CSD) coefficient representation has also been used by many researchers for designing multiplierless high speed FIR filters [13]. Canonical Signed Digit encoding is used for coefficients to minimize the number of additions. In many signal processing and communication applications such as FIR filters, video and image processing, a multiplication with constants e.g. filter coefficients have to be performed. Therefore, the use of multiplierless techniques is inspired to avoid the need of establishing an expensive general purpose multiplier e.g. on the FPGA and instead computing constant multiplications using table lookups and additions.

B. Distributed Arithmetic

An alternative to the approach shown in Fig. 1 is the DA technique which is well known method to save resources. However, using this approach the filter can be implemented in bit serial or parallel mode to trade bandwidth for area utilization. The input variable in equation (1) can be represented in its weighted format as in equation (2).

$$x_k = -x_{n,k-1} + \sum_{m=1}^{k-1} x_{n,k-1-m}\, 2^{-m} \qquad (2)$$

Using equation (2) in (1) and after some mathematical manipulations the filter output given in equation (1) can be written as in equation (3).

$$Y = \sum_{m=0}^{k-1} \sum_{k=0}^{k-1} Z_{k-1-m}\, 2^{-m} \qquad (3)$$

Implementing equation (3) in bit serial DA basic structure [8] will result in constructing lookup table (LUT) of size 2^m (m is the number of input variables e.g. filter coefficients). This is the major drawback of the basic DA architecture which made it sometimes impractical for designing high order FIR digital filters. In [14], this problem has been overcome by proposing a new architecture for the DALUT so that its size is independent of the number of input variables or filter coefficient.

C. Pulse Shaping

In any transmission system, where pulses are transmitted and ultimately detected by the receiver, the goal is to sample the received signal at optimal points in the pulse interval so that the probability of an accurate binary decision is maximized. This implies that the fundamental shapes of the pulses be such that they do not interfere with one another at the optimal point i.e. have zero value at sampling points. In addition, the pulse amplitude must decay rapidly outside the pulse interval. In real systems, it is proved that the quicker a pulse decays outside its interval, the less likely it allow timing jitter to introduce errors when sampling adjacent pulses. One example of a zero-ISI pulse shape is the raised cosine pulse given in equation (4).

$$p(t) = \frac{\sin \pi t/T}{\pi t/T} \frac{\cos(\hat{t}/T)}{1 - 4\beta^2 t^2/-2} \qquad (4)$$

Replacing t by t-td = (t–mT) letting t=nTs and T=kTs yields

$$\frac{t}{T} \rightarrow \frac{nT_s \quad mkT_s}{kT_s} = \frac{n}{k} - m$$

Making this substitution in equation (4) gives the sample sequence

$$p[n] = \frac{\sin \pi \{(n/k) - m\}}{\pi \{(n/k) - m\}} \frac{\cos(\{(n/k) - m\})}{1 - 4\beta^2 \{(n/k) - m\}^2} \qquad 0 \le n \le 2m$$

When the filter response is p[n] and the input x[n]=δ[n-1] then the filter output is represented by

$$y[n] \quad p[n] \otimes x[n] = p[n \quad 1] \qquad (5)$$

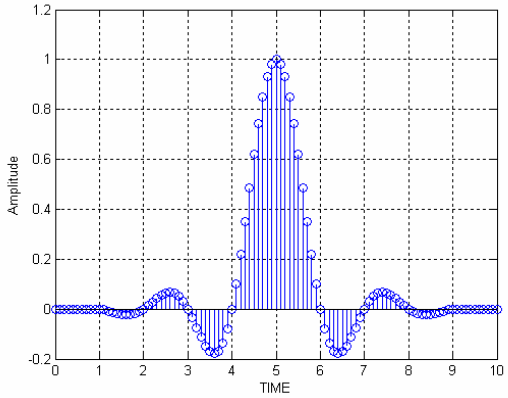

Fig. 2 Raised cosine pulse

and is shown in Fig. 2. It is clear from this Fig. that the pulse is identically equal to zero at integer multiples of the pulse duration.

III. Design and Methodology

A. The Proposed Algorithm

This section present the details of the algorithm proposed in this paper. The main goal of the proposed algorithm is to manipulate and reduced the number of non-zero coefficients used to represent the filter response. The proposed algorithm is summarized below:

1. Derive the filter coefficients based on the desired specifications using the MATLAB or any other filter design software program.
2. Multiply these coefficients with a constant value so that you get some of them greater than zero.
3. Round up the values obtained from step 2 to be integers.
4. The number of non zero values obtained from step 3 must represent at least 93% of the signal power.

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5. If the same signal power representation can be obtained with different constant values then the smaller value is chosen.
6. The values of the first and last coefficient produced from step 5 are equal to zero.
7. Change the values of the first and last coefficient to be non-zeros with their original sign in step 1.
8. Find the frequency response of the filter using the new set of coefficients and see whether it fulfills the desired specifications or not.
9. The absolute value of the first coefficient must be less than 10. Values greater than the proper one will cause either ripples in the passband and/or in transition band and/or maximize the gain factor of the filter response.
10. If ripples are there in the passband or the transition band region of the frequency response found in 8, then the first and last coefficient values must be reduced.
11. Divide the new set of coefficients by the constant used in step 2 so that the filter response is normalized back to zero magnitude.

B. Algorithm Analysis

The proposed algorithm starts with obtaining the filter coefficients based on desired specifications. Using the round function in MATLAB these coefficients are rounded to the nearest integer after being multiplied with a constant integer value. It is better if we choose the constant value to be a power of 2 i.e. (2^m) so that the division in step 11 is done simply by a right shift. The frequency domain representation obtained with the new set of coefficients must cover at least 93% of the signal power (see Fig. 3) otherwise; the filter performance with its new set of coefficients will differ much from its original one. The value of the constant must be the smaller if more than one constant can produce the same signal power. Smaller value will lead to less gain factor and less passband and/or transition band ripples.

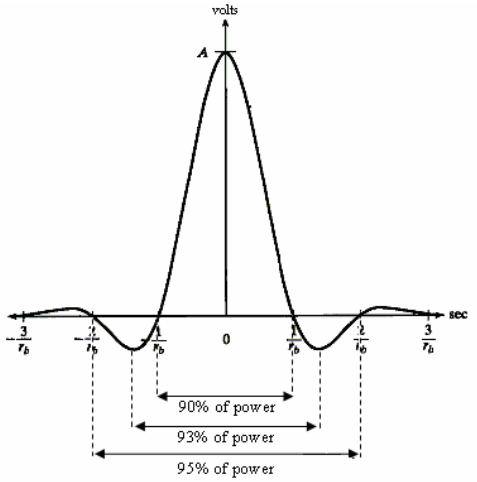

Fig. 3 Distribution of Transmitted Signal's average power

IV. CDMA Communication System

Code-division multiple access is one of several methods of multiplexing wireless users. In CDMA, users are multiplexed by distinct codes rather than by orthogonal frequency bands, as in frequency-division multiple access [15].

A. CDMA Concept

The enhancement in performance obtained from a direct sequence spread spectrum (DSSS) signal through the processing gain and the coding gain can be used to enable many DSSS signals to occupy the same channel bandwidth, provided that each signal has its own pseudorandom (signature) sequence [16]. Thus enable several users to transmit there information over the same channel bandwidth. This is the main concept of a CDMA communication system. The signal detection is accomplished at the receiver side by knowing the code sequence or signature of the desired user.

Since the bandwidth of the code signal is chosen to be much larger than the bandwidth of the information-bearing signal, the encoding process enlarges or spreads the spectrum of the signal. Therefore, it is also known as spread-spectrum modulation. The resulting signal is also called a spread-spectrum signal, and CDMA is often denoted as spread-spectrum multiple access. The processing gain factor is defined as the ratio of the transmitted bandwidth to information bandwidth and is given by:

$$Gp=Bt/Bi.$$

Correlating the received signal with a code signal from a certain user will then only despread the signal of this user, while the other spread-spectrum signals will remain spread over a large bandwidth.

B. The Proposed CDMA System

The CDMA communication link proposed in this paper is shown in Fig. 4. The performance in terms of the bit error rate is examined for different signal to noise ration values against a sinusoidal interference.

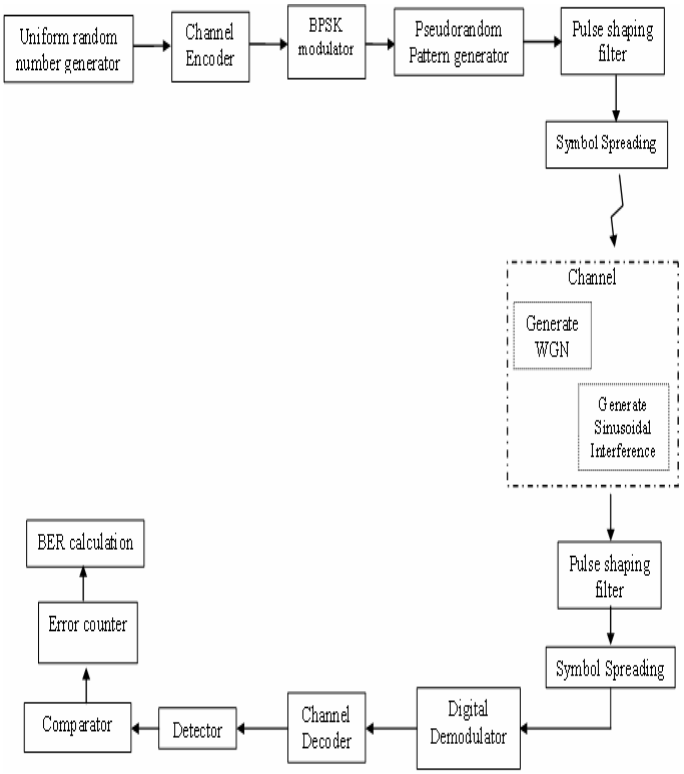

Fig. 4 The proposed CDMA system

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The binary phase shift keying modulation scheme is used for modulating the input data. The pseudorandom sequence is at both the transmitter and receiver side of the proposed system. The system is examined when a raised cosine pulse shaping filter is used at transmission only and when the matched filter is used at the receiver side.

V. Results and Discussion

1. FIR Filter Simulation

A number of simulation runs is performed for different FIR filter orders. The simulation includes both the filter with its original coefficients and with its new coefficients i.e. after applying the proposed algorithm. Fig. 5 (a) shows the simulation results for 80-tap raised cosine pulse-shaping filter with a rolloff factor of 0.22. On the other hand, Fig. 5 (b) shows the frequency and phase response of the filter with its new set i.e. after applying the proposed algorithm. In this Fig. the new set of coefficients are obtained when multiplying the original coefficients with a constant value 8 then rounded to integers and the first and last coefficients are set to a value of 5 (h[0] and h[80] = 5).

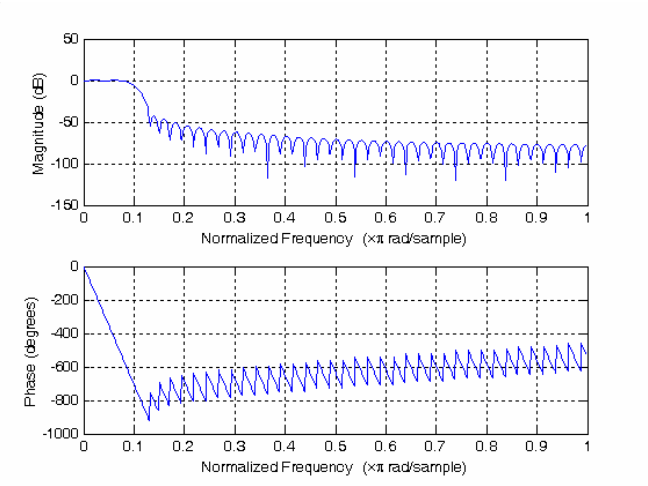

Fig. 5 (a) Phase and frequency response of the filter with its original coefficients

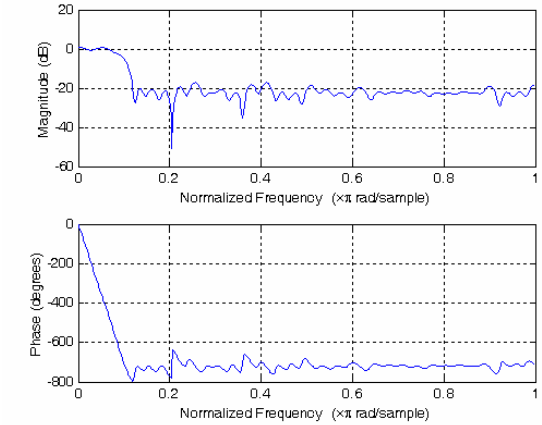

Fig. 5 (b) Phase and frequency response of the filter after using the proposed algorithm

It is known that the number of coefficients for an 80-tap filter is 81 coefficients. However, after applying the proposed algorithm, the number of non-zero coefficients became 41. This means that Fig. 5 (b) is obtained with only 41 coefficients. As a result of the number of addition operations needed is reduced by half. This has a very much influence on increasing the system speed and reducing the hardware complexity requirement. Therefore, simplifying the overall system given that the less hardware you use the more simple design you achieve.

The proposed algorithm has also been applied to designed square root raised cosine pulse shaping filter. The filter is used with the CDMA communication system shown in Fig. 4. The phase and frequency responses of this filter are shown in Fig. 6.

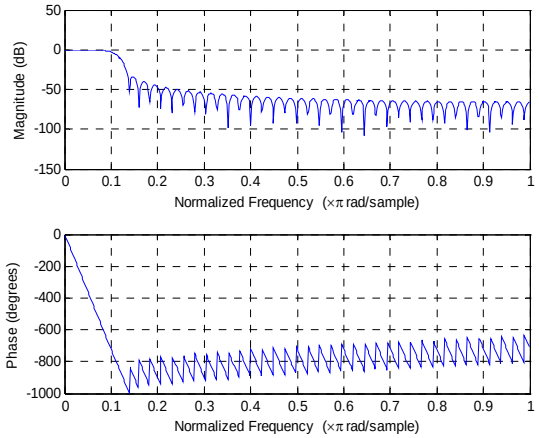

Fig. 6 (a) Response of the 80-tap square root RC filter with its original coefficients

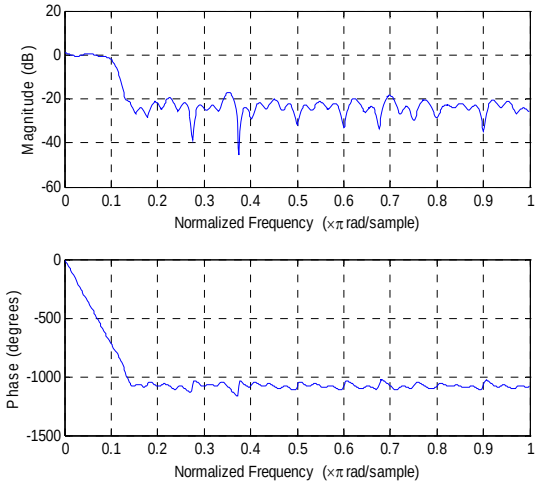

Fig. 6 (b) Response of the 80-tap square root RC filter after using the algorithm

The frequency and phase response of 512-tap FIR filter with its original coefficients is shown in Fig. 7 (a), whereas, the response with new coefficients is shown in Fig. 7 (b). In this case the constant value used to be multiplied with the original filter coefficients is 256. The first and last coefficients i.e. $h[0]$ and $h[512]$ are made equal to 3. Comparing the constant values in this case and the case of 80-tap filter, it is clear that the value here is much greater than that of the 80-tap filter case. The reason behind this increment is that an enough signal power 93% can not be achieved with small constants if the filter order is high e.g. 512-tap filter. Therefore, as the filter order increase, the constant value will probably increase. On the other hand, the value of the first and last coefficients is not a function of the filter order rather it is a filter specification dependent value. As it can be seen that the value of the 1st and last coefficient in the case of 512-tap filter is 3 whereas, in the case of 80-tap filter it is 5. The 512-tap FIR filter for which the

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frequency and phase responses are shown in Fig. 7 has a sampling frequency of 96000Hz and a cutoff frequency of 12000Hz, the rolloff factor α=0.22 (the CDMA suitable value), and the Hamming windowing is used when designing this filter.

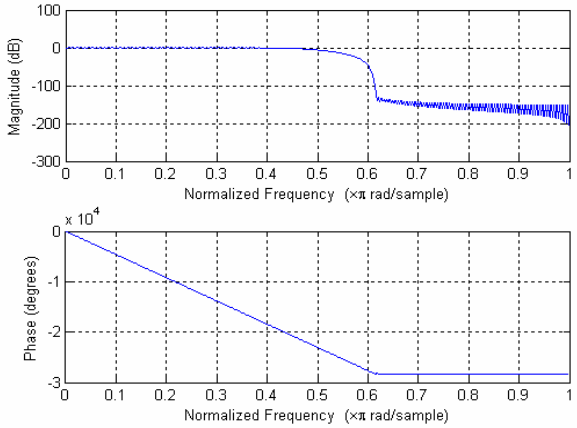

Fig. 7 (a) Phase and frequency response of the filter with its original coefficients

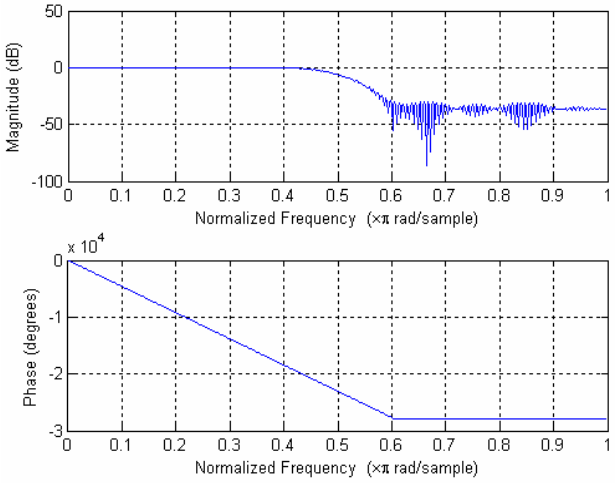

Fig. 7 (b) Phase and frequency response of the filter with the new coefficients

The impulse response for this filter for both cases is shown in Fig. 8.

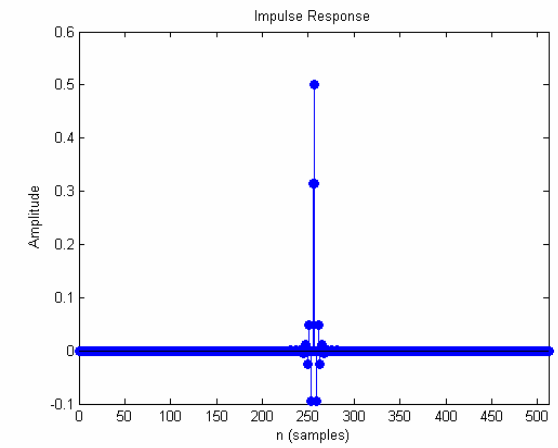

Fig. 8 (a) Impulse response of the filter with its original coefficients

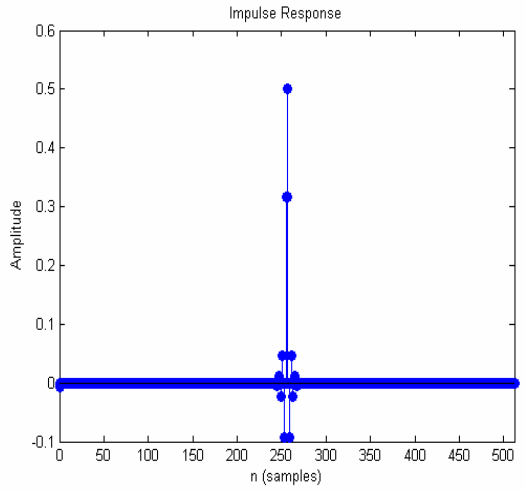

Fig. 8 (b) Impulse response of the filter after using the proposed algorithm

Table I shows arithmetic summary for the values obtained when applying the proposed algorithm to 512-tap FIR filter. It is clear from this table that the 1st coefficient value and the number of non-zero value coefficients increases with the value of constant value used. Table I also shows that when we use a constant value 256, the number of non-zero coefficients is the same as the case when we multiply by 128. Therefore, the 128 value has the priority to be chosen.

TABLE I
512-TAP FILTER SIMULATION

Filter order	Constant value	1st coefficient value	Number of non-zero coefficients
512-tap	32	-1	14
	128	-2	18
	256	-2	18
	512	-4	22
	1024	-4	28

Since our FIR filter is implemented based on DA, multiplierless technique, therefore the number of adders and addition operations are crucial point in system computational complexity. The number of additions needed to accumulate N numbers is (N-1). Hence, after applying this algorithm, the number of addition operation is equal to the (number of non-zero coefficients -1).

2. CDMA Simulation

The CDMA communication system shown in Fig. 4 is used to verify functionality of the proposed algorithm when applied to 80-tap raised cosine pulse-shaping FIR filter. The simulation result is obtained in terms of error probability as a function of E_b/N_o and interference.

The filter is used in this simulation with its original set of coefficients Fig. 5 (a), and with its new set of coefficients i.e. after applying the proposed algorithm Fig. 5(b). The simulation is done for a number of processed symbols 10000 and the 80-tap pulse-shaping filter has a rolloff factor (α=0.22). Fig. 9 shows the result obtained for both cases.

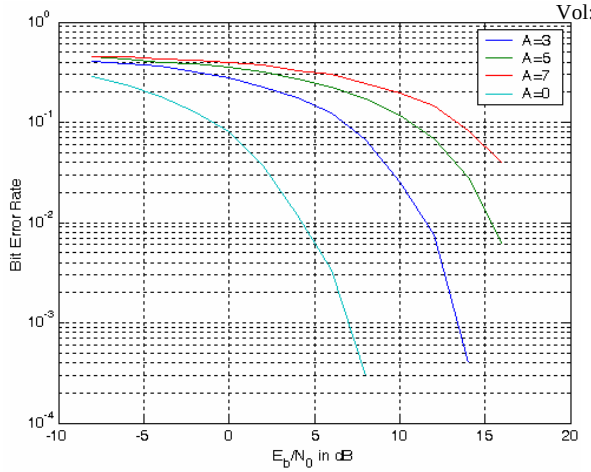

Fig. 9 (a) When pulse shaping filter with its original coefficients

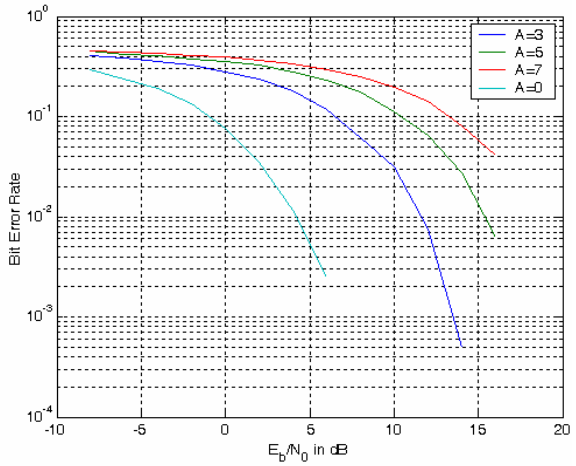

Fig. 9 (b) When pulse shaping filter is used after applying the algorithm

Table II shows the first half of the original filter coefficients i.e. from coefficient 0 to coefficient 40. On the other hand, column 3 of this table shows the new set of coefficients after applying the algorithm. Here we can see that the total number of non-zero coefficients in column 3 is 21 which mean that their total is 43. Hence, the number of additions needed after applying the algorithm is 42, whereas, we need 80 addition when dealing with the original set of coefficients. Therefore, we almost reduced the number of additions needed to the half. Column 3 also shows that the word length needed to represent the original coefficients value is higher than the word length to represent them after applying the modification algorithm. This has a substantial effect on the performance from the area, speed and power consumption point of views when performing the VLSI implementation of the designed filter.

The verilog hardware description language verilog HDL has been used to design the filter for both cases. The verilog code written is synthesized using the Xilinx Synthesis Technology (XST) and the sythesis report is obtained without any error. The ModelSim XE II/Starter 5.7g is used to simulate the verilog code in order to verify the functionality of the designed filter.

TABLE II
FILTER ORIGINAL AND MODIFIED COEFFICIENTS

Coefficient number	Original coefficient	New coefficient
1	0.02543691378952	-0.5
2	0.019828370858788	0
3	0.010470913741668	0
4	-0.001858070804008	0
5	-0.015867752788581	0
6	-0.029866753235948	0
7	-0.041941835678113	0
8	-0.050185743791461	0
9	-0.052949681951008	0
10	-0.049090535518244	0
11	-0.038180841068122	0
12	-0.020651248853743	0
13	0.00215916416357	0
14	0.028060281495628	0
15	0.054179880304451	0
16	0.07723487041437	0.125
17	0.093882608668519	0.125
18	0.101118718347263	0.125
19	0.096679604719143	0.125
20	0.079403887722045	0.125
21	0.049508002269793	0
22	0.008737432184037	0
23	-0.03963396106575	0
24	-0.090969258049985	-0.125
25	-0.139594060928143	-0.125
26	-0.179260276999505	-0.125
27	-0.203709791643149	-0.25
28	-0.207286736217459	-0.25
29	-0.185538936372068	-0.125
30	-0.135746967140597	-0.125
31	-0.057323524246516	0
32	0.047963666933783	0
33	0.175976346989898	0.125
34	0.320408918996059	0.375
35	0.473200159142286	0.5
36	0.625122157214771	0.625
37	0.766496724296835	0.75
38	0.887975644578479	0.875
39	0.981313446365383	1
40	1.040060731588741	1
41	1.060112699841736	1

Table III shows some of the results obtained after synthesizing and implementing the design.

TABLE III
XILINX SYNTHESIS REPORT

Parameter	Original coefficients	New coefficients
maximum frequency	66.227 MHz	77.375 MHz
number of slice flip flops	791	786
total equivalent gate count	12718	12468
number of occupied slices	832	826

Table III shows clearly that filter with its new coefficients is more optimized compared with its original coefficients. The difference in the maximum frequency reached by the design with its new coefficients is 11MHz over the case of its original coefficients. This shows the speed optimization parameter. The number of gate count needed for the design when using the new coefficients is less than the case when using the original set. This clearly shows that an optimization has been achieved in the total area used for the design.

Furthermore, the 80-tap square root raised cosine pulse shaping filter is used in simulating the CDMA system shown in Fig. 4. The number of symbols used in the simulation is also 10000 symbols. The error probability curves obtained with the filter for both cases. Fig. 10 (a) shows the result when the original coefficients are used whereas Fig. 10 (b) shows the result when the new set of coefficient is used.

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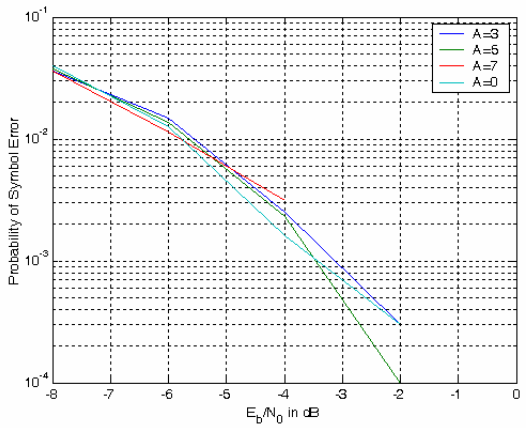

Fig. 10 (a) square root pulse shaping filter with its original coefficients

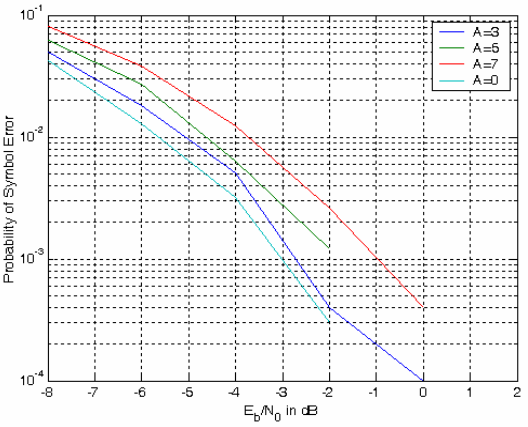

Fig. 10 (b) Error rate curves obtained with filter new coefficients

VI. CONCLUSION

This paper presents in detail an algorithm proposed for modifying the number and values of FIR filters coefficients. The algorithm target is to reduce the number of non-zero coefficients used to represent any FIR. An encouraging results have been achieved when obtaining the phase and frequency responses of the filters with the new set of coefficients. Although with this algorithm, the filter is represented with a number of nonzero coefficients half of the number of its original coefficients; the CDMA system performance, in terms of error probability, when using the filter with its new set of coefficients is the same as in the case when using the filter with its original coefficients.

The proposed algorithm is integrated with the DA technique i.e. one of the most famous multiplierless MAC unit implementation techniques in DSP. Together, they have been used to design and implement high-speed high-order digital pulse shaping FIR filters. The Verilog hardware description language is used to design the filter with its original set of coefficients and after applying the proposed algorithm. The ModelSim XE II/starter 5.7g simulator is used to simulate and prove the correctness of the designed filters output. The Xilinx Synthesis Technology (XST) is used to synthesize the Verilog HDL code and no errors were detected. Finally each of our designed filters have been successfully downloaded to Vertix-II f456 FPGA and a gain the expected filters output is achieved. Therefore, with this algorithm we have been able to design high order high speed FIR filters with half of the number of additions required for the original filter coefficients.

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