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Design of a Low Power Compensated 90nm RF Multiplier with Improved Isolation Characteristics for a Transmitted Reference Receiver Front End

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Abstract—In this paper, a double balanced radio frequency multiplier is presented which is customized for transmitted reference ultra wideband (UWB) receivers. The multiplier uses 90nm model parameters and exploits compensating transistors to provide controllable gain for a Gilbert core. After performing periodic and quasi-periodic non linear analyses the RF mixer (multiplier) achieves a voltage conversion gain of 16 dB and a DSB noise figure of 8.253 dB with very low power consumption. A high degree of LO to RF isolation (in the range of -94dB), RF to IF isolation (in the range of -95dB) and LO to IF isolation (in the range of -143dB) is expected for this design with an input-referred IP3 point of -1.93 dBm and an input referred 1 dB compression point of -10.67dBm. The amount of noise at the output is 7.7 nV/$\sqrt{Hz}$ when the LO input is driven by a 10dBm signal. The mixer manifests better results when compared with other reported multiplier circuits and its Zero-IF performance ensures its applicability as TR-UWB multipliers.

Keywords—UWB, Transmitted Reference, Controllable Gain, RF Mixer, Multiplier.

I. Introduction

THE scaling down of the supply voltage is proving to be the limiting factor in the effort to design efficient RF receiver front-ends in recent literature [1]. Despite that, much attention has been focused on RF mixers designed in sub-micron ranges as CMOS millimeter wave circuits are showing potential to achieve speed in the gigabit range for wireless applications [2]. The Ultra wideband (UWB) technology has been proposed as a promising alternative to wired interconnect systems which could use microwave mixers providing high data rates over short distances [3]. Different RF mixer topologies have been proposed in literature including a folded mixer exploiting reuse of current [4], a modified Gilbert cell mixer without tail transistors [5-6], a current reusing single balanced mixer [7], and a high gain CMOS mixer with low voltages [8], but none of them addresses the design requirements of UWB communication. So RF mixers cum multipliers which would complement the realization of UWB standards need to be explored to utilize the benefits that come with wideband systems. These advantages include high data rate, multiple access features, reduced fading because of frequency diversity, low cost and complexity and even lower power density [9-10].

With the passage of UWB pulse trains through the wireless channel, it may suffer from multi path fading, leading to the reception of replicas of the pulse with additional delay. As a consequence, including the equalizing filter at the start of the receiver to undo the channel effect becomes necessary. Channel estimation can be difficult in such situations because of the high degree of dispersion associated with the transmission. The synchronizing technique in use is also a dominant factor which determines the amount of extra overhead needed for the receiver. As the transmitted reference scheme exploits a self-synchronizing feature and avoids complicated channel estimation methods, it can provide a solution to these problems [11].

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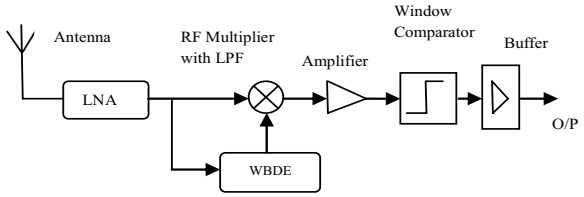

Fig. 1. The proposed transmitted reference UWB receiver architecture

A simplified diagram of the architecture of a transmitted reference ultra wideband receiver with proposed modifications is shown in figure 1. The receiver front-end starts after the receiving antenna and ends with the RF amplifier before the decision circuit (comparator section). It consists of a low noise amplifier (LNA) and a RF mixer cum multiplier which takes the output UWB pulses from the LNA and the delayed version of the same pulses as inputs. Design concerns for the LNA and the wideband delay element (WBDE) are explained in detail in [12-13]. This paper focuses on the design of the RF multiplier which could produce a response suitable to drive the threshold detection section in the back end of the TR-UWB receiver. The multiplier uses a Gilbert core and a passive matching network for input matching. Bleeding transistors are included for current compensation so that the gain provided by the mixer can be regulated. During simulation of the mixer with IBM 90nm CMOS technology the mixer is powered from a 1.2V bias supply. To characterize the multiplier, the RF and IF frequencies are set as 5.1 GHz and 100 MHz respectively. The input radio frequency can be adjusted within the range of 2-20GHz. The mixer achieves a peak conversion gain of 16dB which could be varied for $\sim$3dB by controlling the compensating transistors. The mixer core dissipates 8.19mW of power with the bias circuits with a noise figure of 8.253dB. Section II describes the operation of the RF multiplier. The

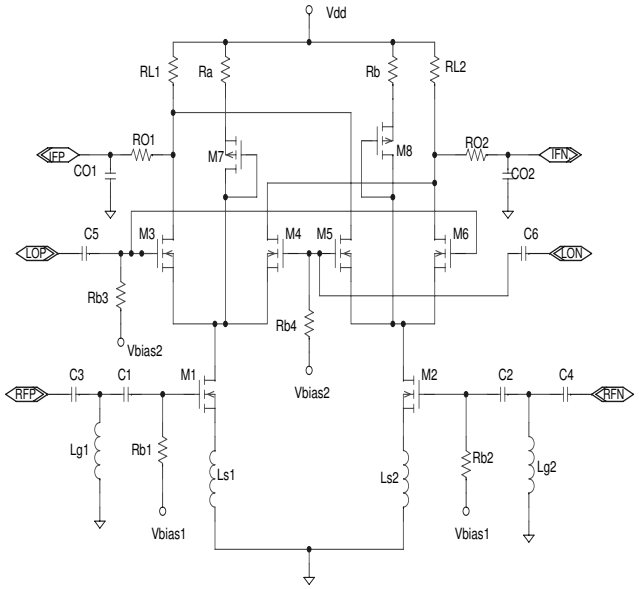

Fig. 2. Double balanced RF multiplier with compensating transistors and matching network

mixer is characterized in terms of microwave parameters in section III and sections IV is concerned with the zero-IF response of the multiplier. Finally, the performance of the circuit is summarized and compared with examples from published literature in section V.

II. FOUR QUADRANT COMPENSATED RF MULTIPLIER CIRCUIT

The RF multiplier in the TR-UWB receiver is supposed to have two inputs: the signal collected from the receiving antenna after passing through a LNA and a delayed version of the same signal. Figure 2 shows the designed double balanced four quadrant multiplier topology using the Gilbert core where the RF signal (received signal or the first input) is applied to the transistors M_1 and M_2 (20 μm/0.1μm) to perform a voltage to current conversion. These devices should be carefully biased for correct operation and therefore, signals with power considerably less than the 1dB compression point should be used as the RF signal. Performance is improved by adding degeneration inductors at the source terminals of M_1 and M_2 which serve the dual purpose of providing input matching for the RF input ports and controlling the gain and linearity of the multiplier. Transistors M_3 through M_6 (20 μm/0.1μm) perform a multiplication operation, multiplying the linear RF signal current collected from the drain terminals of M_1 and M_2 with the LO signal (delayed version of the received signal or the second input) applied across M_3 through M_6 providing the switching function. M_1 and M_2 produce positive or negative RF currents depending on the input. Then M_3 and M_5 switch between them to provide the RF signal or the inverted RF signal to the left hand load R_{L1}. M_4 and M_6 switch between them in a similar fashion for the right hand load R_{L2}. The two load resistors R_{L1} and R_{L2} ($\sim$1KΩ) perform a current to voltage transformation producing a differential output voltage at the output (IF) ports. The second input, at the LO ports, need to be large enough so that the switching transistors alternately commutate the tail current from one side of the mixer to the other at the switching frequency. A passive input matching 'T' network is added before the input transistor M_1 in the form of inductor L_{g1} and capacitors C_1 and C_3. Degeneration inductance L_{s1} adds to this purpose. A similar matching network is provided for the second input transistor M_2, formed by L_{g2}, C_2, L_{s2} and C_4. Capacitances C_5 and C_6 ($\sim 1pF$) provide input coupling for the driving LO signal. The gate and source inductors have inductances below 3nH. The bias circuits for the voltages V_{bias1} and V_{bias2} ($\sim 800mV$) are not shown in this circuit for simplicity. R_{b1} to R_{b4} are resistances around $10k\Omega$, which ensure that the bias voltages don't interfere with the input signals. Two passive low-pass filter sections are included with the load resistors to extract the output signal. As the circuit is designed with IBM 90 nm CMOS technology it is powered by a 1.2V dc bias power supply.

The sources of noise of the double balanced mixer structure are RF input trans-conductance, output load, switching transistors, current mirrors in the bias circuit and noise in the switching signal [14]. Providing controllable gain for the multiplier could be an effective way to negotiate with these factors. To control the mixer conversion gain and minimize the influence of flicker noise at the same time, compensating transistors (M_7 and M_8) are added to the four quadrant multiplier as shown in figure 2. With the introduction of these transistors the current through the switching transistors goes down and

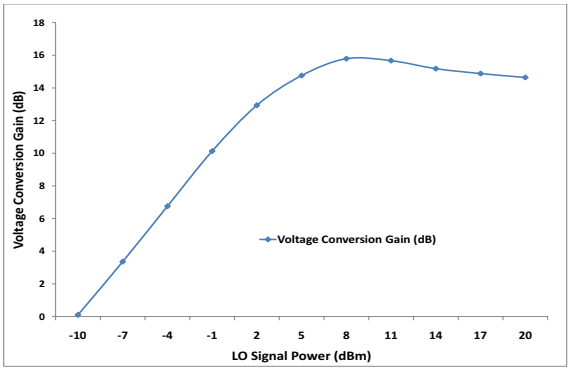

Fig. 3. Voltage conversion gain of the multiplier versus LO signal power

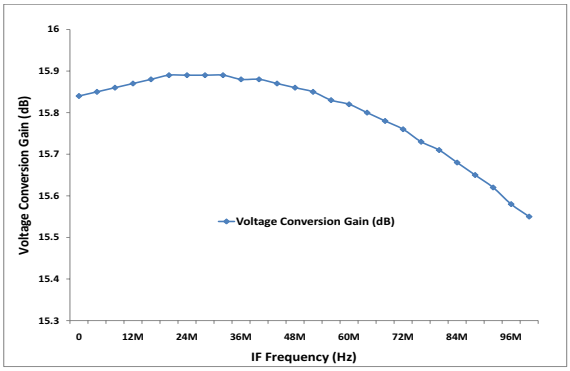

Fig. 4. Voltage conversion gain plotted against IF frequency

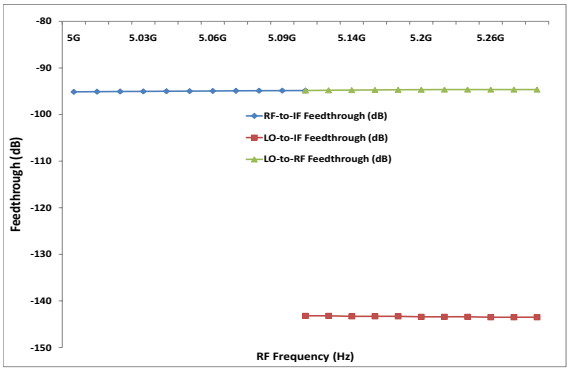

Fig. 5. Port-to-port isolation parameters for the RF multiplier

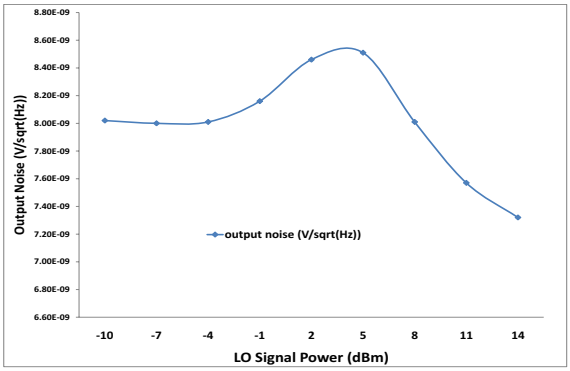

Fig. 7. Total amount of noise in $nV/\sqrt{Hz}$ at the mixer output

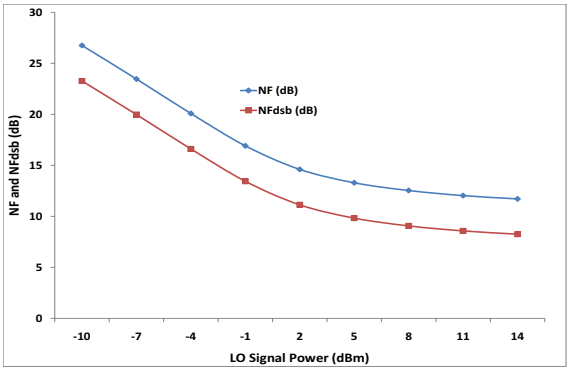

Fig. 6. Single and double sideband noise figure plotted against the driving signal power

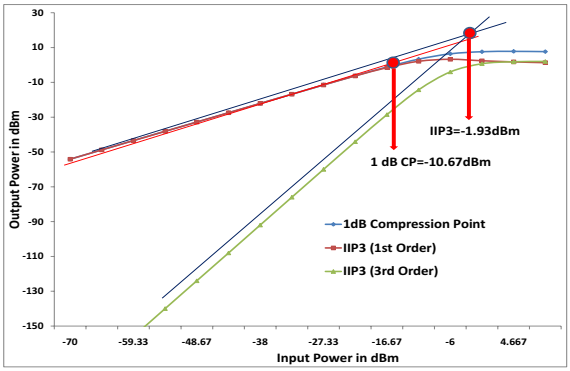

Fig. 8. Linear behaviour of the multiplier in terms of 1 dB CP and IIP3

the LO switches can operate faster, which reduces the $1/f$ noise contribution at the mixer output [15]. The compensating technique also allows the output load resistances (R_{L1} and R_{L2}) to have higher values, which lead to an increased gain for the multiplier. At the same time, the overall current through the input transistors (M_1 and M_2) is increased without manipulating the current through the switching transistors, which results in a regulated conversion gain for the mixer.

III. CHARACTERIZATION OF THE MULTIPLIER CIRCUIT

To ensure the applicability of the double balanced mixer as a TR-UWB multiplier it is important to characterize the circuit in terms of parameters like RF to IF conversion gain, amount of noise at the output, noise figure, input impedance matching, isolation between the three ports, linearity and power requirement for the design. To obtain these parameters a number of analyses including periodic and quasi-periodic noise analysis, swept and quasi-periodic AC analysis, and periodic or quasi-periodic steady state analysis are performed on Cadence Spectre platform.

A. Voltage Conversion Gain

The voltage conversion gain (CG) is the ratio of the rms voltages of the IF and the RF signals. It is plotted against the driving local oscillator signal power which is varied from -10 to 20 dBm. During that sweep the voltage conversion gain from RF to IF node is shown in figure 3. It is manifested that the maximum conversion gain achieved is about 16 dB and this happens when the strength of P_{LO} is about 10dBm. Periodic steady state with swept periodic AC analysis is performed to plot the conversion gain against the IF frequency. Figure 4 shows the conversion gain varying within the range 15.5-15.9dB with a peak gain of 15.9dB.

B. Port to Port Isolation

Four types of isolation parameters between the three ports (RF, LO and IF) are calculated for the designed multiplier. Among them RF-to-LO feed through represents the down converted RF signal at the LO port which should only be present at the output of the circuit. This parameter has a constant value of -6.4kdB at the possible IF frequencies. Figure 5 shows the other three isolation parameters where RF-to-IF feed through represents the RF signal present at the IF port without any down conversion. LO-to-IF feed signal

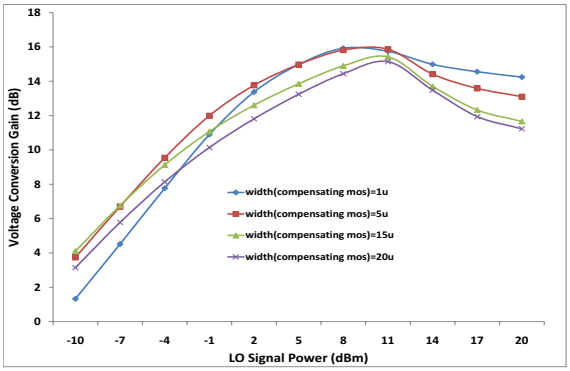

Fig. 9. Gain control by adjusting compensating transistors

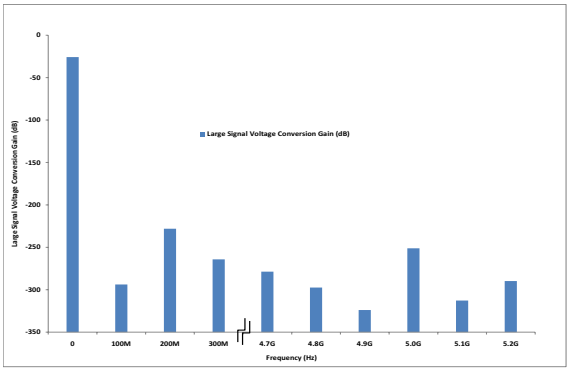

Fig. 10. Large signal power (voltage) conversion gain of the mixer

indicates the influence of the switching signal on the down converted output. LO-to-RF feed through is a measure of the isolation between the two ports. As the isolation parameters have values below -50dB it can be said that the mixer provides a high degree of isolation between the three ports.

C. Noise Figure (NF) and Amount of Noise

For the proposed design it is calculated that when the input RF frequency is 5.1GHz, NF is about 11.05dB and NFdsb is around 8.399dB. When NF and NFdsb are plotted for specific local oscillator signal powers the graphs look like the ones shown in figure 6. As the LO signal power is raised to 10dBm (when conversion gain is maximum), the NF gets about 12.03dB and NFdsb is around 8.253dB. The total output noise, measured in a unit of $V/\sqrt{Hz}$, is plotted in figure 7 which shows that the amount of output noise is 7.7 $nV/\sqrt{Hz}$ for this specified oscillator power.

D. Linearity

When a RF circuit satisfies small signal conditions the output power increases linearly with increase of the input signal. But as the circuits shift toward large signal operation the devices start to behave in a non linear manner. The 1dB

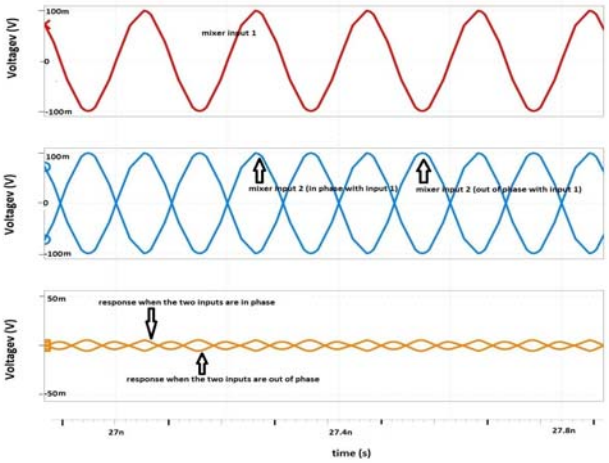

Fig. 11. Zero IF response when mixer inputs have two phase shifted combinations

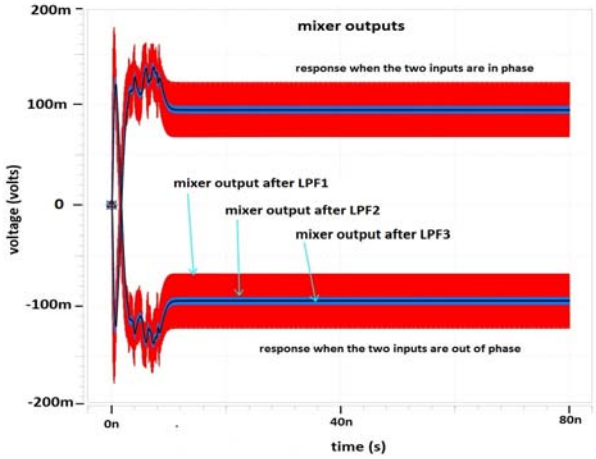

Fig. 12. Outputs of the mixer after different stages of the LPF

compression point and the IP3 (3rd order inter-modulation product) provide a measure of this nonlinearity. Figure 8 is representing these points when they referred to the input port. It can be inferred from the graph that the input referred 1 dB compression point is located at -10.67dBm and the IIP3 point is around -1.93917dBm.

E. Gain control by compensating transistor

Figure 9 shows how the conversion gain of the RF multiplier can be manipulated by changing the dimensions of the compensating transistors. As the width of the bleeding transistors M_7 and M_8 are varied from 1 to 20μm as gain is plotted against driving signal power. The peak conversion gain moves between 14.8 to 16dB which indicates that the multiplier gain can be made a controllable parameter by virtue of the compensating transistors. By setting the transistor width at 20μm a maximum forward gain of 16.1dB can be achieved. All the other parameters remain approximately the same after the addition of the extra transistors with only a slight degradation of linearity.

F. Power Spectrum

Figure 10 presents the large signal power (voltage) conversion gain of the major frequency components (-25dB at DC) for the proposed design. As these bars are indicative of the power spectrum of the mixer, summation of harmonics and sidebands can provide a good estimate of the total power consumption.

IV. ZERO-IF RESPONSE FROM THE RF MULTIPLIER

The zero IF response (when only DC components will be present at the IF output) is important for a RF multiplier to ensure that it is suitable for use in a TR-UWB scheme when the transmission is employing BPSK modulation to establish communication. To obtain the zero IF response, the mixer inputs (RF and LO) are provided with two combinations which have the same frequency and amplitude but differ only in phase. So for the first combination RF and LO have the same amplitude , frequency (5GHz) and phase, and for the second combination, the same amplitude, frequency and a 180^o phase shift. To obtain a satisfactory multiplier response, when RF and LO are in phase the mixer must provide a positive voltage of sufficient magnitude, and when RF and LO are out of phase the mixer must supply a negative response. Figure 11 shows the zero IF response for the RF mixer (with compensating transistors and single stage output low pass filter). The mixer output, having high ripple content and 10mV magnitude, is not deemed satisfactory. So to optimize the response, the amplitudes of RF and LO inputs (when they are in phase) are varied and a three stage output filter is used to extract responses from the mixer. Figure 12 shows the signal at different stages of the output low pass filter when RF and LO have sufficient input voltages and the same two input combinations as mentioned before. Finally, the complete multiplier response of the RF mixer is manifested in figure 13, magnified in the time domain. Figure 14 shows the output from the proposed RF multiplier when the two inputs are an UWB baseband pulse stream and a delayed version of the same stream (following the principle of the transmitted reference ultra wideband communication). The data pulses of the first input are correlated with the reference pulses of the delayed input and the bipolar nature of the mixer response suggests that a suitable comparator section will be able to detect information imparted in the received UWB signal from this design.

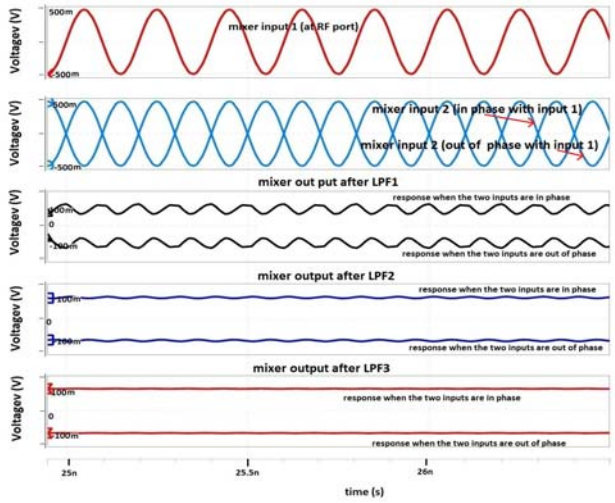

Fig. 13. Complete zero IF response from the multiplier

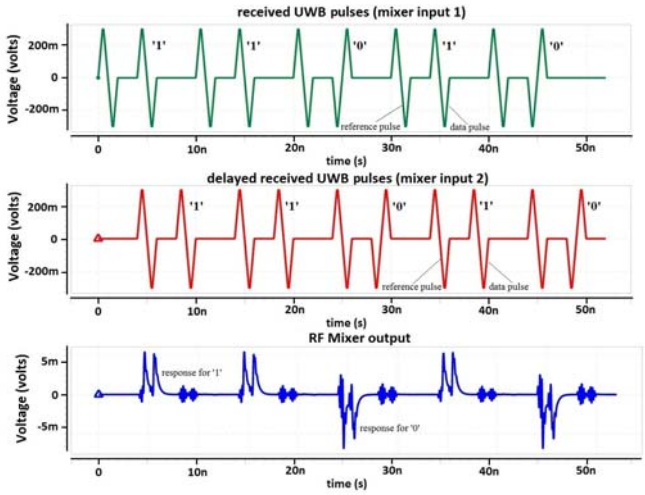

Fig. 14. RF mixer response for input UWB signals

V. PERFORMANCE OF THE PROPOSED MULTIPLIER

The simulated performance of the double balanced four quadrant multiplier is documented in table 1 in terms of indices like technology, voltage conversion gain, feed-through parameters, power spectrum components, frequency range, power dissipation, Sparameters, noise figure, and linearity. The performance of the design with a blocking signal (large interfering signal) suggeststhat the gain or noise figure is not degraded unless the strength of the interfering signal exceeds -25dBm. In table 2 and 3 theparameters of the RF multiplier is compared with examples of other published analog mixers [1, 16-31]. The results show that theproposed architecture achieve better figures, especially in terms of conversion gain and port to port isolation.

VI. CONCLUSION

This paper deals with the transmitted reference UWB architecture while focusing on the design of a microwave multiplier suitable for this standard. Satisfying the criteria of a zero-IF multiplier the proposed circuit produces desirable response for input UWB pulse trains. The RF mixer achieves features of gain control, high degree of forward gain ($\sim 16dB$), linear behaviour up to -1.93dBm, 8dB double sideband noise figure, feed through parameters lower than -50dB for any two of the three multiplier ports and low power consumption for the multiplier core (8.19mW). The performance of the multiplier is better than published reports of its counterparts and it would complete the realization of a TR-UWB receiver front end.

TABLE I
SYNOPSIS OF PERFORMANCE OF THE RF MULTIPLIER

Performance metrics	Proposed RF mixer	Performance metrics	Proposed RF mixer
Technology	90nm CMOS	S23 (dB)	~ -240
Vol. Conversion Gain (CG,dB)	16	NF (dB)	11.05
RF-to-LO Feedthrough (dB)	$-6.4k$	$NF_{dsb}(dB)$	8.399
RF-to-IF Feedthrough (dB)	~ -95	Output Noise ($nV/\sqrt{Hz}$)	7.7
LO-to-IF Feedthrough (dB)	~ -143	1dB Compression Point (dB_m)	-10.67
LO-to-RF Feedthrough (dB)	~ -94	IIP3 (dBm)	-1.93917
DC Power Spectrum (dB)	-25	NF with Blocking Signal	$\sim 12dB$ upto $P_{RF} = -25dBm$
Peak S21 (dB)	15.89	NF_{dsb} with Blocking Signal	$\sim 9dB$ upto $P_{RF} = -25dBm$
S13 (dB)	~ -250	Supply Voltage (V)	1.2
RF Frequency (Hz)	5.1G	Power Spectrum @ (100M$\sim$10GHz)	< -250
IF Frequency (Hz)	100M	Power Dissipation (mW)	8.1873

TABLE II
COMPARISON OF THE PROPOSED RF MIXER WITH REPORTED CIRCUITS

Reference	Technology(CMOS)	Supply Voltage(V)	Max. Conv. Gain(dB)	RF Freq.(GHz)	IF Freq.(MHz)	NF(dB)	NF_{dsb}(dB)
This Work	90nm	1.2	16	5.1	100	11.05	8.399
[1]	0.13μm	1.2	11.6	5.5	500	14.2	–
[16]	0.18μm	0.6	11.2	6.5-8	20	8-10	–
[17]	0.18μm	1.8	6.6	5.15-5.35	–	9.0	–
[18]	0.18μm	1.8	7.3	–	–	–	14.2
[19]	GaAs PHEMT	5.5	14.32	2	100	9.6	–
[20]	0.13μm	–	9.5	5.2	50	–	13.5
[21]	0.18μm	1.2	11	4.2	55	14.5	–
[22]	0.18μm	2	14	1-30	10	14.3-17	–
[23]	0.13μm	3.3	8-14	9-50	–	16.4	–
[24]	0.13μm	1.5	11	2.4	5	18.5	–
[25]	0.13μm	1.5	17	1-5.5	–	–	4.2
[26]	0.18μm	–	11	2.45-5.2	500	10-13	–
[27]	0.18μm	1.8	7.5	5.8	1-100	–	7.6-10.9
[28]	0.18μm	1.8	8.5(power)	2-11	50	16-19	–
[29]	0.18μm	1.8	12.5	22-26	50	10.5-14	–
[30]	0.18μm	2.75	6	12.1	100	18	15
[31]	InGaP/GaAs HBT	5	17.3	30	10	15.1	–

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TABLE III
COMPARISON OF THE PROPOSED RF MIXER WITH REPORTED CIRCUITS (CONTD.)

Reference	1dB CP (dBm)[1]	IIP3 (dBm)	Power (mW)	RF-IF isolation(dB)	LO-IF isolation(dB)	LO-RF isolation(dB)
This Work	-10.67	-1.94	8.19	95	143	94
[1]	-6	2	4.2	–	–	–
[16]	-21	–	3.75	–	–	–
[17]	–	-5.4	5.4	50	45	34
[18]	–	-9.1	10.8	–	–	–
[19]	-4	–	–	58.98	–	63.54
[20]	–	7.6	21.3	–	–	–
[21]	-15	-11.8	3.14	–	–	–
[22]	–	-2∼-4	40	–	22.4	37.5
[23]	–	-0.2∼4	97	>40	>40	>20
[24]	–	2.7	–	–	–	–
[25]	-10.5	0.85	34	–	–	>83
[26]	-17∼-16	-4.9∼5.2	10	–	–	–
[27]	–	-5	8.1	–	–	–
[28]	-10	0	25.7	–	–	–
[29]	-11	–	16.2	–	–	>35
[30]	-12	-2	113	>30	>68	–
[31]	-15	-8	179	–	–	–

[1] Compression Point

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