World Academy of Science, Engineering and Technology
International Journal of Electronics and Communication Engineering
Vol:1, No:2, 2007

NOISE OPTIMIZATION TECHNIQUES FOR 1V 1GHz CMOS LOW-NOISE AMPLIFIERS DESIGN

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Abstract-**A 1V, 1GHz low noise amplifier (LNA) has been designed and simulated using Spectre simulator in a standard TSMC 0.18um CMOS technology. With low power and noise optimization techniques, the amplifier provides a gain of 24 dB, a noise figure of only 1.2 dB, power dissipation of 14 mW from a 1 V power supply.**

I. INTRODUCTION

CMOS transistors have been consistently scaled to smaller feature sizes and continue to reduced towards sub-0.1um lengths. However,as the channel length decreases, so does the gate oxide thickness, dictating a decrease in the supply voltage. Commonly a low noise amplifier (LNA) is a key component in RF front-end receiver which poses a challenge in terms of meeting high gain, low noise figure and linearity requirement at low power supply(such as 1V). The primary role of the LNA is to lower the overall noise figure of the entire RF front-end, noise optimization is considered as one of the most critical steps in the LNA design procedure.

The noise figure (NF) of LNA should not exceed a 3 dB, assuming it has a gain more than 10 dB [1]. The design of LNA is full of trade-offs between optimum gain, lowest noise figure, high linearity and low power consumption. Cascode topology is one of the most popular topology used for CMOS LNA design, which provides high gain, low noise, but it is not suitable for low power supply. The consideration for noise optimization of LNA is illustrated in Section II. The proposed LNA design suitable for 1V power supply is analyzed in Section III. Spectre simulation results and a comparison with other reported LNAs are presented in Section IV.

II. NOISE FIGURE AND OPTIMIZATION

A. Noise Figure

An LNA determines the performance of the communication systems. It needs higher linearity and sufficient gain to overcome the next stage noise but not to overload. A system noise factor is defined as:

$$F_{total} = F_1 + \frac{F_1 - 1}{G_1} + \frac{F_2 - 1}{G_1 G_2} + \dots \quad (1)$$

where F_n (n=1,2,3,....) is the noise factor of each stage, G_n(n=1,2,3,...)is the gain of each stage. In our circumstances, F_1 is the noise factor of the LNA and G_1 is the gain of the LNA which implies that higher gain and lower noise of LNA will lower the total noise of the system. Noise figure represents how much the given system degrades the signal-to-noise ratio, which is defined as:

$$NF = 10\log\frac{TotalOutputNoisePower}{OutputNoisePowerSourduetoImpedance} \quad (2)$$

CMOS LNA design provides high level of integration at low cost but it is a big challenge to achieve low noise performance because of the noisy nature of MOS device. The dominant noise source in MOS devices is channel noise:[2]

$$\overline{i_{nd}^2} = 4kT\gamma g_{d0} \quad (3)$$

Where g_{do} is the zero-bias drain conductance of the device. γ is a bias dependent factor which, for long channel device satisfies $\frac{2}{3} \le \gamma \le 1$,but for short channel devices can be as large as two or three, depending on bias condition. Another source of noise in MOS devices is the noise generated by the distributed gate resistance. This noise can be modeled by a series resistance in the gate circuit and an accompanying with noise generator, which results in:

$$\overline{v_{rg}^2} = 4kT\delta r_g \Delta f \quad (4)$$

where δ is the coefficient of gate noise, normally equal to 4/3 for long channel devices and r_g is the gate resistance. The gate resistance can be minimized through interdigitation without the need of increased power dissipation, thus it is rendered insignificant [2]. If the sizes of the MOS transistors are carefully chosen, the optimum ω_t which is simply a ratio of g_m/C_{gs} can be obtained. Therefore, the minimum noise figure can be achieved according to [3]:

$$F_{min} = 1 + \frac{w}{w_t}\sqrt{\gamma\delta\zeta(1-|c|^2)} \quad (5)$$

If δ were zero, the minimum noise figure would be 0dB[4].

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B. Noise Optimization Techniques

A. Classical Noise Matching

In this technique, the LNA is designed for minimum NF by adding a matching circuit between the source and input of the amplifier [4]. By using this technique in Fig.1, at the input port in order to provide a 50 ohms impedence matching. There are several disadvantages in using this technique: The extra resistor contributes its own thermal noise to the output, which equals the noise contribution of the source resistance. This means that there would be an immediate 3dB increase in the noise figure. Furthermore, the input signal is attenuated by the resistor termination before reaching the active device, which cuases a redcution in gain.Thus,one cannot obtain both input matching and minimum NF simultaneously. The large noise penalty due to the use of resistive termination is the main limitation of the classical noise matching.

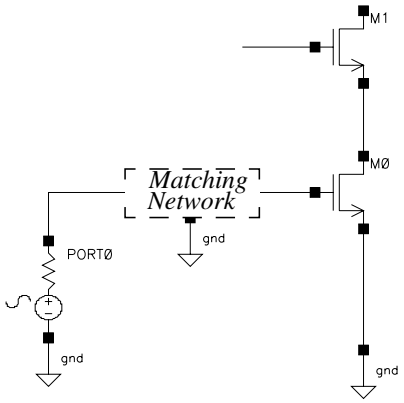


Figure 1. Schematic of a casecode LNA topology used to apply classical Noise Matching technique.

B. Simultaneous Noise and Input matching

To achieve lower noise and higher gain, the casecode with the inductor degeneration topology is employed and shown in figure2.

Neglecting the gate drain capacitances, the input impedance of the LNA shown in Figure1 is:

$$Z_{in} = \frac{g_{mL_S}}{C_{gs}} + \frac{1}{C_{gs}S} + S(L_s + L_g) + R_g \qquad (6)$$

where g_m and C_{gs} are the transconductance and the gate-to-source capacitance of the input device M_1 respectively. L_g and L_s are the gate and source inductors and R_g is the effective gate resistance of M_1 given by $R_g = R_0/(3n^2L)$ where R_0 is the sheet resistance of the gate polysilicon,W and L are the gate width and length of the transister M_1 respectively and n is the number of fingers [2].

At the resonant operating frequency(w_0), the input matching requires that:

$$Z_{in} = R_s = \omega_t L_s \qquad (7)$$

The C_{gs} source degeneration inductance L_s is chosen together with W_t to provide the desired input resistance Rs, the real term can be made equal to 50 ohm without the existence of a real noisy resistor. Then, the input impedence of the LNA is matched to source resistance R_s when the above condition is met.

III. PROPOSED DESIGN APPROACH

For LNA design, inductive source degeneration is used to achieve good input matching without adding thermal noise introduced by real resistor. The cascode topology shown in Figure 2 is a popular configuration for LNA design but it is not

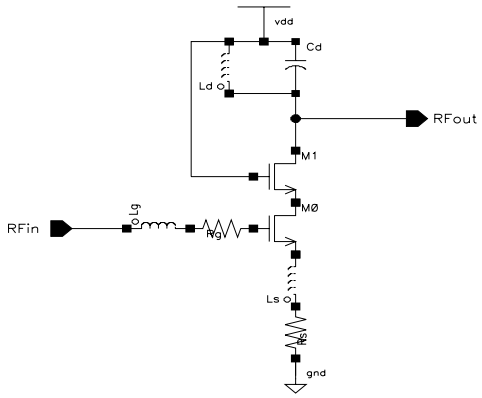


Figure 2. Schematic of a casecode topology with inductively degenerated .

suitable for low voltage supply applications.

The proposed topology is shown in Figure 3, which works

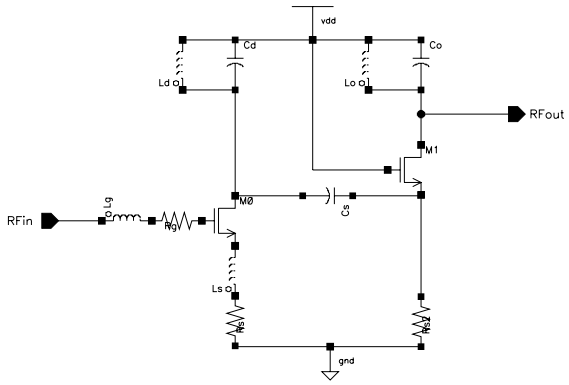


Figure 3. Common-source common-gate topology

for low power supply applications such as 1V, Inductive source degeneration is also used to achieve good input matching and reduce noise figure. The first stage is inductively degenerated common-source amplifier formed by transistor M_0. Followed by a common-gate configurated transistor M_1. The value of LC tank of M_0 is carefully chosen to achieve a resonance frequency of 1GHz and is required to have a much higher impedance than that of the input impedance looked at the source of

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M_1. It provides a DC bias current path and a high impedance branch to force the RF signal to flow into the source of M_1 through a big DC coupling capacitance C_s .

The input impedence of the LC tank ($L_{d,}C_d$) is

$$Z_d = R_d + \frac{\omega^2 L_d^2}{R_d} \approx \frac{\omega^2 L_d^2}{R_d} = R_d Q_d^2 \quad (8)$$

Then,

$$g_{m1} » \frac{1}{R_d Q^2 d} \quad (9)$$

where R_d and Q_d are the resistance and the quality factor associated with the inductor L_d.

The input impedence at the source of the common gate transistor M_1 is:

$$R_i = \frac{1}{g_{m1} + g_{mb1}} \approx \frac{1}{g_{m2}} \quad (10)$$

where g_{mb} is the bulk transconductance.

IV. Simulation Results

The complete circuit is shown in Figure 4. The LNA first

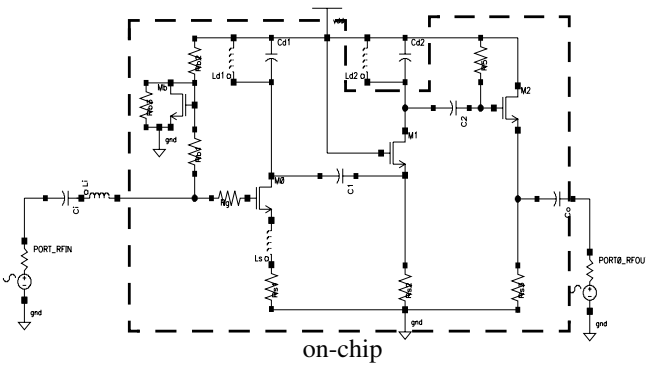


Figure 4. Complete schematic of proposed common-soure, common-gate LNA

stage of the LNA M_0 transister is inductively degenerated is a common-source amplifier followed by M_1 configured as common-gate device. M_b sets the dc bias for M_0. M_2 is configured as the buffer stage for LNA output matching. C_1 between M_0 and M_1 is blocking DC and provides ac path to let RF signal flow into the source of common-gate transistor M_1. In our case, it is designed to be 20 pF. Inductors which are smaller than 5 nH are placed on chip otherwise, they are off-chip. As shown in Figure 4 only the framed components are on-chip.

The proposed circuit was simulated using Spectre simulator in 0.18um CMOS process. Figure 5 shows a forward power gain (S_{21}) of 24 dB at 1 GHz. After noise optimization a low

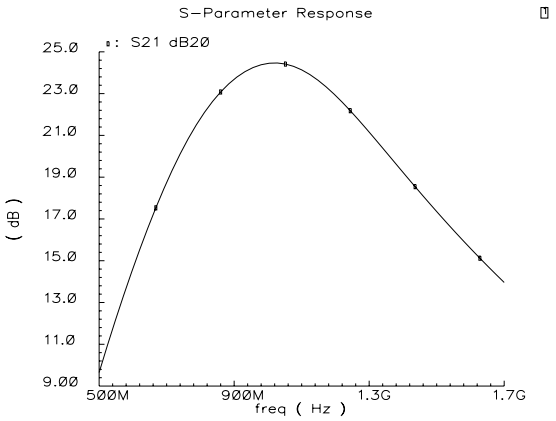


Figure 5. Power gain of proposed LNA

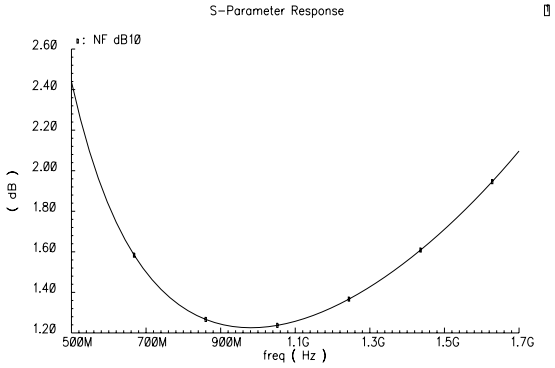


Figure 6. Noise figure of proposed LNA

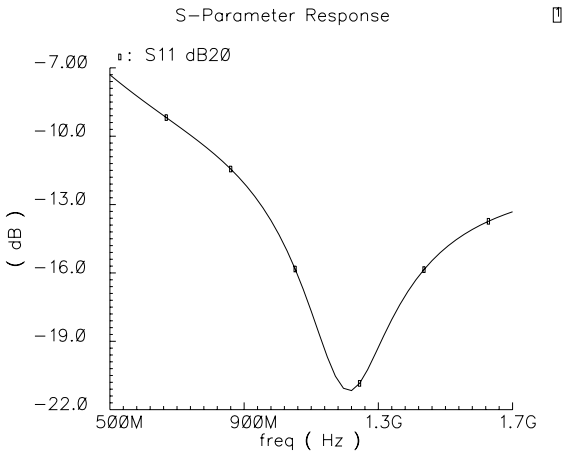


Figure 7. S11 of proposed LNA

noise figure of 1.2 dB at 1 GHz is achieved and shown in Figure 6.

The S-parameters of the LNA are illustrated in Figure 7 and Figure 8 respectively. The S_{11} shows a good input match of -21dB. The S_{22} shows a good output match with the output buffer which achieves -15dB.The S_{12} at 1GHz is -74.9 dB.The

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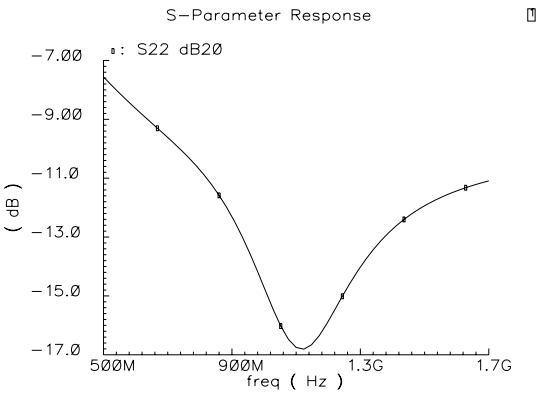


Figure 8. S22 of proposed LNA

IIP3 simulation result of the LNA is shown in Figure 9. A two-

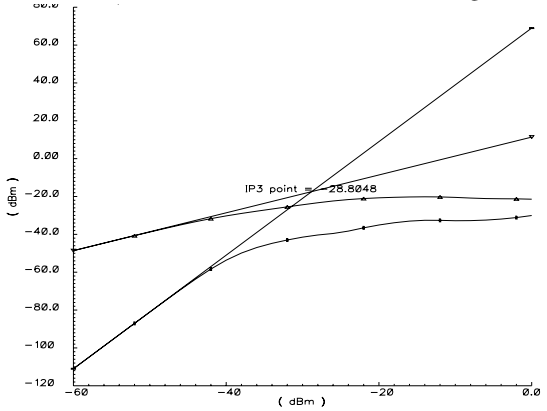


Figure 9. IIp3 simulation of the proposed LNA

tone signal which are chosen close to each other has been applied to the input port. The input-referred third-order intercept points (IIP3) is -29dBm.

The layout of the LNA is shown in Figure 9. The chip area is

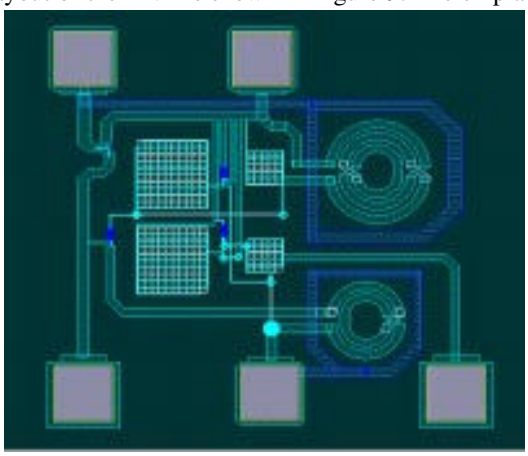


Figure 10. Layout of the proposed LNA

1mm x 1mm. This work is placed alongside with other recent reported LNA in Table 1. It shows that with the noise optimization techniques the proposed LNA achieves a much lower noise figure than other LNAs.

Table 1: Comparison of Various Recent Reported LNAs

f_0	[5]	[6]	[7]	[8]	[1]	This Work
Freq.(G Hz)	0.9	0.9	0.9	1	1	1
NF(dB)	2	2.5	6	3.5	2.7	1.2
S_{21}(dB)	17.5	9	17	22	12.2	24
$IIP_{3(dBm}$	-6	-4.7	-14	12	-21	-29
Power(mw)	N/A	10	78	27	17	14
Tech(um)	.35	0.5	0.8	1.0	0.5	0.18

V. CONCLUSIONS

In this paper, a new CMOS low noise amplifier using common-source inductive source degeneration followed by common-gate configurations is proposed. The proposed topology is suitable for low power supply application and works good at 1 V voltage supply. Spectre simulation using TSMC 0.18µm CMOS technology shows a low noise figure of 1.2 dB, high power gain (S_{21}) of 24 dB and low power consumption of 14 mW from 1 V power supply.

ACKNOWLEDGEMENT

The research was supported by a grant awarded to Dr. R. Raut by the Natural Science and Research Council (NSERC) of Canada

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