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Charge-Pump with a Regulated Cascode Circuit for Reducing Current Mismatch in PLLs

Jae Hyung Noh, and Hang Geun Jeong

***Abstract*—**The charge-pump circuit is an important component in a phase-locked loop (PLL). The charge-pump converts Up and Down signals from the phase/frequency detector (PFD) into current. A conventional CMOS charge-pump circuit consists of two switched current sources that pump charge into or out of the loop filter according to two logical inputs. The mismatch between the charging current and the discharging current causes phase offset and reference spurs in a PLL. We propose a new charge-pump circuit to reduce the current mismatch by using a regulated cascode circuit. The proposed charge-pump circuit is designed and simulated by spectre with TSMC 0.18-μm 1.8-V CMOS technology.

***Keywords*—**Phase-locked loop (PLL), charge-pump, phase/frequency detector (PFD), regulated cascode.

I. Introduction

PHASE-locked loops (PLLs) are widely used in frequency synthesizers for wireless communication systems [1]. A PLL based on a charge-pump is preferred over other types because it has a wide capture range and zero static phase offset. In practice, nonidealities of the charge-pump degrade the performance of the entire loop. One of noidealities of the charge-pump is the current mismatch. The mismatch between the charging current and the discharging current causes a phase offset and reference spurs in PLL [2]. Fig. 1 shows the conceptual model of the charge-pump. It consists of two switched current sources driving a capacitor. In a conventional charge-pump, usually Up and Down switches are made of a PMOS transistor and an NMOS transistor, respectively. The current mismatch is caused by the charge-pump current variation due to changes of the drain-source voltage of the PMOS and NMOS transistors.

In this paper, we propose a new charge-pump with a regulated cascode circuit for reducing current mismatch to increase the output resistance of the charge-pump.

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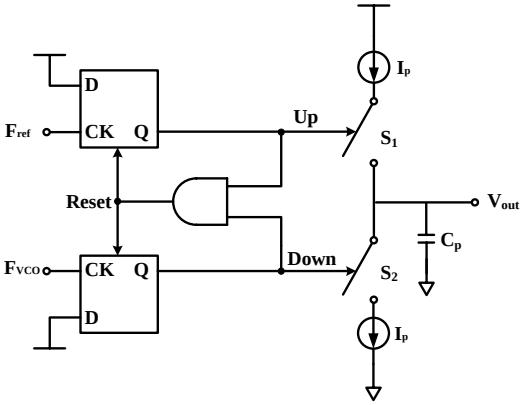


Fig. 1 The conceptual model of the charge-pump

II. Proposed Charge-Pump

Fig. 2 shows the charge-pump with the current steering switches. The advantage of this structure is that switching time is improved by using the current steering switches [3]. However, the charge-pump current changes as a function of V_{out} due to channel-length modulation effect. Therefore we apply a regulated cascode circuit to the output of the charge-pump to reduce the channel length modulation effect.

Fig. 3 shows the generalized regulated cascode circuit consisting of a simple cascode M_1 and M_2 and a differential amplifier [4]. The basic idea is to use a feedback amplifier to keep the drain-source voltage across M_1 as stable as possible, irrespective of the output voltage. The output resistance of the regulated cascode circuit is given by

$$R_{out} \approx g_{m2} r_{o2} r_{o1} (1 + A). \quad (3)$$

The proposed charge-pump using the regulated cascode circuit is shown in Fig. 4. When the UP signal is active, the differential amplifier with NMOS input pair regulates V_{DSP4} at V_{bn}. The bias voltage V_{bn} is fixed 1.5 V to increase the output voltage range. Similarly when the DN signal is active, the differential amplifier with PMOS input pair regulates V_{DSN9} at V_{bp}. The bias voltage V_{bp} fixed 0.3 V to increase the output voltage ranges. And we added capacitors to the output of differential amplifiers to ensure the feedback loop stability. Fig. 5 shows differential amplifiers with source-follower level shifters for use in a regulated cascode circuit. Owing to the increased output resistance and the extended output voltage ranges of the charge-pump, the mismatch between the Up

current and the Down current with the wide output voltage ranges can be reduced.

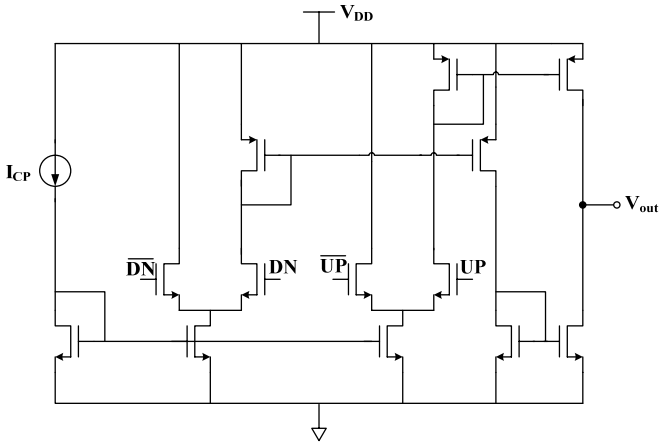


Fig. 2 The charge-pump with current steering switches

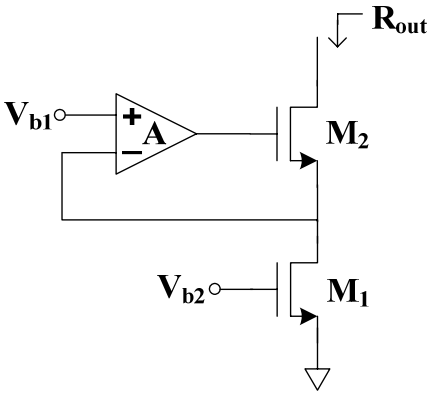


Fig. 3 The regulated cascode circuit

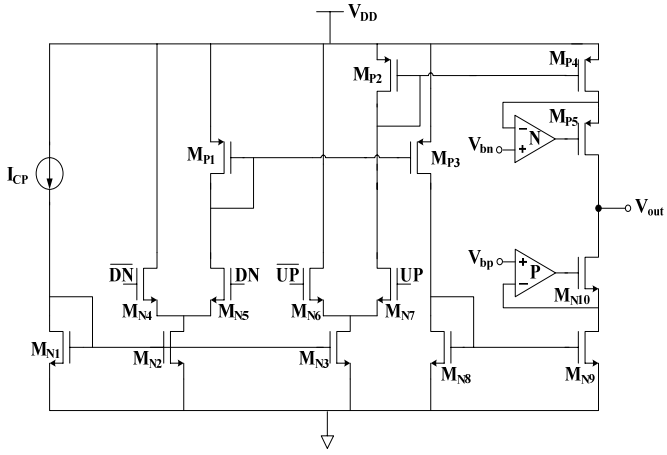


Fig. 4 The proposed charge-pump

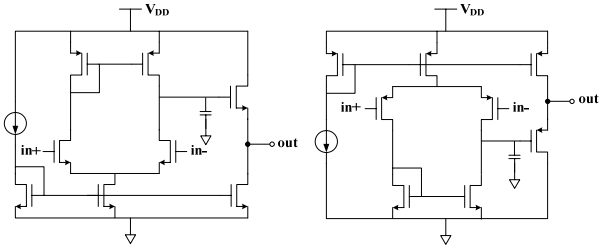


Fig. 5 Differential amplifiers with source-follower level shifters for use in a regulated cascode circuit

III. Simulation Results

The proposed charge-pump and the conventional charge-pump without a regulated cascode circuit are simulated by spectre with TSMC 0.18-µm 1.8-V CMOS technology. Fig. 6 shows the variation of the Up/Down current without a regulated cascode circuit as the charge-pump output voltage varies 0 to 1.8 V. The maximum variation of the Up/Down current over the charge-pump output voltage range of 0.4~1.4 V is approximately 24 µA. Fig. 7 shows the variation of the Up/Down current with a regulated cascode circuit as the charge-pump output voltage varies 0 to 1.8 V. The maximum variation of the Up/Down current over the charge-pump output voltage range of 0.4~1.4 V is approximately 720 nA.

Fig. 8(a) and 8(b) shows the transient Up/Down current waveforms for lock state without the compensation capacitor and with the compensation capacitor on the output of the added differential amplifiers. As observed from the figures, with the compensation capacitor, the Up/Down current doesn't show overshoot and ringing.

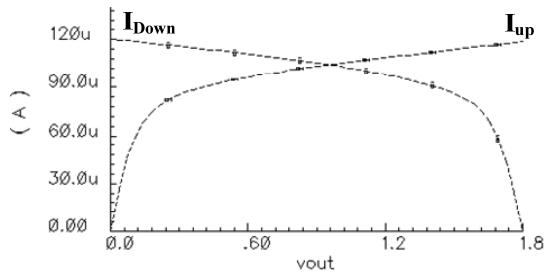


Fig. 6 The current matching characteristic of the charge-pump without a regulated cascode circuit

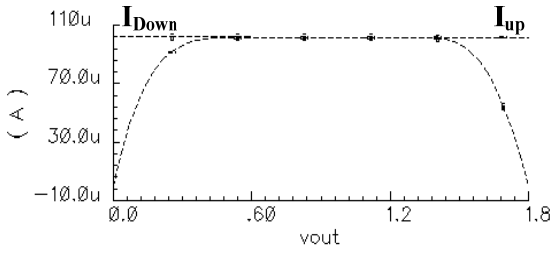
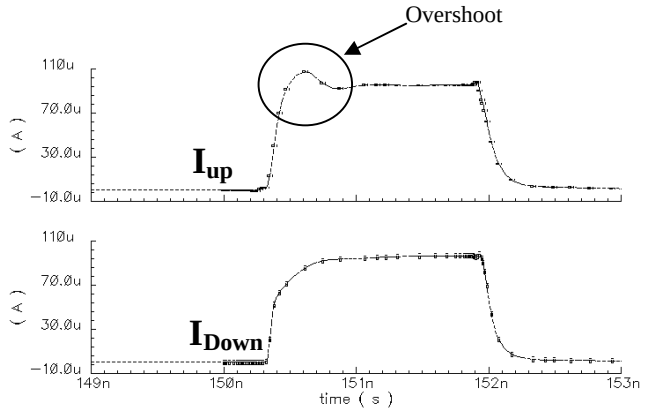
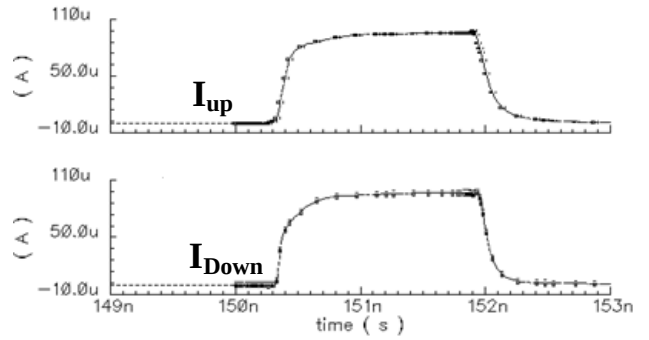


Fig. 7 The current matching characteristic of the charge-pump with a regulated cascode circuit



(a)



(b)

Fig. 8 The transient Up/Down current waveform for lock state (a) without a compensation capacitor. (b) with a compensation capacitor

IV. Conclusion

We proposed a new charge-pump circuit, designed for good current matching characteristics in PLLs. The proposed charge-pump is simulated by spectre with TSMC 0.18-µm 1.8-V CMOS technology. The proposed charge-pump using a regulated cascode circuit to increase the output resistance improved the current matching characteristics. It shows the maximum variation of the Up and Down current over the charge-pump output voltage range of 0.4~1.4 V is less than 1 %. Also as the output voltage range of the charge-pump is increased, the proposed charge-pump is suitable for low supply voltage operation.

References

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