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Modeling and Analysis of SVPWM Based Dynamic Voltage Restorer

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***Abstract*—**In this paper the modeling and analysis of Space Vector Pulse Width Modulation (SVPWM) based Dynamic Voltage Restorer (DVR) using PSCAD/EMTDC software will be presented in details. The simulation includes full modeling of the SVPWM technique used to control the DVR inverter. A test power system composed of three phase voltage source, sag generator, DVR and three phase resistive load is used to demonstrate restoration capability of the DVR. The simulation results of the presented DVR proved excellent voltage sag mitigation to protect sensitive loads.

***Keywords*—**Dynamic voltage restorer, power quality, simulation and modeling, voltage sag.

I. Introduction

THE last decades has seen a revolution in the end user equipment highly sensitive to poor quality power supply. Due to the increasing complexity in the power system, voltage sags are now becoming one of the most significant power quality problems and deserves attention. Voltage sag is defined as a decline ranging from 0.1 to 0.9 p.u. in the RMS value of the voltage at the supply frequency for a time period of 0.5 cycles to 1 minute [1]. A power quality study done recently indicates that 92 % of all disturbances in a power system are caused by voltage sags [2]. The interest in voltage sags is mainly due to the problems they cause on several types of equipment like adjustable-speed drives, process-control equipment, and computers. Generally voltage sags can be divided into two main categories; the first is voltage sag due to faults and the second is voltage sag due to starting of heavy loads. Of course the first type is much more difficult to mitigate because it happens very fast and so it needs faster response.

Dynamic Voltage Restorer (DVR) is one of the most important mitigation equipment for voltage sag in both medium voltage and distribution levels. The [3-4] is based on the idea of using DC storage and voltage source converter (VSC) to inject series voltage for sag mitigation. Recent improvements in fast switching power devices have led to an increased interest in VSC with Pulse Width Modulation (PWM) techniques [5]. Space Vector Pulse Width Modulation (SVPWM) technique is widely adopted due to its simple and effective digital implementation [6]. The theory of SVPWM with several modes of operation is presented in [7-8]. SVPWM technique introduces reduced commutation losses, lower harmonics and better utilization of the DC voltage compared to other PWM techniques.

Modeling of DVR is extensively tackled under MATLAB [9]. This paper introduces the simulation of a power system with a sag generator of the first type including DVR using PSCAD/EMTDC [10]. The restoration capability of the DVR is one of the most with most important issues to evaluate a DVR. Different sag levels will be applied to the simulated system to test the restoration capability of the DVR.

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II. Structure of DVR

The DVR is composed of power circuit and control circuit to implement the control algorithm. As shown in Fig. 1, the power circuit of DVR is composed of; DC energy storage device, inverter, filter, injection transformer and bypass switch.

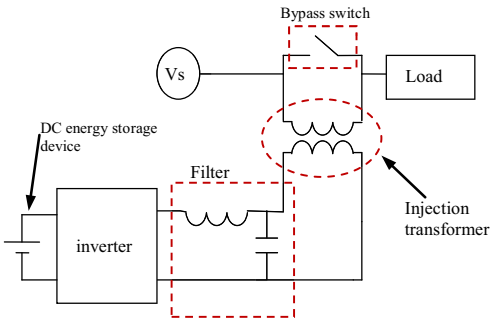

Fig. 1 The structure of DVR

The controller of DVR has two main functions; to detect the sag occurrence and to derive the parameters of the control signal (magnitude, frequency, phase shift, etc…) that has to be injected by the DVR. Accordingly, proper firing pulses for the inverter are produced; proper injected voltage is consequently generated by the switches in the power circuit. In some sophisticated dynamic voltage restorers, further functions are handled by the controller like selective harmonics elimination. To construct the control circuit of the DVR, a suitable control technique has to be adopted and accordingly implemented as shown in Fig. 2.

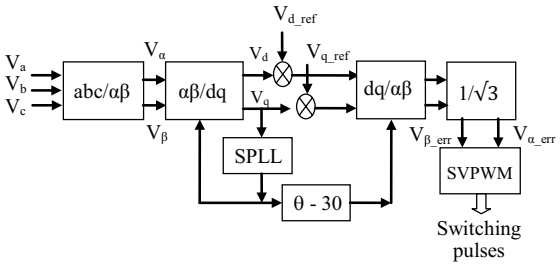

Fig. 2 The control algorithm

The transformation matrix from the supply voltages to the stationary orthogonal α-β frame is;

$$\begin{bmatrix} V\alpha \\ V\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \cdot \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} Va \\ Vb \\ Vc \end{bmatrix} \quad (1)$$

The transformation matrix between α-β frame and the synchronous rotating d-q frame is;

$$\begin{bmatrix} \mathrm{Vd} \\ \mathrm{Vq} \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} V\alpha \\ V\beta \end{bmatrix} \quad (2)$$

A Software Phase Locked Loop (SPLL) is needed to track the reference angle of the supply voltage. After calculating the error signal, it is transformed back into α-β frame to calculate the inverter firing pulses using SVPWM technique. The 30^{o} angle shift and the division by √3 are to compensate the delta/open connection of the injection transformers.

III. Theory of SVPWM

Space Vector Pulse Width Modulation (SVPWM) control strategy is a novel control strategy which used to manipulate inverters based on the space voltage or current switching of converter. Any three phase system can be represented by a vector rotating with the synchronous speed with respect to stationary orthogonal α-β axes where the α-axis coincides the V_a axis. The magnitude of this vector is constant and equal to the victoria sum of the three phase voltages at any instant. This vector can be projected on the α-β to give V_α and V_β as shown in Fig. 3.

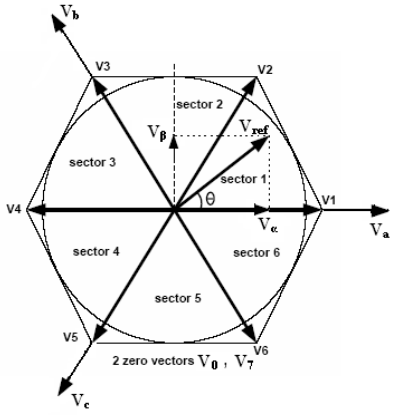

Fig. 3 Realization of SVPWM for two-level inverter

For a two level converter using DC source V_{dc}, there are only eight possible switching states, which yield eight vectors (V_0 to V_7) given in table 1.

TABLE I
SWITCHING STATES VECTORS FOR TWO-LEVEL INVERTER

State(abc)	Vector	magnitude	angle
000	V_0	0	0
100	V_1	$\sqrt{\frac{2}{3}}V_{dc}$	0
110	V_2		60
010	V_3		120
011	V_4		180
001	V_5		240
101	V_6		300
111	V_7	0	0

These vectors split the space into six sectors as shown in Fig. 3. If the reference (desired output) voltages are

$$V_a = V_m \cos \omega t \quad (3)$$

$$V_b = V_m \cos(\omega t - 120) \quad (4)$$

$$V_c = V_m \cos(\omega t + 120) \quad (5)$$

Then the reference vector will be:

$$\vec{\mathrm{V}}_{\mathrm{ref}} = \sqrt{\frac{3}{2}} \mathrm{V_m} e^{\mathrm{j}\theta} \quad (6)$$

Where $\theta = \omega t$

This reference vector can be composed by the two adjacent vectors V_N and $_{VN+1}$ beside the two null vectors V_0 and V_7 in such a way to minimize the switching losses. To determine the time durations, the concept of equal volt-second area is used [9];

$$\vec{\mathrm{V}}_{\mathrm{ref}} . \mathrm{T_s} = \vec{\mathrm{V}}_{\mathrm{N}} . \mathrm{T_N} + \vec{\mathrm{V}}_{\mathrm{N+1}} . \mathrm{T_{N+1}} \quad (7)$$

Using (7) the time of each firing state can be calculated to determine the firing signals.

IV. Simulation of SVPWM based DVR

PSCAD and SIMULINK are more convenient for the simulation and analysis of the power electronics and control provided with DVR system. PSCAD/EMTDC is selected to perform the simulation in spite of being less user-friendly compared to SIMULINK as it yields more accurate results that match practical system performance especially when concerning transients. The complication of using PSCAD originates from the need to build every block from scratch using the basic available library blocks. Nevertheless, it allows more capability to control every detail in the simulation project. Power circuit simulation is shown in Fig. 4 where the components of the circuit are illustrated as follow,

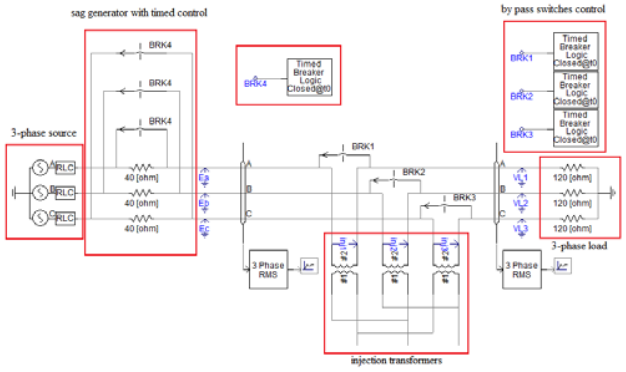

Fig. 4 Simulation of the power circuit of the DVR

Three-phase source: A ready unit in the master library of PSCAD is adopted; its parameters are adjusted to give line-to-line voltage "V_{LL}" of 110 V (rms) behind impedance per phase of 1.3 Ω.

Sag generator: Three resistors connected in series with the source voltage are by-passed via a three phase switch. When the switch is on, the source voltage will be applied to the load. When the switch is off the load voltage will be under sag condition. The value of the sag can be controlled by changing the series resistors' values. The (on/off) state of the sag switch is controlled though a timed breaker logic module adjusted to start the fault (sag) after 0.2 sec from the start of the simulation. The timed breaker module is adjusted to clear the sag after another time of 0.2 sec. the values of the fault resistors are adjusted to obtain different sag levels.

By-pass switches control: In the present simulation, by-pass switches (BRK1, BRK2 and BRK3) are closed during normal operation and opened only during the sag duration.

Injection transformers: The injection transformers are used to inject a series voltage with the supply voltage during the sag to maintain the load voltage within the desired range.

The Load: The load used in the system under simulation is a three-phase resistive load. The values of resistors are adjusted to make a load current of 0.53 A.

The simulation of the control circuit is shown in Fig. 5 where the components of the circuit will be illustrated in the following sub-sections.

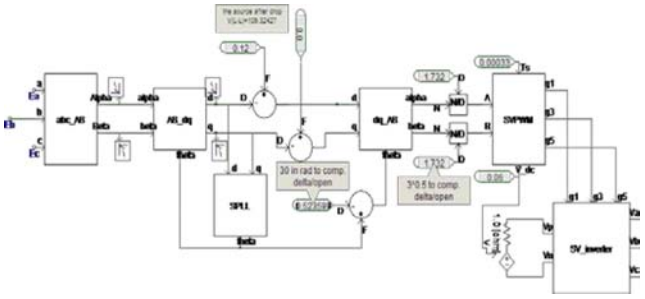

Fig. 5 Simulation of the control circuit of the DVR

Transformation of "abc: to "α-β": The phase voltages (V_a, V_b and V_c) are measured and used as inputs to the transformation block to get the stationary orthogonal components (α-β). The transformation is based on (1).

Transformation of "α-β" to "d-q": The "d-q" components are the synchronous orthogonal components. The transformation from "alpha beta" to "d q" needs also the angle of the rotating vector which is achieved from the SPLL (Software Phase Locked Loop) block. The transformation is based on (2).

The "d-q" reference values: The values of "d" and "q" components are subtracted from the "d" and "q" reference values respectively. The "q" reference value is set to zero, while the "d" reference value is set to 120 V; higher than the 110 V nominal "d" component of the load voltage. This difference is essential to compensate for the losses and allow load voltage retrieval during sag up to 100% of its nominal value.

SVPWM: The error signal in "d-q" components form is transformed to the "α-β" form SVPWM block receives the error signal, the switching period "Ts" and the value of the DC battery V_{dc}. The firing signals of the inverter switches are generated accordingly.

The SVPWM PSCAD/EMTDC model could be split into 4 stages:

Stage (1): Calculation of the magnitude (mag), the angle inside each sector (phi) and the sector number (N) using (8) as shown in Fig. 6.

$$\emptyset = \theta - (N\text{-}1).60 \tag{8}$$

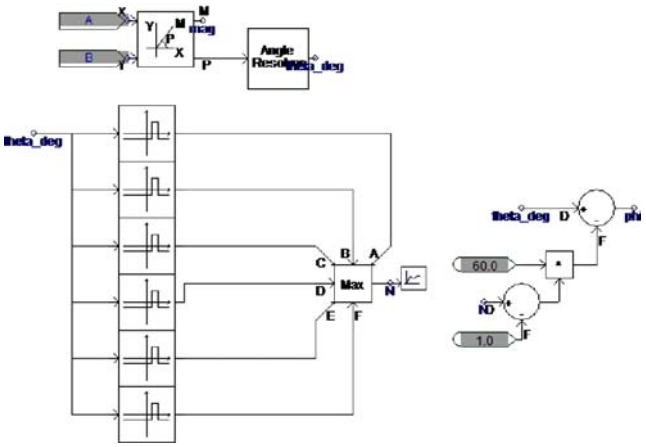

Fig. 6 Calculation of the magnitude, angle and sector number

Stage (2): Calculation of duty ratios and switching time using (10) and (11) as shown in Fig. 7.

$$T_N = T_s \frac{2}{\sqrt{3}} \frac{V_{ref}}{V_N} \sin(60 - \phi) \tag{9}$$

$$T_{N+1} = T_s \frac{2}{\sqrt{3}} \frac{V_{ref}}{V_{N+1}} \sin\phi \tag{10}$$

The time left for the null vectors T_o will be

$$T_o = T_s - (T_N + T_{N+1}) \quad (11)$$

Where V_N and V_{N+1} are two adjacent vectors from the six vectors in the space. T_N and T_{N+1} are the on times for each switching vector (pattern) V_N and V_{N+1} respectively.

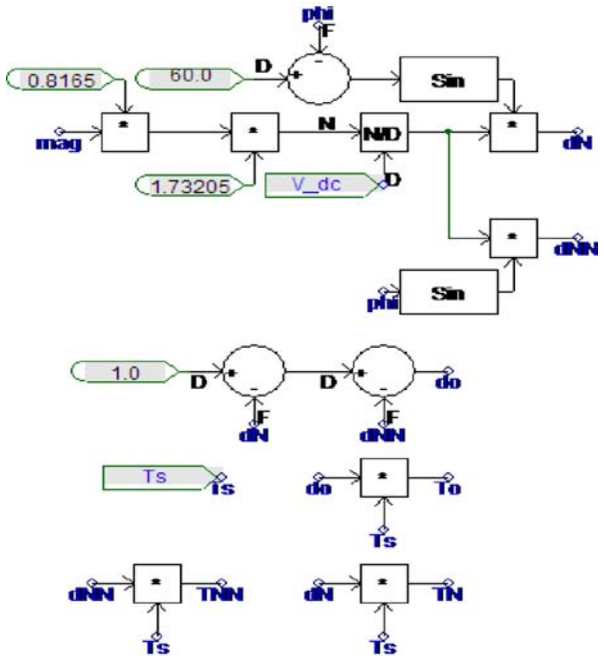

Fig. 7 Simulation of the duty ratios and switching time calculavvtions

Stage (3): Developing a time signal (T) that starts from zero each switching period (T_s), and preparing the logic constants (1 or 0) that identify the sector (n_1 to n_6) as shown in Fig. 8.

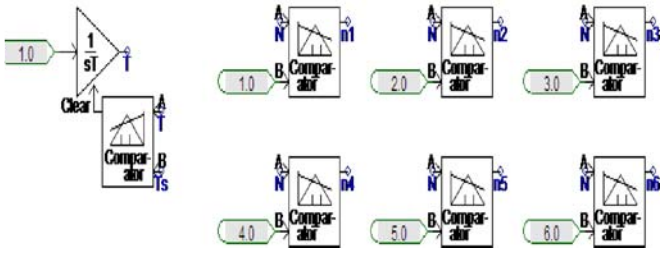

Fig. 8 Simulation Developing a time signal

Stage (4): Constructing the firing signal by using two comparators, one to start the signal (from 0 to 1) and the other to end the signal (from 1 to 0). The simulation of the firing signal constructor for the upper switch of the first leg is shown in Fig. 9.

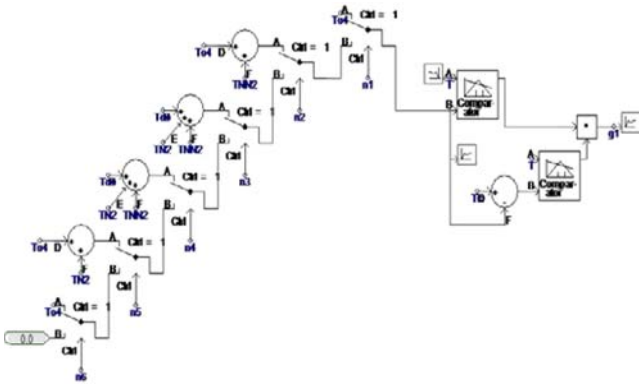

Fig. 9 Construction of the firing signal

V. Simulation Results

The sag generator has been adjusted to generate sag values of 20%, 30%, and 40%. The DC source for the inverter has been choosen to mitigate up to 40% sag. Since the system and the sag are balanced, only one phase of the three phases will be presented. The results both in rms and instantaneous have been recorded as follows;

At 20% sag: The load and the injected DVR voltages before and after the DVR activation are shown in Fig. 10, 11, and 12.

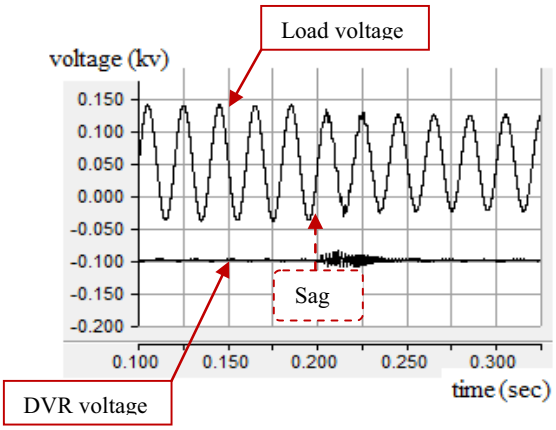

Fig. 10 Load and DVR voltages 20% sag while DVR is deactivated

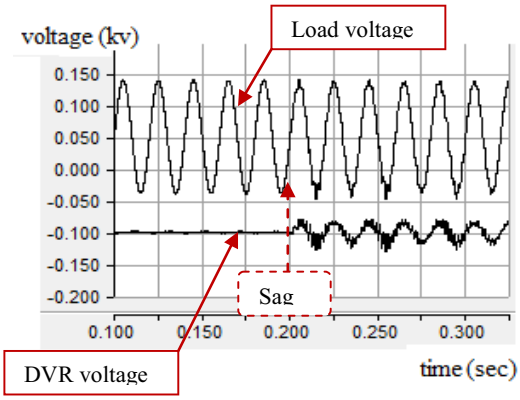

Fig. 11 Load and DVR voltages with 20% sag while DVR is activated

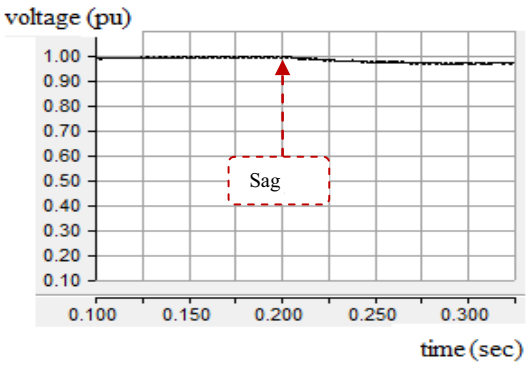

Fig. 12 Peak load voltage with 20% sag while DVR is activated

At 30% sag: The load and the injected DVR voltages before and after the DVR activation are shown in Fig. 13, 14, and 15.

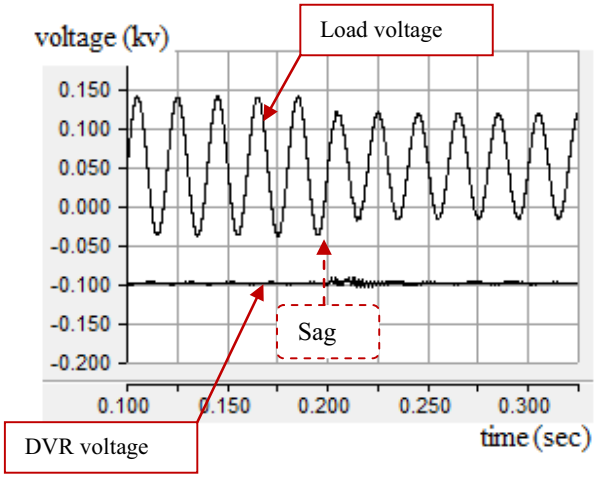

Fig. 13 Load and DVR voltages 30% sag while DVR is deactivated

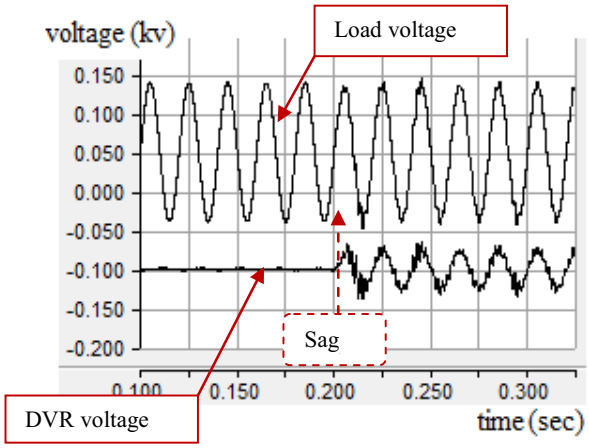

Fig. 14 Load and DVR voltages 30% sag while DVR is activated

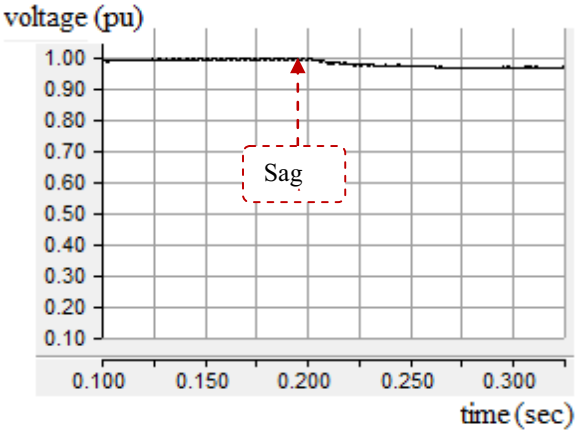

Fig. 15 Peak load voltage with 30% sag while DVR is activated

At 40% sag: The load and the injected DVR voltages before and after the DVR activation are shown in Fig. 16, 17, and 18.

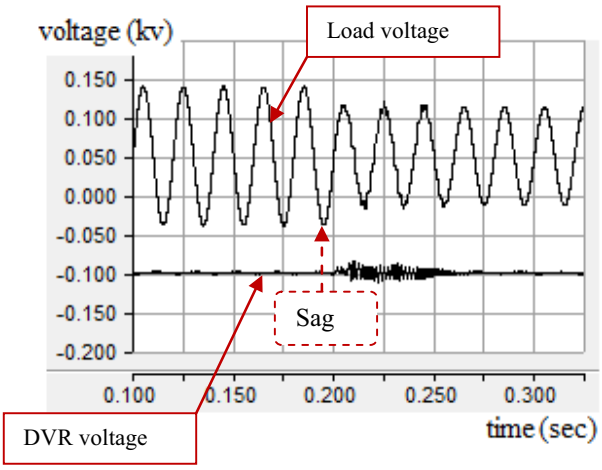

Fig. 16 Load and DVR voltages 40% sag while DVR is deactivated

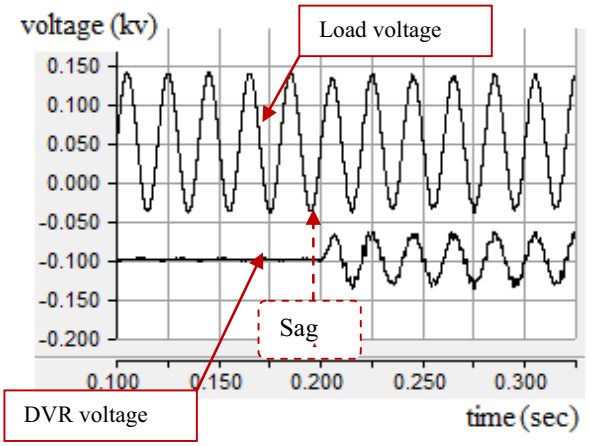

Fig. 17 Load and DVR voltages with 40% sag while DVR is activated

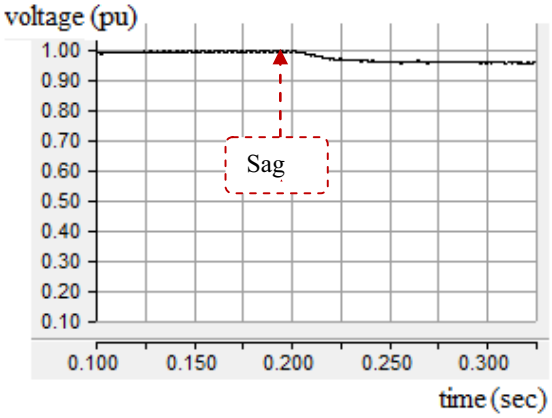

Fig. 18 Peak load voltage with 40% sag while DVR is activated

It is shown from Fig. 10 to Fig. 18 that the injected voltage is equal to zero when the DVR is deactivated due to the inclusion of the shunt by-pass switches in the model. With the DVR activated it has the capability to restore the load voltage to its original value even with voltage sag up to the predesigned sag limit (in this case 40%). This is performed by series injection of the appropriate voltage magnitude and phase. It is also noticed that the DVR efficiency in voltage sag restoration, measured by the deviation in the magnitude of load voltage before and after sag, decreases with the increase of the sag level.

VI. Conclusion

In this paper a detailed model describing the operation of dynamic voltage restorer was built in PSCAD/EMTDC environment. The simulation model facilitates analyzing the performance of DVR during different operating conditions. The DVR effectiveness in voltage sags compensation up to the designed sag level makes it an interesting power quality device compared to other custom power devices. The results of the PSCAD/EMTDC simulation also verify the presented control algorithm based on SVPWM technique to generate the necessary switching pulses for the DVR inverter in order to generate the proper injected voltage for voltage sag mitigating.

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