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Coding based Synchronization Algorithm for Secondary Synchronization Channel in WCDMA

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***Abstract*—**A new code synchronization algorithm is proposed in this paper for the secondary cell-search stage in wideband CDMA systems. Rather than using the Cyclically Permutable (CP) code in the Secondary Synchronization Channel (S-SCH) to simultaneously determine the frame boundary and scrambling code group, the new synchronization algorithm implements the same function with less system complexity and less Mean Acquisition Time (MAT). The Secondary Synchronization Code (SSC) is redesigned by splitting into two sub-sequences. We treat the information of scrambling code group as data bits and use simple time diversity BCH coding for further reliability. It avoids involved and time-costly Reed-Solomon (RS) code computations and comparisons. Analysis and simulation results show that the Synchronization Error Rate (SER) yielded by the new algorithm in Rayleigh fading channels is close to that of the conventional algorithm in the standard. This new synchronization algorithm reduces system complexities, shortens the average cell-search time and can be implemented in the slot-based cell-search pipeline. By taking antenna diversity and pipelining correlation processes, the new algorithm also shows its flexible application in multiple antenna systems.

***Keywords*—**WCDMA cell-search, synchronization algorithm, secondary synchronization channel, antenna diversity.

I. Introduction

WIDEBAND CDMA is a typical asynchronous CDMA system of current 3G standards. In WCDMA systems, each cell site is assigned a unique long scrambling code in the downlink for identification. The process that a mobile station tries to identify and synchronize to a cell is called cell search. Cell search is critical to achieving code and time synchronization. The main process of achieving cell search is divided into three stages followed by code verification, tracking and carrier frequency adjustment: 1) slot synchronization, 2) frame synchronization and code group identification, 3) primary scrambling code identification [1]-[2]. During the first stage, the slot boundaries are determined. The two tasks of the second stage are to find the frame boundaries and to identify the code group of the cell. During the third stage of the cell search, the exact primary scrambling code is identified by using Common Pilot Channel (CPICH). The overall synchronization processes are implemented by pipelining. When mobile stations are switched on, going through handover or during idle and active modes, they have to synchronize to the scrambling code used in the best serving base station. The cell-search in the asynchronous CDMA systems is a time-costly process when compared with other inter-cell synchronous systems such as CDMA2000 in which all base stations and mobile stations are time-aligned by GPS timing service.

A lot of efforts were made to reduce the cell search time. First, to avoid searching all possible scrambling codes, a large number of scrambling codes (512 primary scrambling codes) are divided into 64 groups [3]. The code groups are determined before the exact scrambling code is found out. Second, the three-stage cell search process was introduced in [4]. The algorithm in the second stage was further improved as the Cyclically Permutable (CP) code was introduced in [5]-[6]. By using (15, 3) Reed-Solomon (R-S) codes, no codeword is a cyclic shift of another one. Hence, once the scrambling code group has been found, the frame boundary is determined simultaneously by identifying the starting phase of the RS code sequence. Simulations and experiments were made to improve the performance in [7]. In [8], the cell-search performance over Rayleigh fading channels was numerically evaluated. The improvement and optimization of cell-search algorithm were made in [3]-[10]. However, all previous works above focused on the default or improved algorithm based on the CP code. In this case, a great number of R-S codeword computations and comparisons are required, which leads to high system complexity and long processing time [10].

To further simplify the system complexity and shorten the acquisition time as compared to the conventional techniques, in this paper, we propose new Secondary Synchronization Code (SSC) structure and acquisition method. Since antenna diversity is justified to be able to improve performances of code acquisition and cell search process [11]-[14], the new acquisition scheme is also designed for flexible application in multiple antenna systems.

This paper is organized as follows. Section II describes and compares the channel structure and acquisition methods of the conventional algorithm and new algorithm. In section III, the new acquisition scheme and system function are introduced. Numerical analysis is given in section IV. Section V shows the

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simulation results both in AWGN channel and Rayleigh fading channels. Antenna diversity applications of the new algorithm are proposed in section VI. Section VII compares the acquisition performances of all schemes in three aspects. Finally, conclusion is drawn in section VIII.

II. System Description

In the W-CDMA standard [15]-[17], the synchronization channel (SCH) is used in the initial cell search procedure. It contains two sub-channels: the Primary Synchronization Channel (P-SCH) and the Secondary Synchronization Channel (S-SCH). Both P-SCH and S-SCH are transmitted only during the first 256 chips (1/10 of the slot length) of each slot. In P-SCH, the Primary Synchronization Code (PSC) of length 256 chips is transmitted once every slot to mark the slot boundary. All base stations have the same PSC in the system.

A. Conventional S-SCH synchronization

In WCDMA systems, to reduce the cell-search time, 512 primary scrambling codes are divided into 64 groups. The functionality of the S-SCH is to determine the scrambling code group as well as the frame boundary.

In the S-SCH of the conventional algorithm, a radio frame of length 10ms consists of 15 slots. Each slot contains a Secondary Synchronization Code (SSC) sequence in the first 256 chips. As shown in Fig. 1, the 256-chip SSC sequences are mapped into one of 16 different symbols. Hence, in a frame, 15 slots with 15 concatenated SSC symbols form a vector. This vector is a kind of special Reed-Solomon (RS) codeword. 64 different codewords are utilized to identify 64 scrambling code groups. In order to determine the frame boundary at the same time, these codewords are chosen to have unique code phase shift and any phase shift of a codeword is different from all phase shifts of all other codewords. In this case, once the codeword is obtained, the frame boundary can be determined based on the correct starting phase of the codeword.

In the cell search pipeline, after the slot synchronization is achieved in the first stage, the received SSC sequences correlate with 16 local SSC matched filters, the largest correlation result is found out in every slot as the correct SSC symbol. During a frame time, correlation is taken in 15 slots and 15 SSC symbols are correspondingly obtained. The correlation results over 15 slots are compared the 64 possible RS codewords and all their phase shifts. The total number of hypothesis is $64 \times 15 = 960$. Then 960 comparison weights in total are computed and accumulated. The largest one is chosen as the candidate for code group and the frame starts at the original first phase of the candidate codeword.

B. New S-SCH synchronization

The new SSC sequence has the same chip length (256 chips) as the conventional one but it is divided into two subsequences, each of length 128 chips. The first subsequence is utilized to perform frame boundary synchronization and the second subsequence is used to convey the information of primary scrambling code group.

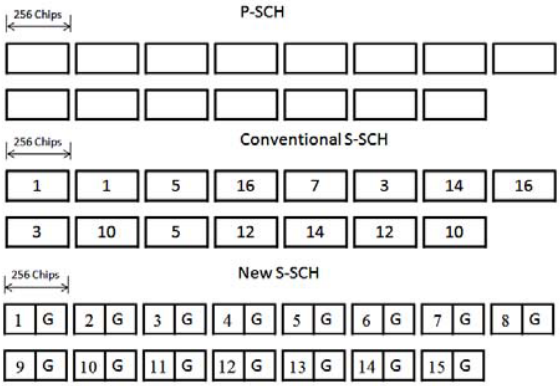


Fig. 1 PSC and SSC code structure

As shown in Fig. 1, in a slot time, the first 128 chips of the new SSC sequence are called Slot-ID Secondary Synchronization Code (S-SSC). We assign the slot IDs from 1 to 15 to every slot in sequence as in Fig. 1. Therefore, S-SSC is mapped into 15 symbols corresponding to 15 slot ID numbers. The S-SSC sequences can be represented as

$$S_n = (S_n(0), S_n(1), ..., S_n(127))$$

where $S_n(j) = 0$ or 1 and represents the nth row chosen from the Walsh-Hadamard matrix H_7.

On the other hand, the second 128 chips of the new SSC sequence are called Group-ID Secondary Synchronization Code (G-SSC). G-SSC switches between two 128-chip sequences from two rows of Walsh-Hadamard matrix H_7, which are mapped into binary bits (0 or 1). The new algorithm detects scrambling code group by decoding instead of searching. In each frame, there are totally 15 bits used to convey group ID number. Six bits are sufficient to represent a total of 64 possible code groups. A strong error correcting (15,7) BCH code is utilized to encode the group ID information. At the transmitter, a certain 6-bit group ID number supplemented by a parity bit is encoded into a 15-bit BCH codeword. Each of the 15 binary bits is mapped into 128-chip Walsh sequences for transmission.

In all, the new 256-chip SSC sequence at the beginning of each slot consists of 128-chip S-SSC and 128-chip G-SSC. Because of Walsh functions' orthogonality, it is possible to design all S-SSC and G-SSC combinations orthogonal to Primary Synchronization Code (PSC). Although the acquisition of the new SSC is very different from that of the conventional one, its code structures are compatible with the standard.

III. The New Synchronization Algorithm

The synchronization processes of the new S-SCH acquisition scheme are illustrated in Fig. 2. The slot boundary is already known by the system, as the first stage in the cell-search pipeline is assumed to be completed. In the new synchronization scheme, in each time slot, the first 128 chips of SSC are fed into a slot ID detector with 15-branch matched filters, each matched to one of the 15 slot IDs. As shown in Fig.

3, the detector chooses the largest coherent correlation value from matched filters to identify the slot ID, which is represented by a decimal number. Slot by slot, the outputs of the slot ID detector are fed into a counter logic unit, which detects boundary of the received frame, i.e. the most likely starting slot.

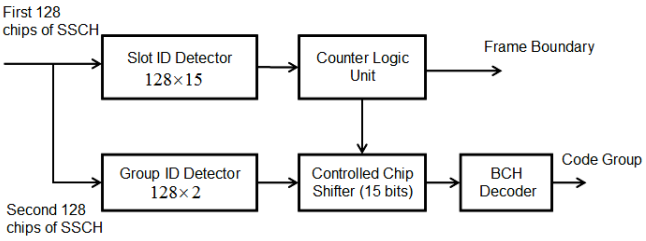


Fig. 2 Block diagram of new acquisition scheme

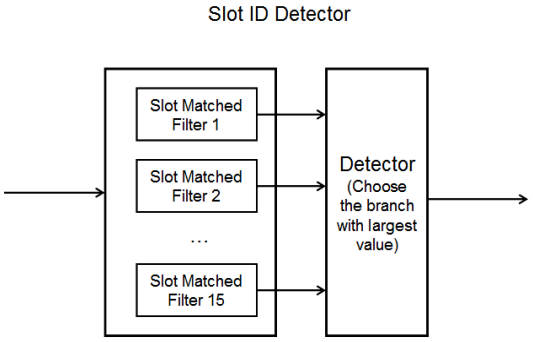


Fig. 3 Block diagram of slot ID detector

The counter logic unit adopts the maximum-likelihood principle to determine the starting slot ID of a certain received frame. The counter logic unit algorithm is shown in Fig. 4. During a frame time, 15 received slot IDs are fed into the counter logic unit in sequence. The received slot IDs (top of Fig. 4) form a 1×15 vector. In the counter logic unit, the received vector is compared with each row of a 15×15 matrix. The first row of the matrix assumes the starting slot is slot 1 and the total 15 slots in the first row are 1, 2, 3…15, denoted as decimal numbers. The remaining 14 rows of the matrix are different shifts of the first row. After comparison between the vector and the matrix column by column, the number of agreements is recorded as the counter value for each row, e.g. C1, C2…C15. For example, in Fig. 4, if the second element d2 in the received slot ID vector is 5 and it is equal to the second element in the fourth row w5, then the value of counter C4 is incremented by one. Finally, in a frame time, the row corresponding to the largest counter value of 15 counters is considered as the candidate of correct received slot ID vector and then the frame boundary is determined. For example, in Fig. 4, if C14 is the largest counter, then the starting slot of a radio frame is d3.

The computation of the counters C1, C2…C15 above is performed slot by slot and not on frame basis. This pipelined computation and sliding of slots assume fast processing so that all sliding frame based computations can be performed on slot basis.

The second 128 chips, namely G-SSC, are fed into a group ID detector, which makes binary bit decisions 1 or 0 by determining the larger output from two parallel matched filter branches matched to the possible two 128-chip sequences representing 1 or 0. For each received frame time, there are total of 15 binary bits to be decided and stored in the bit shifter, which is controlled by the control signal from counter logic unit (Fig. 2).

Since the counter logic unit has achieved frame boundary synchronization, it sends a control signal to group ID bit shifter. According to the control signal, the bit shifter is able to know the starting bit of the original BCH code sequence. Then the 15 bits received from detection of G-SSC are shifted and reordered as a BCH code sequence. Scrambling code group is identified by decoding the BCH code sequence and checking the parity bit.

d1	d2	d3	d4	…	d14	d15	
w1	w2	w3	w4	…	w14	w15	C1
w2	w3	w4	w5	…	w15	w1	C2
w3	w4	w5	w6	…	w1	w2	C3
w4	w5	w6	w7	…	w2	w3	C4
…	…	…	…	…	…	…	…
w14	w15	w1	w2	…	w12	w13	C14
w15	w1	w2	w3	…	w13	w14	C15

Fig. 4 Algorithm of counter logic unit

IV. Performance Analysis

In this section, we derive the successful synchronization probability based on the new algorithm. S-SSC detector and counter logic unit work together to perform frame boundary synchronization. The S-SSC detector consists of 15-branch matched filters and chooses the largest output of matched filters to determine the slot ID number. In this case, the correct detection probability of a single slot ID symbol P_{SD} has to be obtained. Normally, the worst case of Signal to Interference plus Noise Ratio (SINR) per chip in WCDMA system is $-18dB$. The SINR is defined as the ratio between the total SCH power and total interference noise power, which is equal to chip energy over noise density E_c / N_0. Because of the properties of orthogonal Walsh code sequences, P_{SD} can be approximately evaluated from the error rate of M-ary orthogonal signalling. The equivalent E_b / N_0 of S-SSC is $1dB$ for an equivalent orthogonal 16-FSK. From [18], the error probability for symbol detection P_e at $1dB$ is 0.4, which means the detection probability of a single slot ID symbol P_{SD} at $-18dB$ is 60%. This value is verified by computer

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simulations. Although the P_{SD} is not sufficient for the acquisition, the counter logic unit is able to improve the performance of frame boundary synchronization. Based on the functionality of the counter logic unit, the successful frame boundary detection probability P_{FB} can be expressed in (2). The derivation of P_{FB} is shown in the appendix.

Fig. 5 shows the calculation results of the relationship between P_{SD} and P_{FB}. The computations of P_{FB} show that even for low value of correct slot ID number detection probability $P_{SD} = 0.5$, the final successful frame boundary detection probability P_{FB} is 0.94. The counter logic unit is much more robust to slot ID detection errors yielded by match filters than the R-S code searching.

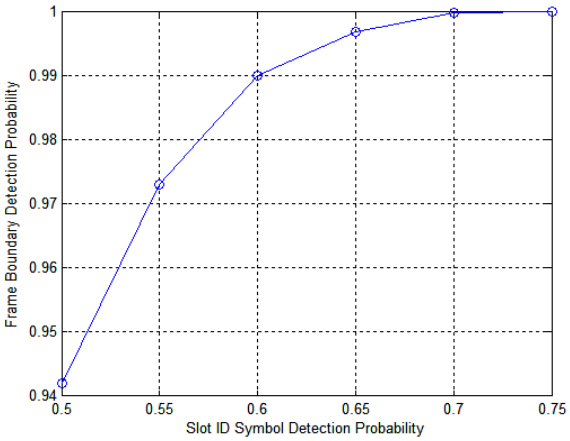


Fig. 5 Probability of correct symbol detection vs probability of successful frame boundary synchronization (SINR = -18dB)

Now we move to the group ID detection. It mainly benefits from 128-chip Walsh sequences and strong error correct coding. A single (15, 7) BCH code with two-bit error correction capability is selected for simplicity and powerful FEC coding. P_{GD} is the probability for code group number detection. The BCH decoding and parity bit checking increase the performance and reliability of group ID detection. When the E_c / N_0 is equal to $-18dB$, then the equivalent E_b / N_0 for BPSK signalling is $3dB$. Based on the analysis and simulation results for a AWGN BPSK system using a (15,7) BCH code, the Bit Error Rate (BER) at $3dB$ is 0.9×10^{-2}. Then the probability of correctly detecting the 6-bit group ID is $0.991^6 = 0.947$.

The final probability of successful code synchronization in the second stage of the WCDMA standard in the pipeline is shown as

$$P_D = P_{FB} \times P_{GD} \tag{1}$$

Under the worst condition that E_c / N_0 is $-18dB$, from the numerical analysis above, the probability of frame synchronization and the probability of code group detection are 0.96 and 0.95 respectively. Then the probability of acquisition for the case of AWGN channels is $P_D = 0.912$ and the Synchronization Error Rate (SER) is $1 - P_D = 0.088$.

V. Analysis and Simulation Results

In order to verify the analysis results of the new algorithm, we simulate the new SSC code synchronization process. The synchronization signals are transmitted through AWGN channels and Rayleigh fading channels with 30 Hz Doppler. The SINR varies from $-18dB$ to $-10dB$. The simulation assumes that the slot boundary is decided without errors by the first cell-search stage and the received S-SCH signal randomly starts from any slot in a radio frame. The group ID bits shifter is controlled by the outputs of counter logic unit. (15,7) BCH encoder and decoder are used in the transmitter and receiver. Finally, we check the frame boundary and code group number acquired by the receiver. If both of them are correctly detected, the successful synchronization counter is incremented. This synchronization simulation process is repeated 10,000 times. Fig. 6 shows the Synchronization Error Rate (SER) vs SINR of the simulation results and approximate analysis results of AWGN channel in the previous section.

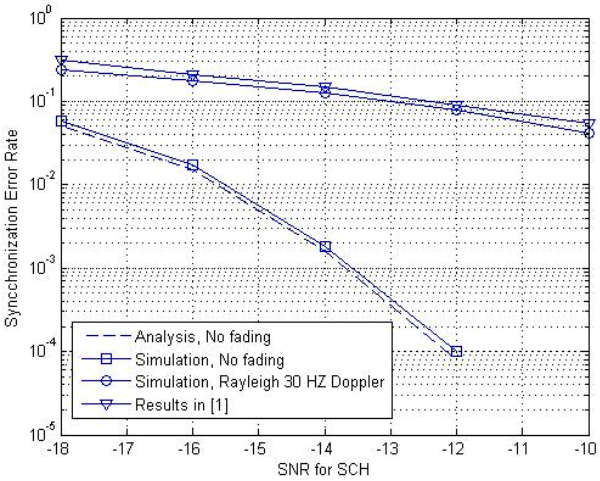


Fig. 6 Analysis and simulation results of synchronization error rate

In Fig. 6, we observe that the SER becomes less as the E_b / N_0 increases from $-18dB$ to $-10dB$. For the AWGN

$$P_{FB} = \sum_{i=8}^{15}\binom{15}{i}P_{SD}^{i}(1-P_{SD})^{15-i} + \sum_{k=6}^{7}\binom{15}{k}P_{SD}^{k}(1-P_{SD})^{15-k}\left(1-14\sum_{j=k+1}^{15-k}\binom{15-k}{j}\left(\frac{1}{14}\right)^{j}\left(\frac{13}{14}\right)^{15-k-j} - \frac{14}{2}\binom{15-k}{k}\left(\frac{1}{14}\right)^{k}\left(\frac{13}{14}\right)^{15-2k}\right)$$
$$+\binom{15}{5}P_{SD}^{5}(1-P_{SD})^{10}\left(1-14\sum_{n=6}^{10}\binom{10}{n}\left(\frac{1}{14}\right)^{n}\left(\frac{13}{14}\right)^{10-n} - \frac{14}{2}\binom{10}{5}\left(\frac{1}{14}\right)^{5}\left(\frac{13}{14}\right)^{5} + \frac{14}{6}\binom{10}{5}\left(\frac{1}{14}\right)^{10}\times 13\right) \tag{2}$$

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channel, the SER drops very quickly from 0.1 at $-18dB$ to almost 0 at $-10dB$. The analysis results and the simulation results are very close. However, for the Rayleigh fading channel with $30Hz$ Doppler, the SER keeps at relatively large values and it decreases slowly as the SINR drops. The simulation results for Rayleigh fading channels with different Doppler frequency are showed in Fig. 7. It is seen that the influence of the Doppler frequency on SER is very small. The comparison of acquisition performance between the new acquisition scheme and conventional technique will be given in section VII.

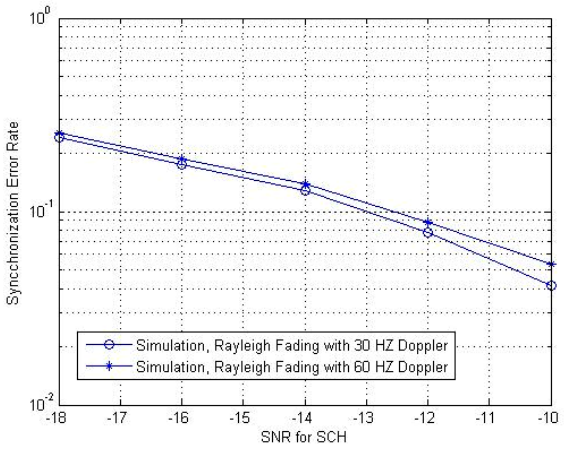


Fig. 7 Simulation results with different Doppler frequency

VI. Utilization of Antenna Diversity

In this section, we introduce the antenna diversity application with slot pipelining to the new algorithm. A simple and practicable antenna diversity system with 1 transmit antenna and 2 receive antennas is proposed as in Fig. 8. In this system, two duplicate synchronization signals are received by the receive antennas separately with different channel parameters, which are assumed to have been estimated from the result of the first stage PSC acquisition of the WCDMA standard. In [14], multiple receive antennas were able to significantly decrease the acquisition time in the first stage.

The new algorithm of the second stage works in this multiple antenna system as in Fig. 8. Without losing generality, we assume the maximum separation distance between two receive antennas is 1/4 wavelength $2\times1/4\times0.15=0.075m$. Then the propagation time difference between signal paths of two reception antennas is $0.025\times10^{-8}s$, which is much smaller than the chip duration $2.6\times10^{-7}s$. Therefore, it is reasonable to assume that after the successful slot boundary synchronization in the first stage, two received duplicate signals from the two antennas start at the same chip phase. The complexity of overall coherent matched filters is kept the same as $128\times(15+2)$, which is expressed as the total number of necessary additions and multiplications.

In the multiple antenna system as shown in Fig. 8, the 128-chip S-SSC sequence received by the first antenna is fed into the slot-ID detector which consists of 15 parallel matched filters. All correlation values yield by matched filters are temporarily stored. The S-SSC received by the second antenna is delayed by 128 chips to be fed into the same slot-ID detector. In this case, the correlation values obtained by 15 matched filters are accumulated through two 128-chip S-SSC sequences from two different reception antennas. For frame boundary synchronization, the detector chooses the largest correlation value from the combined correlation values to determine correct slot ID. For the group ID detection, same pipelined correlation combining process from two received signals is followed. The 256-chip correlations of two duplicate 128-chip G-SSC are accumulated for binary bit decision. In Fig. 8 and 9, we observe that the G-SSC received by the first antenna and the S-SSC received by the second antenna are fed into the group-ID detector and slot-ID detector separately at the same time. This implies a pipelining multiple-antenna acquisition process using same detection resources. There is no change for counter logic units, bit shifter and BCH decoder, which operate on the combined results of the two antennas as mentioned above.

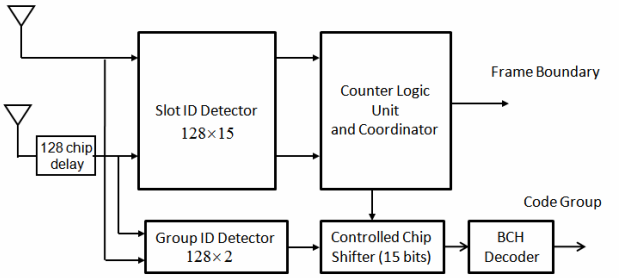


Fig. 8 Block diagram of two reception antennas

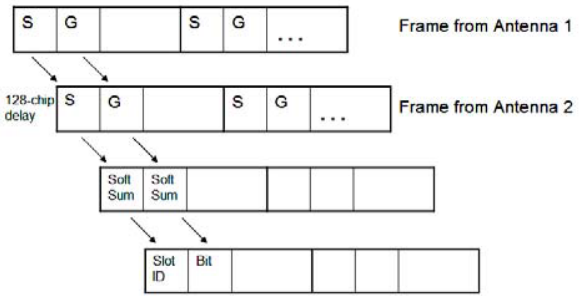


Fig. 9 Pipelined acquisition for antenna diversity

In fact, the SSC sequence only occupies the first 256 chips of the slot with 2560 chips. Therefore, the delays of the multiple antennas occur within a slot time. It may not increase the acquisition time if the correlation processes are sufficiently fast. This implies that more receiving antennas can be employed in this pipelining multiple antenna systems to further improve the synchronization performance. The summation of all different antenna delays should be smaller than 2560 chips. Hence, ignoring the correlation processing time, the maximum number of reception antennas which can be implemented in the system is (2560-256)/128 + 1= 19.

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By introducing multiple antenna diversity, we can observe the SER improvements in Fig. 10 and Fig. 11, which illustrate the simulation results of systems with and without antenna diversity in AWGN channels and in Rayleigh fading channels. Obviously, the error rates of the system with two receive antennas are less. There is still no R-S decoding and 960 times searching in further process of acquisition in the standard, which implies a lot of time and computations are saved. So in this kind of slot pipelining multiple antenna systems, the overall new synchronization scheme is still less complicated and more time efficient than the conventional technique used in the standard.

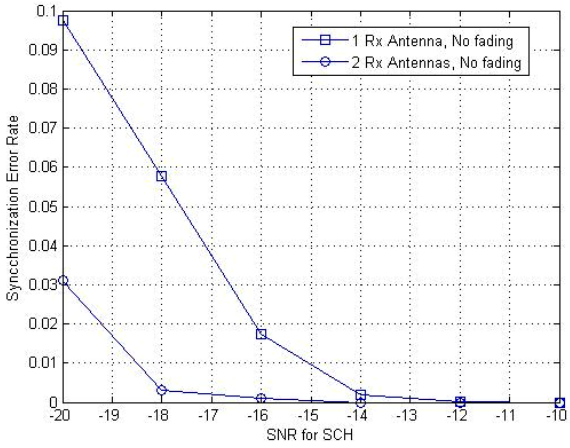


Fig. 10 Simulation results of SER in AWGN channel with different number of receive antennas

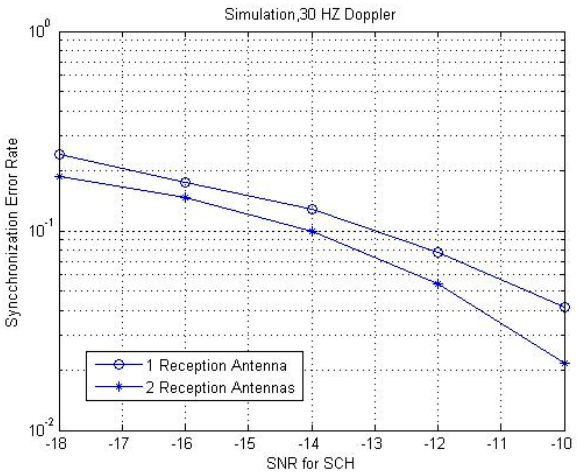


Fig. 11 Simulation results of SER in Rayleigh fading channels with different number of receive antennas

VII. Synchronization of Performance Comparisons

In this section, we compare the new secondary synchronization algorithm with the conventional one in three aspects: synchronization error rate (SER), system complexity and acquisition time.

First, from the Fig. 7 in [1] and Fig. 6 in this paper, we observe that the SER performance of the new algorithm is very close to that of the conventional one in Rayleigh fading channels. As we analyzed before, the counter logic unit can tolerate with more detection errors than R-S code searching and the BCH coding can improve the error probability. These properties compensate the SINR loss of each sub-sequence. Moreover, as shown in Fig. 11, by simply applying two receive antennas in the new acquisition scheme to perform slot-based pipelining, the SER decreases and the synchronization performance is improved by almost $3dB$ SINR.

Second, for general correlation process, the required number of multiplication and addition operations is measured by the chip length multiplied by the number of correlation branches. In the conventional acquisition scheme of the SSC secondary stage, to obtain the coherent values, 256×16 multiplication and addition operations are needed. The new algorithm reduces these operations into 128×17 , a reduction of almost 50% . Because of pipelining, the coherent correlation complexity can be kept the same as 128×17 when two or more receive antennas are utilized. Moreover, in the standard, the RS code weight computations and comparisons are much more involved than the counter logic unit and the BCH decoder, which can be performed by simple logic circuits. Obviously, the new algorithm is able to simplify the hardware design and implementation.

Third, assuming T_S denotes the time for filling code sequences of a single slot. Because we have already discussed the matched filter complexity, for fair comparison, we assume the coherent correlation time T_{CD} of all systems are the same under different hardware complexities. T_{RS} denotes the time for the R-S code weight computation and comparison, T_{BCH} denotes the time for BCH decoding. The time taken in bit shifter is negligible. P_{CSY} denotes the probability of successful synchronization for conventional algorithm, P_{NSY1} denotes the probability of successful synchronization for the new algorithm with 1 receive antenna and P_{NSY2} is the probability of synchronization for new algorithm with 2 receive antennas. Because of the pipelined cell-search process, we don't consider the penalty time of false alarm for the single cell-search step. Then the share of the second stage of the total acquisition time for conventional acquisition scheme is

$$T_{CSY}=\sum_{n=0}^{\infty}(T_{CD}+T_{RS})(1-P_{CSY})^n=\frac{T_{CD}+T_{RS}}{P_{CSY}} \qquad (3)$$

where T_{RS} is mainly due to RS code searching and the frame fill up time is not included. Actually, each acquisition time in the conventional scheme consumes at least $T_{CD}+T_{RS}=10ms$, which is a SCH frame duration. And the shares of stage 2 of the total acquisition time with 1 receive antenna and 2 receive antennas for the new acquisition scheme are

$$T_{NSY}=\sum_{n=0}^{\infty}(T_S+T_{CD}+T_{RS})(1-P_{NSY1})^n=\frac{T_S+T_{CD}+T_{BCH}}{P_{NSY1}} \qquad (4)$$

$$T_{NSY2}=\sum_{n=0}^{\infty}(T_S+T_{CD}+T_{RS})(1-P_{NSY2})^n=\frac{T_S+T_{CD}+T_{BCH}}{P_{NSY2}} \qquad (5)$$

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where we again ignore frame fill up time for fair comparison. Fig. 12 shows the approximate results of the synchronization time in the secondary cell-search stage. We can clearly observe that the acquisition time of the new synchronization scheme is much smaller than the time of the conventional scheme.

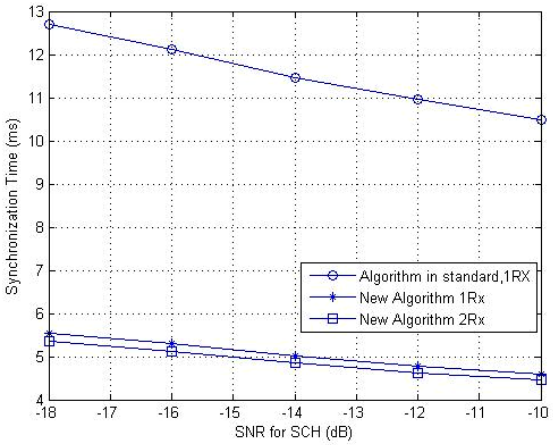


Fig. 12 Mean synchronization time for different acquisition schemes

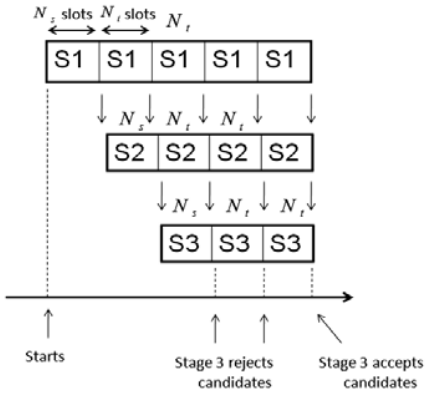


Fig. 13 Cell-search time evaluation

In fact, the synchronization time improvement of the S-SCH acquisition techniques has to be combined with the results of other two stages in the WCDMA cell-search. In this paper, when evaluating the average cell-search time, we assume there is no synchronization error yielded in other two stages. Fig. 13 illustrates a sample of the three-stage cell-search process. It is seen that the process starts at the first synchronization trial in the first stage and stops until the third stage accepts the correct candidate. For each synchronization stage, as shown in Fig. 13, the first synchronization trial consumes N_s slot durations and the following trials consume N_t slot durations. The verification process and penalty time are not considered. Then the average cell search time T_{CS} can be expressed as

$$T_{CS} = 3N_S \times 0.667ms + \sum_{n=1}^{\infty}(1-P_D)^n N_t \times 0.667ms \qquad (6)$$

where P_D denotes the probability of correct synchronization in the secondary stage.

In the conventional cell-search process, the synchronization trial in the first stage and in the third stage can be fast completed within several slot durations. However, due to the time-costly RS code searching in the second stage, the cell-search process takes the frame-based pipelining, which means every synchronization trial consumes more than 15 slot durations. In the new algorithm, however, only the first synchronization trials in all stages consume 15 slot durations. The synchronization trials in the following only update several slots less than 15. For example, the counter logic unit and BCH decoder can update 5 slot IDs and 5 BCH bits to obtain new candidates of frame boundary and scrambling code group. In this case, the new S-SCH synchronization algorithm is able to eliminate the bottleneck caused by the second stage and performs the slot-based pipelining.

Therefore, we can derive the expressions of the average cell-search time for conventional and new synchronization schemes from (6)

$$T_{CCS} = 45 \times 0.667ms + \sum_{n=1}^{\infty}(1-P_{CSY})^n \times 15 \times 0.667ms \qquad (7)$$

$$T_{NCS} = 45 \times 0.667ms + \sum_{n=1}^{\infty}(1-P_{NSY-SB})^n \times 5 \times 0.667ms \qquad (8)$$

where P_{CSY} denotes the correct synchronization probability in the secondary stage of the conventional scheme and P_{NSY-SB} denotes the correct synchronization probability in the secondary stage of the new slot-based pipelining scheme.

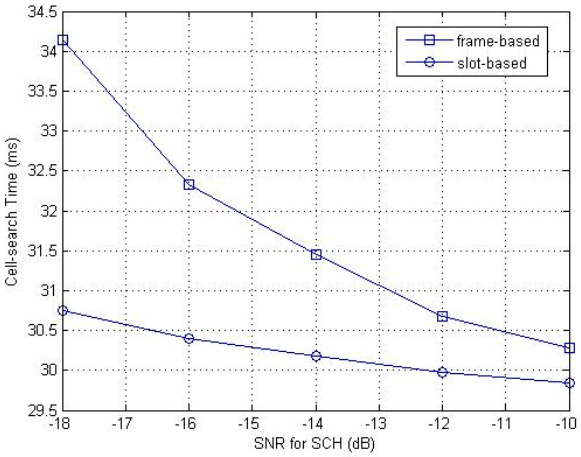


Fig. 14 Average cell-search time of frame-based and slot-based pipelines

Fig. 14 demonstrates the average cell-search time of frame-based pipelining and slot-based pipelining. We observe that the slot-based pipelining significantly reduces the average cell-search time especially in the range of low SINR.

In all, the code group number is obtained by a decoding process which is much faster than the 960 times R-S code comparisons in the conventional synchronization case. After receiving the first frame, the candidates of the frame boundary and code group can be updated by several slots (e.g., 5 slots)

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rather than a frame (15 slots), which is able to perform the cell-search process by slot-based pipelining.

VIII. Conclusion

In this paper, a new synchronization algorithm for the second cell-search stage of the WCDMA system is presented and its performance is compared with that of the conventional synchronization scheme in three aspects: Synchronization Error Rate (SER), system complexity and acquisition time. The conventional algorithm employs the involved and time-costly RS code computations and comparisons to capture frame boundary and scrambling code group simultaneously. New SSC sequences are redesigned by splitting into two sub-sequences, one for frame boundary acquisition and the other for code group determination. Counter logic algorithm and synchronization coding improve the probability of successful synchronization. The SER performances of the new algorithm and conventional techniques are very close but the new algorithm reduces the system complexity, shortens the mean acquisition time and can be implemented in the slot-based cell-search pipeline.

Another advantage for the new algorithm is that antenna diversity can be easily utilized by pipelining without change system complexity. The SER is obviously reduced with the application of two receive antennas. Because of the synchronization coding design of the new SSC sequences rather than searching, it provides the acquisition system with potential to utilize Space-Time coding in the MIMO environment.

Appendix

The analysis for counter logic algorithm can be divided into several conditions. It is a must to note that the sum of all counter values in a frame time is equal to 15. So if 8 or more slot ID numbers are detected correctly, the largest value out of 15 counters is yielded by the correct detection and the maximum value of any other 14 counters is 15-8=7. Obviously, the maximum counter yields the correct decision for frame boundary synchronization. Under this condition, the probability of correct frame boundary detection is

$$P_8 = \sum_{i=8}^{15} \binom{15}{i} P_{SD}^{i} (1-P_{SD})^{15-i} \tag{9}$$

Following, the probability of 7 slot ID correctly detected out of 15 slots in a certain frame is expressed as

$$P_{70} = \binom{15}{7} P_{SD}^{7} (1-P_{SD})^{15-7} \tag{10}$$

However, this is not the probability of final detection given 7 correctly detected counter IDs and we have to subtract few probabilities corresponding to following two scenarios. Since 8 out of 15 slot ID numbers are detected in error, it is possible that the largest counter value is 8. In this scenario, the counter logic unit makes the false frame synchronization. The probability of this scenario is shown in (11), which is the probability that a counter value of 8 falsely exceeds the correct detection of value 7.

$$P_{71} = \binom{15}{7} P_{SD}^{7} \binom{8}{8} (15-1)\left(\frac{1-P_{SD}}{15-1}\right)^{15-7} \tag{11}$$

where $\binom{15}{7} P_{SD}^{7}$ means 7 slot IDs are detected correctly. $\left(\frac{1-P_{SD}}{15-1}\right)^{8}$ represents the probability that the eight slot ID errors help to increase one specific counter value. $15-1=14$ means we have 14 possible counters which are possible candidates for having a counter value of 8 due to slot ID errors except the counter with value 7 because of correct slot ID detection.

Another scenario for condition 7 is that we have two largest counter values and each value is equal to 7. One is caused by the correct detection P_{SD}^{7} and the other one is caused by the wrong slot ID detection $\left(\frac{1-P_{SD}}{15-1}\right)^{15-7-1}$. This is a tie condition that our system randomly chooses one of the largest counter values. The probability for this scenario is shown in (12).

$$P_{72} = \binom{15}{7} P_{SD}^{7} \binom{8}{7} (15-1)\left(\frac{1-P_{SD}}{15-1}\right)^{15-7-1}\left(\frac{(1-P_{SD})(15-2)}{15-1}\right) \tag{12}$$

where $\left(\frac{(1-P_{SD})(15-2)}{15-1}\right)$ is the probability that the remaining one slot helps to increase the other 13 counters expect two largest counters. So finally, the successful frame boundary detection probability for 7 slot ID numbers detected correctly is

$$P_7 = P_{70} - P_{71} - \frac{1}{2} P_{72} \tag{13}$$

All other scenarios given the maximum value of the correct counter value is 7 ensure the 8 remaining counter values are scatted and no counter has a value exceeding 6. The analysis for 6 and 5 slot ID number correct detection is similar but more involved. In order to be more confident in the results of frame boundary detection, if the largest counter value is smaller than 5, the system thinks the result is not reliable and provides no candidate for the next synchronization process. As a matter of fact, the probabilities for these conditions are very small.

Repeating the above procedure for P_6, P_5, etc and combing all terms, we can obtain the successful frame boundary detection probability P_{FB} in (2).

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