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Improvement of Short Channel Effects in Cylindrical Strained Silicon Nanowire Transistor

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***Abstract*—**In this paper we investigate the electrical characteristics of a new structure of gate all around strained silicon nanowire field effect transistors (FETs) with dual dielectrics by changing the radius (R_{SiGe}) of silicon-germanium (SiGe) wire and gate dielectric. Indeed the effect of high-κ dielectric on Field Induced Barrier Lowering (FIBL) has been studied. Due to the higher electron mobility in tensile strained silicon, the n-type FETs with strained silicon channel have better drain current compare with the pure Si one. In this structure gate dielectric divided in two parts, we have used high-κ dielectric near the source and low-κ dielectric near the drain to reduce the short channel effects. By this structure short channel effects such as FIBL will be reduced indeed by increasing the R_{SiGe}, I_D-V_D characteristics will be improved. The leakage current and transfer characteristics, the threshold-voltage (Vt), the drain induced barrier height lowering (DIBL), are estimated with respect to, gate bias (V_G), R_{SiGe} and different gate dielectrics. For short channel effects, such as DIBL, gate all around strained silicon nanowire FET have similar characteristics with the pure Si one while dual dielectrics can improve short channel effects in this structure.

***Keywords*—**SNWT (silicon nanowire transistor), Tensile Strain, high-κ dielectric, Field Induced Barrier Lowering (FIBL), cylindrical nano wire (CW), drain induced barrier lowering (DIBL).

I. INTRODUCTION

DRIVING capability of strained silicon (Si) field effect transistors (FETs) make them more attractive than pure Si-based FETs. Compared with the pure Si-based FET, the strained FET has a slightly higher leakage current due to the silicon germanium (SiGe) channel film has a lower bandgap[1]-[6]. Multiple gate structures are considered as promising candidates to overcome short channel effects (SCE) usually encountered in nano-scale MOSFET.

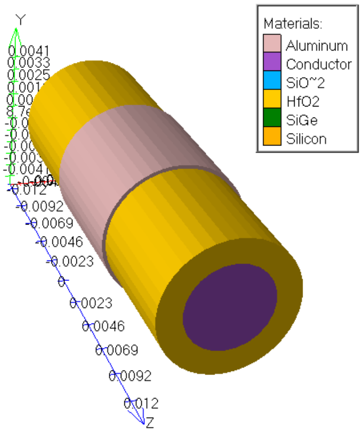

Fig.1 Simulated strained nano wire field effect transistor

They have better transport characteristics and improved short channel effects (SCEs) than that of single gate (SG) FETs [7] - [11]. Pure Si-based gate all around transistors have the best channel controllability and lowest SCEs among different structures of FETs [12]–[14]. In this paper, a new structure of gate all around stained Si nanowire FET with various gate dielectrics will be investigated as shown in fig.1. High-κ dielectrics are using to compensate the thick oxide. By using the High-κ dielectrics gate control increases and drain current will be improved while fringing drain field can affect to barrier height easily and result in increasing the short channel effects [5]-[18]. To reduction this effects we used low-κ dielectric near the drain to control the DIBL effects. We find that the gate all around strained Si nanowire FETs exhibit higher on-state current and sustain almost the same off-state current and short channel effects, compared with the surrounding-gate Si nanowire FETs. Combinative dielectrics of high-κ and low-κ could help to improve the short channel effects and get the high speed structures.However, the surrounding-gate strained Si nanowire FET sustains the similar I_{on}/I_{off} current ratio, the threshold voltage roll-off, and SCEs, compare with the characteristics of pure Si one. The

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paper is organized as follows. In section 2, we describe the device and its structural parameters. Section 3 describes the simulation results. Section 4 draws conclusions.

II. DEVICE STRUCTURE

We have simulated a cylindrical gate all around strained SNWT with dual dielectrics as shown in fig.1. The structure is with a SiGe nanowire covered by a layer of Si. The composition of Si_xGe_{1-x} of the *n*-type FET is fixed at $x = 0.8$ in our simulation. In these analyses the gate length is 8nm, gate is made of aluminum and its work function is 4.1 eV. The oxide thickness is 2nm, the channel is P-doped with $N_A=10^{17}(cm^{-3})$ and the source and drain are doped with $N_d= 10^{20}(cm^{-3})$. The radius of Si and SiGe is equal to 2.5 nm, and transport is along z direction. Full quantum mechanical models are the most accurate ways to study such nano scale devices. 3D density-gradient drift-diffusion model is used in this simulation [12]-[14]. In this study we work on device characteristic optimization with respect to various physical parameters including R_{SiGe}, composition effects of Si_xGe_{1-x} and $L_{high-\kappa}/L_{low-\kappa}$.

III. RESULTS AND DISCUSSIONS

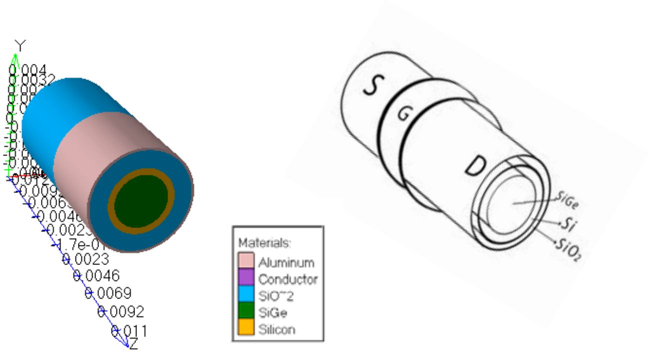

Fig. 2 Three dimensional simulation of the Gate all around Cylindrical strained SNWT with different SiGe radius

A. Strained Silicon Channel

Figure 3 shows the $I_D - V_G$ curves of the gate all around strained Si FETs with different R_{SiGe}. Results confirm that by increasing the R_{SiGe} transfer characteristic doesn't change alot thus threshold voltage and I_{ON}/I_{OFF} ratio are the same for pure Si and strained Si nano wire transistors. Band gap of SiGe is intrinsically smaller than that of pure Si, but the leakage current does not influenced. This consequence is caused from the fact that gate all around nanowire FETs have excellent gate control. Therefore, leakage current can not improve the on state current. Fig. 4, Shows the $I_D - V_D$ curves of the gate all around strained Si nanowire FET. Strained SNWT with R_{SiGe} = 1 and 2 nm, respectively, has a higher drain current than that of the pure Si one (solid lines). The larger radius (R_{SiGe} = 2 nm) of SiGe implies the higher drain current due to a higher stress caused from the thicker SiGe radius. The lower source/drain parasitic resistance caused from the SiGe layer plays another factor for the enhancement of the on-state current [19].

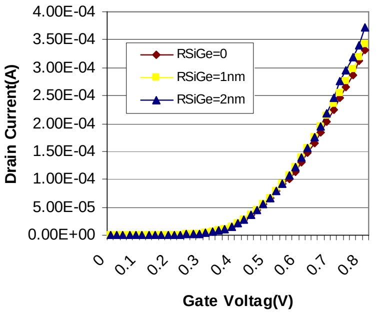

Fig. 3 I_{DS} verses gate voltage in SNWT with different R_{SiGe} V_{DS}=0.5V

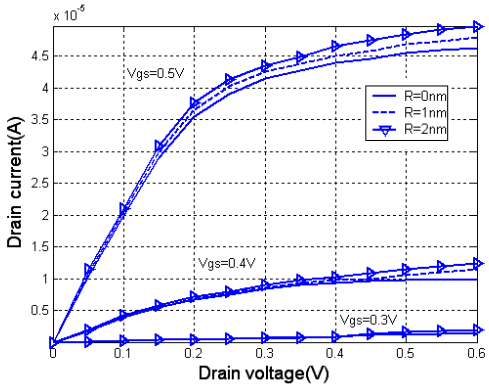

Fig. 4 The computed $I_D - V_D$ curves of the FET with different R_{SiGe}.

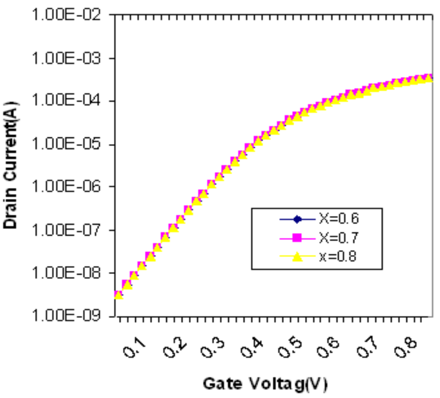

Fig. 5 The computed $I_D - V_G$ curves of the FET with different X.composition (Si_xGe_{1-x}),V_{DS}=0.5V

In fig. 5 transfer characteristic are plotted for different X.composition. the results show that drain current has not been influenced by changing the composition.

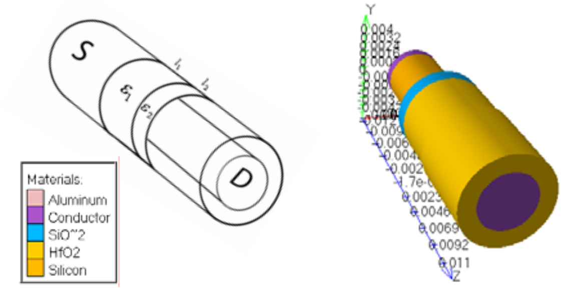

Fig. 6 Three dimensional simulation of the Gate all around Cylindrical strained SNWT with dual gate dielectrics and R_{SiGe}=1.5nm

B. Dual dielectrics

In this section we are going to improve the short channel effects by using the Combinative dielectrics of high-κ in all structure and low-κ dielectric near the drain as shown in fig.6. High-κ materials are using to improve the gate control in stead of thin oxide layer. On the other hand these materials cause to increasing the drain fringing field effects on the channel and FIBL increases. Therefore the use of a low-κ material near the drain could help to reduce the FIBL. In fig. 7 the effect of two dielectrics length rate on threshold voltage is investigated for different dielectrics constant at drain side. In this study the dielectric constant of gate is 26 and the dielectric constant at drain side is changes from 26 to 3.9. As the figure shows by considering the rate $L_{high-κ}$/ $L_{low-κ}$ equal to 3 or upper, threshold voltage will be almost constant.

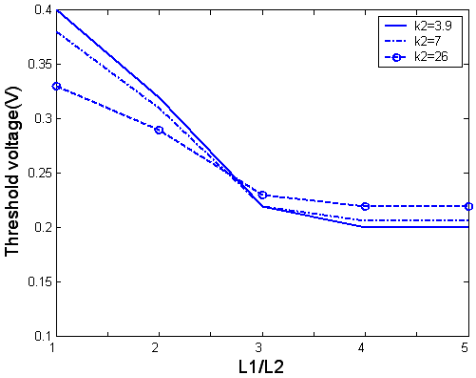

Fig. 7 The effect of dielectrics length rate on threshold voltage with dual gate dielectrics and R_{SiGe}=1.5nm (L_1 is high-κ dielect and L_2 is low-κ length)

In fig.8 the effect of dual gate dielectrics on transfer characteristics is plotted. In this simulation R_{SiGe} is 1.5 nm and L_1/L_2 ratio is equal to 3. $κ_1$ is dielectric constant at source side and $κ_2$ is dielectric constant at drain side.

The result shows that by decreasing the dielectric constant at drain side off state current reduces as well as reduction in short channel effects.

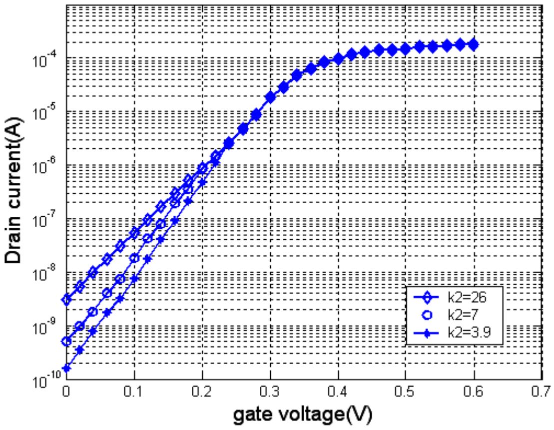

Fig. 8 The effect of dielectrics constant at drain side on I_D-V_{GS} characteristic in strained silicon nano wire transistor with R_{SiGe}=1.5nm (k_1 is high-κ dielectric and k_2 is low-κ dielectric)

By this structure we could reduce the short channel effects and off state current as shown in table 1.

TABLE I
THE EFFECT OF DIELECTRIC CONSTANT AT DRAIN SIDE ON FIBL AND OFF STATE CURRENT

$l_1/l_2 = 3$, $\varepsilon_1 = 26$	*FIBL*	I_{OFF}
$\varepsilon_2 = 26$	517	3.21e^{-9}
$\varepsilon_2 = 7$	342	6.09e^{-10}
$\varepsilon_2 = 3.9$	168	1.52e^{-10}

IV. CONCLUSION

We have investigated a new structure of cylindrical strained SNWT with dual gate dielectrics. We have studied the effect of R_{SiGe} on the electrical characteristics of the gate all around strained Si nanowire FET using a 3D device simulation by ATLAS simulator [20]. R_{SiGe} can change the driving current of our structure. When R_{SiGe} is increased, the driving current is increased. However, it does not have significant effects on the transfer characteristics. In this structure strain can not improve the short channel effects, the I_{on}/I_{off} ratio or any changes in threshold voltage. Because of excellent gate control in gate all around structures, gate leakage current negligibly increase the on state current. To reduce the short channel effects and improve the I_{on}/I_{off} ratio dual gate dielectrics is used. Length ratio (L_1/L_2) is chosen equal to 3, to keep the threshold voltage off changing by dielectric constant. Simulation results have shown that this structure of gate all around strained Si nanowire FET is attractive to application of high speed nano devices. Low source/drain parasitic resistance, high driving current, low off state current, high gate control and low short channel effects are the significant characteristics of this structure. By this structure the Field Induced Barrier Lowering reduced about 350mV/V which indicates to high gate control in this gate all around silicon nano wire structure.

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