

# An On-chip LDO Voltage Regulator with Improved Current Buffer Compensation

Lv Xiaopeng, Bian Qiang, Yue Suge

**Abstract**—A fully on-chip low drop-out (LDO) voltage regulator with 100pF output load capacitor is presented. A novel frequency compensation scheme using current buffer is adopted to realize single dominant pole within the unit gain frequency of the regulation loop, the phase margin (PM) is at least 50 degree under the full range of the load current, and the power supply rejection (PSR) character is improved compared with conventional Miller compensation. Besides, the differentiator provides a high speed path during the load current transient. Implemented in 0.18 $\mu$ m CMOS technology, the LDO voltage regulator provides 100mA load current with a stable 1.8V output voltage consuming 80 $\mu$ A quiescent current.

**Keywords**—capacitor-less LDO; frequency compensation; transient response; power supply rejection

## I. INTRODUCTION

COMPARED with DC-DC converters, LDO voltage regulators are less complex and easier to be fully integrated on-chip. As an essential building block of the power management system, LDO voltage regulators provide an accurate and stable DC voltage under the battery powered circumstances.

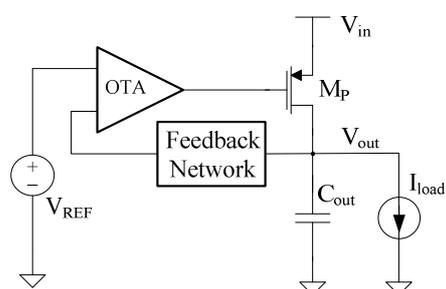


Fig. 1 Conventional LDO voltage regulator structure

The conventional LDO voltage regulators (Fig. 1) implemented in CMOS technology often use the PMOS FET with common source connection as the pass transistor between the input and output voltages. An amplified error signal is fed back to the gate of the pass transistor through the feedback loop to respond to the load current while keeping the output voltage constant. Recently, the off-chip output capacitor of several microfarads is eliminated to meet the System-on-Chip (SoC) demand of on-chip LDO voltage regulators; however, the on-chip output capacitor provided by the power line capacitance is reduced to tens or hundreds of picofarads, degrading the output voltage peaks during fast load current transient.

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Moreover, the stability of the closed loop under the full range of the load current needs to be guaranteed, however, the conventional Miller compensation with pole splitting degrades the frequency response and the power supply rejection (PSR) character due to the feed forward path [1].

This paper presents an improved current buffer compensation technique for on-chip LDO voltage regulator, the unit gain frequency and the PSR character are improved by eliminating the feed forward path. Besides, a high-speed path provided by a differentiator is adopted to supply extra charging or discharging current during fast load current transient.

## II. THE PROPOSED BLOCK DIAGRAM

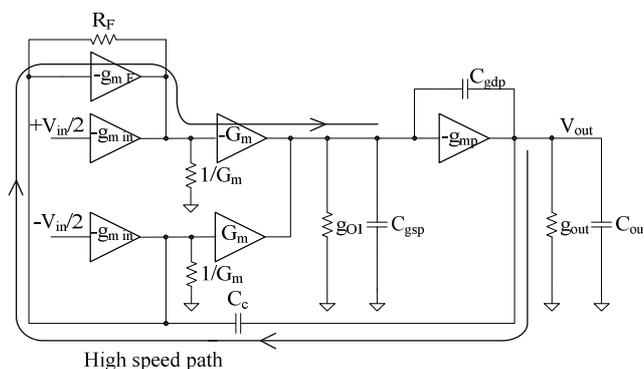


Fig. 2 Block diagram of the proposed LDO voltage regulator

The proposed block diagram of the open loop LDO voltage regulator with improved current buffer compensation [2], [3] and high speed path is shown in Fig. 2. It consists of a folded cascode differential amplifier and a pass transistor with common source connection. The transconductance of the input stage, the cascode transistor, and the pass transistor is  $g_{m\text{ in}}$ ,  $G_m$ , and  $g_{m\text{ p}}$ , respectively. The output conductance of the OTA and the LDO is  $g_{o1}$  and  $g_{o\text{ out}}$ . To drain load current of 100mA, the pass transistor with large dimension introduces parasitic capacitors  $C_{g\text{ sp}}$ ,  $C_{g\text{ dp}}$  that have to be considered with the compensation capacitor  $C_c$ .  $C_{o\text{ ut}}$  is the on-chip capacitor provided by the power line. The differentiator composed of inverting transconductance  $g_{m\text{ F}}$ , capacitor  $C_c$  and resistor  $R_F$  creates a high speed path during load current transient.

### A. AC small signal analysis

Consider the loop gain frequency response where the feedback factor is 1, the AC small signal transfer function of the proposed LDO structure is given by (1), based on assumptions:

- The transconductance  $g_m$  is much larger than the output conductance  $g_o$ , that is  $g_m/g_o \gg 1$ ;
- Only the parasitic capacitors  $C_{g\text{ sp}}$ ,  $C_{g\text{ dp}}$  of the pass transistor,

the compensation capacitor  $C_c$  and the output load capacitor  $C_{out}$  are considered, ignoring the other parasitic capacitors.

The DC gain of the feedback loop is

$$\frac{V_{out}}{V_{in}}|_{DC} = \frac{g_{m in} g_{mp}}{g_{o1} g_{out}} \quad (2)$$

the dominant pole and zeros are

$$\omega_{dp} = -\frac{g_{o1} g_{out}}{g_{mp} C_c} \quad (3)$$

$$\omega_{zL} = -\frac{2G_m}{C_c} \quad (4)$$

$$\omega_{zR} = +\frac{g_{mp}}{C_{gs} + 2C_{gd}} \quad (5)$$

the gain bandwidth product is

$$GBW = \frac{g_{m in}}{C_c} \quad (6)$$

The proposed structure presents single dominant pole within the GBW; two zeros far beyond the GBW and two non-dominant poles changing dramatically with the load current. Considering the stability of the proposed structure at different load conditions:

Case 1: low to moderate load current:  $g_{mp}$ , the transconductance of the pass transistor is small enough that  $g_{mp} C_{gdp} C_c \gg G_m C_{pgate} C_{out}$  holds, thus, the later factor of the transfer function's denominator is given approximately as bellow, where  $C_{pgate}$  is the sum of  $C_{gsp}$  and  $C_{gdp}$ .

$$D(s) \approx C_{pgate} C_c C_{out} s^2 + G_m C_{pgate} C_{out} s + G_m g_{mp} C_c \\ \approx (s + \frac{g_{mp} C_c}{C_{pgate} C_{out}}) (C_{pgate} C_c C_{out} s + G_m C_{pgate} C_{out}) \quad (7)$$

Under this condition, the proposed structure presents two non-dominant poles beyond the GBW.

$$\omega_{ndp1} = -\frac{g_{mp} C_c}{C_{pgate} C_{out}}; \quad (8)$$

$$\omega_{ndp2} = -\frac{G_m}{C_c}; \quad (9)$$

$$H(s) = \frac{V_{out}}{V_{in}}(s) = \frac{\frac{1}{2} g_{m in} [C_c (C_{gsp} + 2C_{gdp}) s^2 - g_{mp} C_c s - 2G_m g_{mp}]}{C_{pgate} C_c C_{out} s^3 + (G_m C_{pgate} C_{out} + g_{mp} C_{gdp} C_c) s^2 + G_m g_{mp} C_c s + G_m g_{o1} g_{out}} \\ \approx \frac{\frac{1}{2} g_{m in} (s + \frac{2G_m}{C_c}) [C_c (C_{gsp} + 2C_{gdp}) s - g_{mp} C_c]}{\left( s + \frac{g_{o1} g_{out}}{g_{mp} C_c} \right) [C_{pgate} C_c C_{out} s^2 + (G_m C_{pgate} C_{out} + g_{mp} C_{gdp} C_c) s + G_m g_{mp} C_c]} \quad (1)$$

Case 2: moderate to large load current:  $g_{mp}$  is large enough that the proposed structure presents a pair of conjugate complex non-dominant poles far beyond the GBW. The corresponding natural frequency and quality factor are

$$\omega_{ndp} = -\sqrt{\frac{G_m g_{mp}}{C_{pgate} C_{out}}}; \quad (10)$$

$$Q = \frac{C_c \sqrt{C_{pgate} C_{out} G_m g_{mp}}}{G_m C_{pgate} C_{out} + g_{mp} C_{gdp} C_c}; \quad (11)$$

The analysis of the two cases above indicates that the proposed structure presents only single dominant pole within GBW, moreover, the impact of the zeros and non-dominant poles beyond the GBW on the phase margin of the feedback loop fulfills the stability condition.

### B. Transient analysis

To reduce the output voltage variation during fast load current transient, the differentiator detects the output voltage and injects the current through the high speed path to charge or discharge the capacitor of the pass transistor.

### C. Power supply rejection analysis

The frequency compensation scheme based on current buffer creates the same dominant pole as the Miller compensation while eliminating the feed forward path provided by conventional Miller capacitor. Thus, the PSR at high frequency is improved.

## III. THE PROPOSED TRANSISTOR-LEVEL IMPLEMENTATION

The transistor-level implementation of the proposed LDO structure is shown in Fig. 3. Transistors  $M_1$  to  $M_8$  form the folded cascode OTA with differential inputs provided by the feedback voltage  $V_{FB}$  and the reference voltage  $V_{REF}$ . The pass transistor and the on-chip output capacitor are labeled as  $M_p$  and  $C_{out}$  respectively. The series feedback network composed of  $R_{fb1}$ ,  $R_{fb2}$  provides the feedback signal  $V_{FB}$  to the non-inverting input of the OTA.

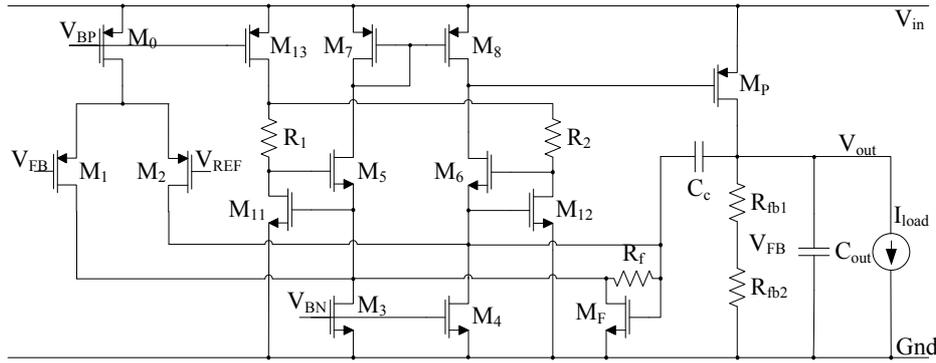


Fig. 3 Schematic of the proposed LDO voltage regulator

To obtain adequate phase margin without peaking in magnitude response beyond the GBW, the transconductance of the cascode transistor is increased with gain boosting technique. The auxiliary amplifiers composed of  $M_{11}$ ,  $R_1$  and  $M_{12}$ ,  $R_2$  increase the transconductance of the cascode transistor by a factor of  $1+g_{m11}R_1$ ,  $1+g_{m12}R_2$  respectively.  $M_{13}$  supplies bias current for the auxiliary amplifiers and the differential mode signal is cancelled out at the drain.

The capacitor  $C_c$  implementing the current buffer frequency compensation is connected between the output voltage and the input of the cascode transistor  $M_6$ . The differentiator composed of  $M_F$ ,  $R_F$  and  $C_c$  detects the variation of the output voltage in the form of current. Then, the current passes through the cascode transistor  $M_5$  and current mirror composed of  $M_7$  and  $M_8$  with low resistance nodes to charge or discharge the capacitors at the gate of the pass transistor.

#### IV. SIMULATION RESULTS

The proposed LDO voltage regulator has been simulated with  $0.18\mu\text{m}$  CMOS technology. The compensation capacitor  $C_c$  is only  $3\text{pF}$ . The feedback resistors  $R_{fb1}$ ,  $R_{fb2}$  are  $30\text{k}\Omega$ ,  $60\text{k}\Omega$  respectively; the resistor  $R_F$  of the differentiator is  $100\text{k}\Omega$ ; the load resistors  $R_1$ ,  $R_2$  of the auxiliary amplifiers are both  $20\text{k}\Omega$ . The output voltage is  $1.8\text{V}$  while the reference voltage is  $1.2\text{V}$ .

##### A. Line regulation

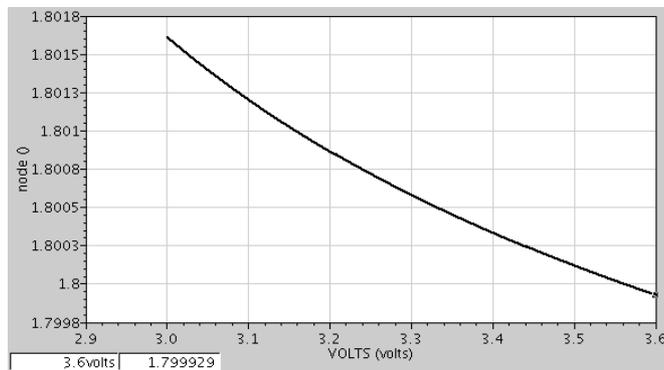


Fig. 4 Output voltage versus input voltage

The output voltage versus input voltage is presented in Fig. 4. The output voltage is around  $1.8\text{V}$  when the input voltage varies from  $3\text{V}$  to  $3.6\text{V}$ , with line regulation of  $1.68\mu\text{V}/\text{mV}$ .

##### B. Load regulation

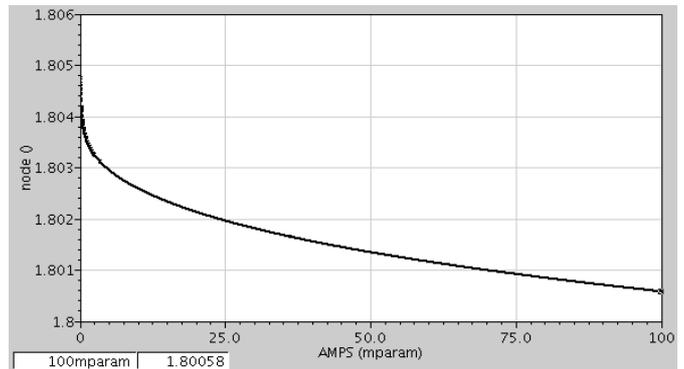


Fig. 5 Output voltage versus load current

The output voltage versus load current is presented in Fig. 5. The output voltage is around  $1.8\text{V}$  when the load current varies from  $0$  to  $100\text{mA}$ , with load regulation of  $30\mu\text{V}/\text{mA}$ .

##### C. Frequency response and phase margin

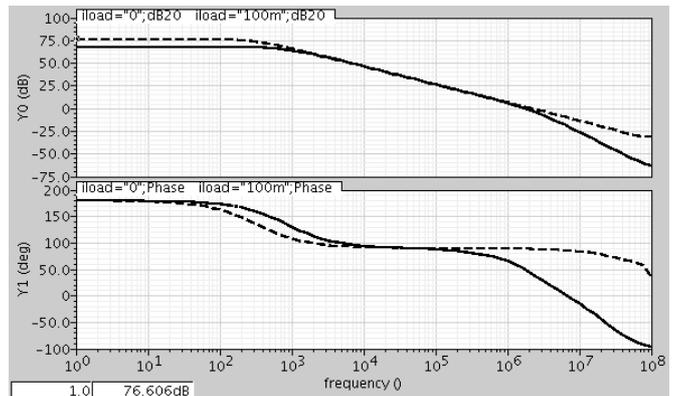


Fig. 6 Frequency response of the proposed LDO

(—solid for  $I_{load}=0$ ; ----dashed for  $I_{load}=100\text{mA}$ )

The frequency response of the proposed LDO is presented in Fig. 6 with the load current of  $0$  and  $100\text{mA}$ . The GBW is between  $1.77\text{MHz}$  and  $2.2\text{MHz}$ ; the phase margin is larger than  $50^\circ$ , the loop gain is around  $70\text{dB}$ .

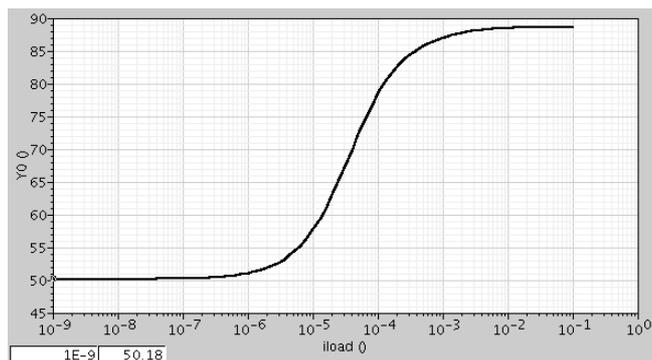


Fig. 7 Phase Margin under different load currents

Fig. 7 presents phase margin of the proposed LDO under different load current with 100pF output capacitor, simulation results validate the existence of single dominant pole within GBW. The minimum phase margin is always larger than 50° for the entire load current range, thus, the stability and transient characteristic of the closed loop can be guaranteed.

**D. Load current transient response**

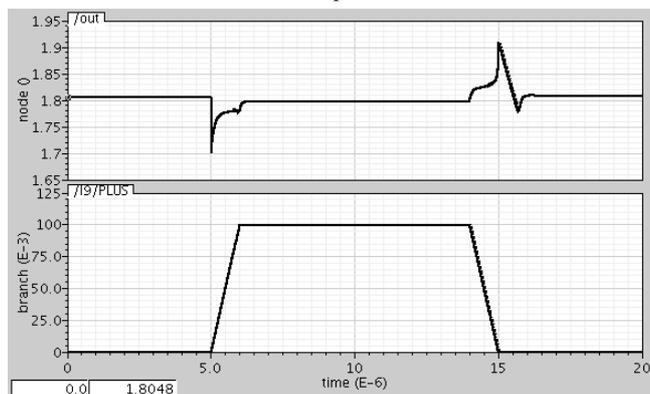


Fig. 8 Load current transient

The output voltage variations are 114mV and 112mV for load current transient from 0 to 100mA with 1μs rising and falling time as shown in Fig. 8.

**E. Power Supply Rejection**

The PSR character of different load currents shown in Fig.9 yields -50dB from DC to 40 kHz; -40dB at 151 kHz.

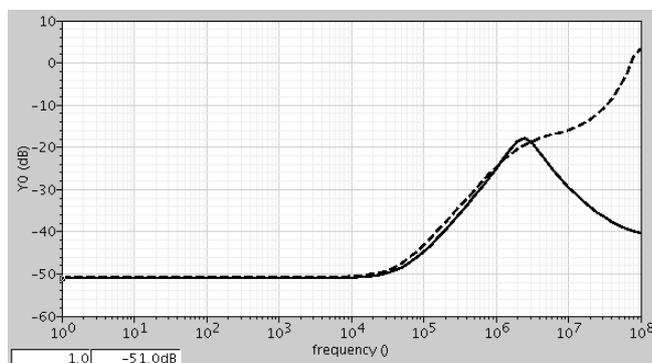


Fig. 9 PSR character

(—solid for  $I_{load}=0$ ; -----dashed for  $I_{load}=100mA$ )

**V. CONCLUSION**

A comparison among other output capacitor-less LDO voltage regulators [4], [5], [6] implemented in CMOS technology is summarized in Table 1. The proposed LDO voltage regulator presents faster settling and better PSR with only 3pF internal compensation capacitor.

TABLE I  
 PERFORMANCE SUMMARY

	[4]	[5]	[6]	This work
Year	2007	2007	2010	2011
$I_{out}(mA)$	50	100	100	100
$C_{com}(pF)$	21	6	7	3
Line regulation	1%	344 $\mu V/V$	57.4 $\mu V/mV$	1.67 $\mu V/mV$
Load regulation	2%	388 $\mu V/mA$	109 $\mu V/mA$	35.3 $\mu V/mA$
Transient peak(mV)	<90	<50	<100	<115
Settling( $\mu s$ )	15	$\approx 30$	<9	<3
PSR(dB)	-55@DC	NA	-40@10k	-50@DC -40@151k

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