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New Gate Stack Double Diffusion MOSFET Design to Improve the Electrical Performances for Power Applications

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***Abstract*—**In this paper, we have developed an explicit analytical drain current model comprising surface channel potential and threshold voltage in order to explain the advantages of the proposed Gate Stack Double Diffusion (GSDD) MOSFET design over the conventional MOSFET with the same geometric specifications that allow us to use the benefits of the incorporation of the high-k layer between the oxide layer and gate metal aspect on the immunity of the proposed design against the self-heating effects. In order to show the efficiency of our proposed structure, we propose the simulation of the power chopper circuit. The use of the proposed structure to design a power chopper circuit has showed that the (GSDD) MOSFET can improve the working of the circuit in terms of power dissipation and self-heating effect immunity. The results so obtained are in close proximity with the 2D simulated results thus confirming the validity of the proposed model.

***Keywords*—**Double-Diffusion, modeling, MOSFET, power.

I. Introduction

POWER field-effect transistors (MOSFETs) have been focus of interest both from applications and fundamental research point of views. Today, high-voltage MOS devices are extensively used in all kinds of integrated power circuits, like switch-mode power supplies, choppers, and power amplifiers [1]-[3]. As the MOSFET is biased with high voltages, the advantages of power MOSFET are diminished by the self-heating-effects [1]-[4].These effects lead to the working limitations on conventional planar MOSFETs. To overcome these limitations and realize high-performance MOS transistors, a new transistor called Double Diffused (DD) MOSFET has been proposed as potential candidate for power CMOS-based circuits' design [3,4]. But, the continued scaling of SiO2–based gate dielectrics leads to a large gate leakage and therefore, DD MOSFET performances can be degraded [3]-[5]. To minimize self-heating-effects and improve drain current, a new design and improvement of conventional DD MOSFETs become indispensable. In this work, a new design of DD MOSFET called gate stack (GS) double-diffused (DD) MOSFET, in which the gate leakage and self-heating-effects will be greatly improved, is proposed for the future power electronics circuits. In the proposed design, the average electric field under the gate further increases and the high density of interface hot-carrier at the drain end region can be reduced using the gate stack design.

The aim of this paper is to present an analytical model comprising channel potential and drain current in order to explain the advantages of the proposed (GSDD) MOSFET over the conventional DDMOSFET with the same geometrics specifications that allow us to utilize the benefits of the incorporation the high-*k* layer aspect on the immunity of the proposed design against the self-heating-effects. The results so obtained are in close proximity with the simulated results thus confirming the validity of the proposed model.

This paper is organized as follows. In section.2, we develop a compact analytical model for drain current based on surface potential aspect in order to analyse the device immunity against the self-heating-effect. In Section 3, we investigate the immunity of the DD MOSFETs with additional high-k layer (Gate Stack) against the self-heating-effect degradation. Moreover, the implementation of the proposed design into circuits' simulator allows us to analyse the impact of the proposed approach on the performances of the power electronic circuits. The conclusions will be drawn in Section 4.

II. Modeling Methodology

In Fig.1 a cross section of a high-voltage GSDD MOSFET is given. The-well bulk is diffused from the source-side under the gate (G), and thus forms a graded channel region. The internal-drain *Di* represents the point where the graded channel turns into the lightly doped region. With the gate extending over the drift region, an accumulation layer forms in the drift region underneath the gate oxide. Therefore, above the threshold voltage of the channel region, electrons flow through an inversion channel from the source toward the drain terminal at the end of the drift region. The structure has a double-layer gate stack, oxide and high-k layers, the effective oxide layer thickness of insulator layer toxeff is given by the superposition of the thickness of the SiO_2 layer t1 with permittivity ε_1 and the thickness of the high-k layer *t2* having permittivity *ε2* as follows,

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$$t_{oxeff} = t_1 + (\varepsilon_1 / \varepsilon_2) t_2 \quad (1)$$

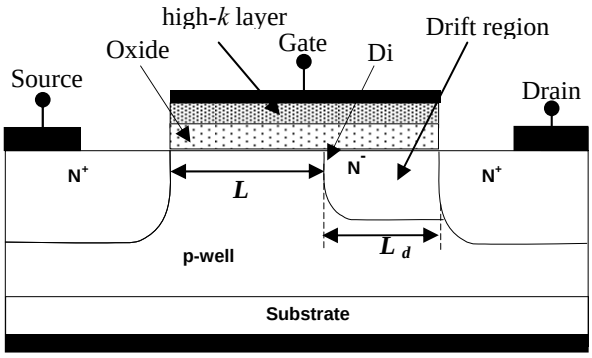


Fig. 1 Cross section of the GSDD MOSFET investigated in this work.

In the analytical modeling approach, expressions for the current through the inversion channel, I_{ch}, as well as for the current through the drift region, I_{dr}, should be derived in order to develop our drain current model as function of the internal-drain *Di* . This internal-drain voltage is expressed explicitly in terms of the external terminal voltages. The expression for this internal drain voltage is derived by equating I_{ch} to I_{dr}. Next, the internal drain voltage is used to calculate the surface potentials, in which the final drain current is formulated. In this way, I_{ds} is surface-potential based and it is explicitly expressed in terms of the external terminal voltages and fitting parameters which will be calculated using genetic algorithm approach.

The channel current for DD MOSFET is expressed as [6]-[8],

$$I_{ch} = \frac{W \mu_{ch} C_G}{L_{ch}} (V_{inv0} - 0.5\zeta \Delta\psi_s + \zeta V_{th}) \Delta\psi_s \quad (2)$$

where, W is the gate width, μ_{ch} represents the electron mobility in the channel, $C_G = \varepsilon_1 / t_{oxeff}$ is the gate capacitance per unit area, V_{inv0} represents the inversion voltage per unite area at the source side. The parameter ζ reflects the variation of inversion charge in the channel region with surface potential. $\Delta\psi_s = \Psi_{sL} - \Psi_{s0}$ is the surface potential drop across the channel region (difference between the surface potential at internal-drain point and source-side one) , and V_{th} represents the thermal voltage.

Velocity saturation in the channel is calculated for by taking the mobility μ_{eff}^{ch} equal to

$$\mu_{ch} = \frac{\mu_{eff}}{1 + \alpha_3 \Delta\psi_s} \quad (3)$$

where μ_{eff} is the effective electron mobility in the channel, $\alpha_3(\alpha_1, \alpha_2) = \mu_0^{ch}(\alpha_1, \alpha_2) / (L_{ch} v_{sat}(\alpha_1, \alpha_2))$ represents the model parameter which describes the velocity saturation in channel region, with μ_0^{ch} the low field electron mobility in the channel and v_{sat} represents the saturation electron mobility. It is to note that the model parameters α_3, α_1 *and* α_2 are calculated using genetic algorithm technique, in which the fitness function is defined as,

$$f = \frac{1}{M} \sum_{V_{ds}} \sum_{V_{gs}} \left[\frac{I_{ds,NUM} - I_{ds,ANA}}{I_{ds,NUM}} \right]^2 \quad (4)$$

where f is the fitness value; $I_{ds,ANA}$ is the predicted drain current based on analytical computation; $I_{ds,NUM}$ represents the target function (numerical results based on 2-D numerical simulation [9]); and M represents the number of samples (database size). It is aimed to minimize this fitness function in order to improve the accuracy of the analytical drain current model for GSDD MOSFETs.

In the linear working regime, the drift current I_{dr} is expressed as,

$$I_{dr} = \frac{W \mu_{acc}}{L_d} \int_{V_{Di}}^{V_D} (-Q_{acc}^{dr}) dV_C + \frac{W \mu_{dr}}{L_d} \int_{V_{Di}}^{V_D} (-Q_b^{dr}) dV_C \quad (5)$$

where the first term of (5) represents the current through the accumulation layer, and the second one the current through the bulk. μ_{acc} is the electron mobility through the accumulation layer, while μ_{dr} is that through the bulk. In addition, Q_{acc}^{dr} and Q_b^{dr} represent the charge per unit area in the accumulation and bulk regions, respectively. V_C is the channel voltage in drift region.

An approximate computation of (5) is given by as,

$$I_{dr}(\theta_1, \theta_2, \theta_3) = \frac{f_{lin}(\theta_1, \theta_2, \theta_3)}{R_D} V_{DDi} + \frac{W \mu_{acc}(\theta_1, \theta_2, \theta_3) C_G}{2 L_d} ((V_{accDi})^2 - (V_{accD})^2) \quad (6)$$

where V_{accDi} and V_{accD} represent the voltage value at internal drain point and drain side, respectively. R_D is the on-resistance in drift region, the parameters θ_i are the fitting parameters can be extracted using genetic algorithm technique (4).

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In order to derive an explicit analytical model of drain current, the expressions for drain current in the channel and drift regions are obtained separately. These expressions are then equated and simplified to obtain a second order polynomial for the channel current in terms of the unknown internal drain potential V_{Di} (under the imposed constraint ($0 \le V_{Di} \le V_{ds}$)), and the solution of this latter equation for V_{Di} is explicitly expressed in terms of the external applied voltages.

III. Results and Discussions

In this section, the accuracy and various properties of the DD and GSDD MOSFETs current model will be studied and analyzed by comparing the obtained results with 2D numerical simulations in order to show the effect of the induced high-*k* layer on the improvement of the device performances in terms of drain current values and self-heating-effects immunity.

The obtained analytical and numerical *I-V* characteristics of DD and GSDD MOSFETs with are given in Fig.2. It can be seen that GSDD design has higher current as compared to DD device and the analytical results are found to be in close agreement with the simulated results. This increasing in drain current can be explained by the effect of the introduced high-*k* layer on the limitation of oxide tunnel current and the improvement of the gate-channel controllability. Moreover, the self-heating-effect degradation becomes more apparent when the applied gate voltage is increased to higher values. In this case, it clear shown that a great immunity against this degradation has been observed for GSDD design. Therefore, the GSDD MOSFET brings prominent advantages in terms of immunity against the self-heating-effect degradation and delivered drain current compared to DD MOSFETs.

In order to show the impact of our proposed design, we propose the simulation of the power chopper CMOS circuit, which is considered as an important device for power electronics applications. However, as the CMOS technology enters the high power regime, nonlinear effects and self-heating-effect degradation become more and more important and consequently an improvement of thermal behavior of a DD MOSFET is necessary. In this study, using the developed analytical models, we have simulated a power chopper CMOS circuit. The purpose of this simulation is to study the evolution of the output voltage as function of transistor design. The power chopper CMOS circuit consists of four GSDD MOSFETs (Fig. 3). The output voltages characteristics of the power chopper were predicted using the implemented analytical models into simulator library as it is shown in Fig. 4. It is clear that an improvement of the output voltage has been recorded in the case of GSDD MOSFET-based chopper.

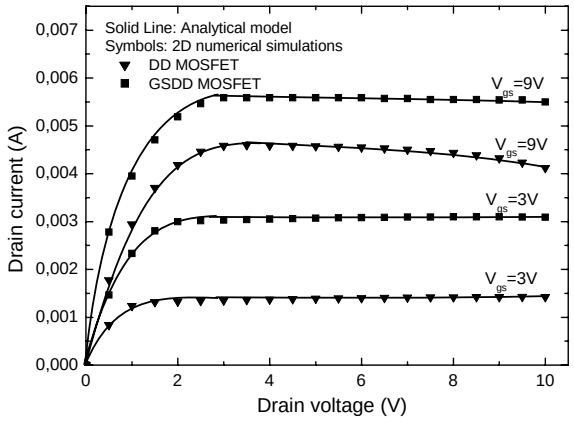


Fig. 2 I_{ds}-V_{ds} characteristics of the DD MOSFET including self-heating- effects for both designs: with and without high-k layer (t_1=15nm, L=0.8µm, L_d=0.8µm, t_2 = 15nm and W=17 µm).

This improvement can be explained by the high electrical performances (high drain current, low ON-resistance, self-heating immunity,…) of our proposed design.

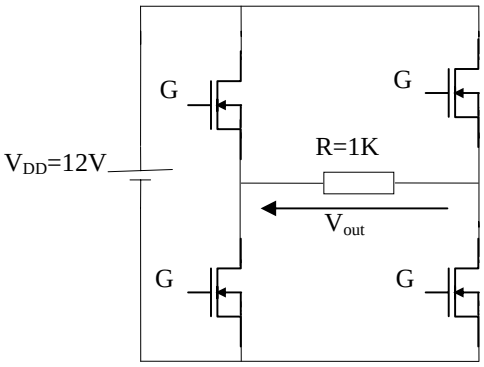


Fig.3 Circuit diagram of the GSDD MOSFET-based chopper.

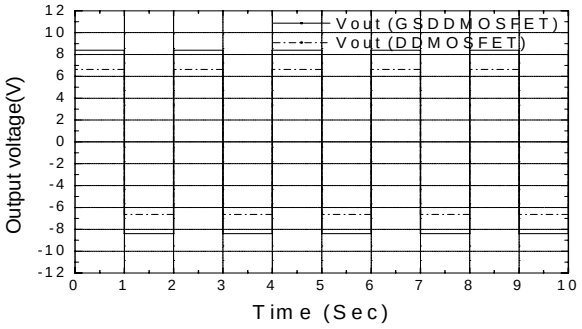


Fig. 4 Pspice output signals for both designs: DD MOSFET and GSDD MOSFET-based choppers.

IV. Conclusion

In this paper, a new design of DD MOSFET by introducing of high-*k* layer is presented. The performances of the proposed design were compared to the conventional DD MOSFET, illustrating the superior performance of the proposed design with respect to the conventional DD MOSFET in terms of thermal behavior and electrical performances. The encouraging obtained results have indicated that the proposed design is particularly suitable to be incorporated into electronic devices simulators to study and improve the CMOS-based circuits for power electronics applications.

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