

A Software-Supported Methodology for Designing General-Purpose Interconnection Networks for Reconfigurable Architectures

Kostas Siozios, Dimitrios Soudris and Antonios Thanailakis

Abstract—Modern applications realized onto FPGAs exhibit high connectivity demands. Throughout this paper we study the routing constraints of Virtex devices and we propose a systematic methodology for designing a novel general-purpose interconnection network targeting to reconfigurable architectures. This network consists of multiple segment wires and SB patterns, appropriately selected and assigned across the device. The goal of our proposed methodology is to maximize the hardware utilization of fabricated routing resources. The derived interconnection scheme is integrated on a Virtex style FPGA. This device is characterized both for its high-performance, as well as for its low-energy requirements. Due to this, the design criterion that guides our architecture selections was the minimal Energy×Delay Product (EDP). The methodology is fully-supported by three new software tools, which belong to MEANDER Design Framework. Using a typical set of MCNC benchmarks, extensive comparison study in terms of several critical parameters proves the effectiveness of the derived interconnection network. More specifically, we achieve average Energy×Delay Product reduction by 63%, performance increase by 26%, reduction in leakage power by 21%, reduction in total energy consumption by 11%, at the expense of increase of channel width by 20%.

Keywords—Design Methodology, FPGA, Interconnection, Low-Energy, High-Performance, CAD tool.

I. INTRODUCTION

FIELD Programmable Gate Arrays (FPGAs) have become the key implementation medium for the vast majority of digital circuits designed today. This makes the field of FPGA architecture even more important, as there is a stronger demand for faster, smaller, cheaper and lower-energy programmable logic.

Due to its programmability features, FPGA technology offers design flexibility which is supported by quite mature

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commercial [10, 11] and academic [2, 5, 6, 18] design flows. Moreover, the FPGA logic characteristics and capabilities have changed and improved significantly in the last two decades, from Look-Up tables (LUT) with same size to devices that integrate numerous hardware blocks (i.e., Look-Up tables with different size, microprocessors, DSP modules, RAM blocks, etc.) onto the same chip [10, 11]. In other words, the part of the FPGA architecture that implements application logic, changed gradually from a homogeneous and regular architecture to a heterogeneous (or piece-wise homogeneous) and piece-wise regular architecture.

However, this trend is not affect the interconnection network, which still consists by horizontal/vertical wires and Switch Boxes (SBs) that provide communication among the logic modules. This uniformity on interconnection resources across the FPGA leads to waste on delay, energy and silicon area, as the designs do not fully utilize them (there are no uniform connectivity demands across the device).

In addition to that, most of the commercial FPGAs have a number of devices in each family. Traditionally, the upcoming device of each family includes more logic elements compared to the previous ones. If the available hardware resources are not enough to implement the applications functionality, then a greater device from the same family can be chosen. On the other hand, this solution is not possible whenever a device with higher interconnection demand is required. In most of these cases, the designer has to choose an FPGA from another family (or vendor), which forces him to face a number of additional design problems. In other words, larger FPGAs are made simply by integrating more slices on a larger die. However, creating larger FPGAs do not improve significantly the interconnection of the device (there is no connectivity improvement). As the FPGAs are built for the worst-case routing scenario (fixed routing channel width), the availability of interconnection resources is a critical issue for effective application implementation.

Platform-based design allows the designer to build a customized FPGA architecture, using specific blocks, depending on the application domain requirements. The platform-based strategy changed the FPGA's role from a "general-purpose" machine to an "application-domain" machine, closing the gap with ASIC solutions. Such architectures might be though as alternatives to Structured-ASIC [22].

Due to the fact that about 70-90% of a typical FPGA is occupied by routing resources [8], many researchers have

spent significant effort on minimizing their impact to the device performance [4, 8, 12, 13, 15, 16, 20, 21]. The developed techniques aim to reduce the energy consumption in the whole device and/or to achieve higher operation frequencies, ignoring the spatial info regarding the connectivity demands. Among others, the design of non-homogeneous interconnection structure [15, 21] and the use either of multiple supply voltages, V_{DD} , or multiple threshold voltages, V_{th} , [13, 16, 20] are the main strategies which have been chosen. In other words, the energy consumption of the routing structure is the dominant energy component of the total energy. For instance, the Xilinx Virtex-II family consumes 50-70% of its total energy in the interconnection network, whereas the rest is consumed by the clock, the logic modules and the I/O blocks [17]. Furthermore, the integration technology advances imply that the role of interconnects becomes more dominant, since the interconnection characteristics scale faster than linearly in device gate capacity. In other words, more routing resources per logic module are needed.

The basic building blocks of a typical FPGA interconnection network are the wire segments and the Switch Boxes (SBs). Due to the fact that the wires exhibit higher resistance/capacitance values than the SBs, the proposed methodology targets first to minimize the impact of wire segments to the device performance and secondly to improve additionally this performance through efficient SBs selection. Implementing FPGAs in a deep-submicron technology, the leakage power becomes a dominant power component with equal importance to the dynamic power consumption [5]. Thus, we study both the total power/energy consumption, as well as the leakage power.

In this paper, we propose a novel methodology for designing a general-purpose interconnection structure for reconfigurable architectures. For evaluation purposes, this network was integrated into a Virtex-based FPGA [14]. The applications mapped onto the derived platform achieve high operation frequency and low-energy requirements. In order to design such an interconnection architecture, we have to find the appropriate wire length as well as the associated combination of multiple SB patterns, taking into account the spatial and statistical characteristics that introduced by the Placement and Routing (P&R) algorithms.

The alternative segment wires that employed in the exploration procedure of the proposed methodology are designed with the 0.18 μ m STM technology. The differences between them affect their length, as well as the spatial position over the reconfigurable architecture that assigned. Similarly, for the multiple SB pattern combination we employ three SBs, namely Subset, Wilton and Universal [1]. We select these because they are widely-used and they can be supported by the *EX-VPR* tool [2, 6, 9]. Additional segment wires and/or SB patterns can be found in relevant references, resulting into a more efficient interconnection architecture. However, the primary goal of this paper is to prove that a combination of properly-chosen hardware routing resource, i.e., segment wires and SB patterns, results into reduced delay and energy consumption, and not to find which combination among all existing is the optimal choice.

The efficiency of a wire segment and SB pattern is evaluated by analyzing parameters such as energy consumption, performance, and the minimum number of routing tracks for successful P&R. We made an exhaustive exploration with a representative number of benchmarks [3] (i.e., combinatorial, sequential, and FSM), to find out the appropriate interconnection architecture for minimizing the Energy \times Delay Product (EDP) of a Virtex based FPGA. Among others, we study the statistical and spatial info regarding the utilized routing resources, as well as their impact on the applications maximum operation frequency and the energy consumption for Virtex devices. Based on these conclusions we propose a new heterogeneous interconnection scheme composed by appropriately selected and assigned (to different parts of the device) segment wires and SB patterns.

Having EDP as a selection criterion, we made exploration both for different wire segment lengths and SB patterns combinations, as well as different assignment over the reconfigurable device. Throughout this paper, we prove that the best suited wire segment distribution is the L_1 & L_2 (L_1 means that each routing wire spans only one slice, whereas the L_2 tracks spans two slices). Similarly, the derived SB pattern combination is the "Subset-Universal", as this exhibits the smaller EDP value.

The main contributions of in this work can be described as follows:

- Study the connectivity constraints introduced by the P&R algorithms.
- 3D visualization for the design parameters (i.e., connectivity, energy) of each (x,y) point of an FPGA.
- Introduction of a general-purpose heterogeneous interconnection network for reconfigurable architectures consisted of multiple segment wires and SB patterns.
- Development of novel software tools for supporting and validating the design of heterogeneous FPGAs.

The paper is organized as follows: In Sections II and III the proposed methodology and the connectivity requirements of Virtex FPGAs are described, respectively. The introduction to heterogeneous interconnection network is discussed in Section IV. Section V and VI gives detail information regarding the selection procedure of the segment wires and the SB patterns combination that form the enhanced interconnection network, whereas Section VII presents the comparison results. The main conclusions are summarized in Section VIII.

II. THE PROPOSED DESIGN METHODOLOGY

The proposed methodology for designing an efficient interconnection architecture in terms of delay and energy consumption consists of five steps, as shown in Fig. 1:

- Step 1) Place and Route (P&R) a representative number of applications (i.e., combinatorial, sequential, and FSM) from [3] onto Virtex style FPGAs.
- Step 2) Visualize the results of Step 1 in order to study the interconnection demands implied by the P&R algorithms. Even though, different applications might have different connectivity constraints, the hardware utilization mainly depends on the chosen P&R algorithms.

- Step 3) After the appropriate exploration, define the suitable wire segment distribution in each routing channel.
- Step 4) Given the segments from former step, define the combination of SB patterns across the device.
- Step 5) Based on the previous results regarding the segment wires and SB patterns, build the proposed general-purpose heterogeneous interconnection architecture.

For demonstration purposes, the derived heterogeneous interconnection is integrated within a Virtex FPGA. In order to measure the efficiency of the proposed interconnection architecture, each of the applications is mapped onto two different FPGA devices. These mappings have identical placement, however, the routing of them differs. More specifically, the re-routing procedure is necessary because the employed timing-driven router by the *EX-VPR* tool needs application re-routing in order to make appropriate delay-oriented decisions when forming connections between logic blocks. Detailed description of each step, as well as the exploration and evaluation results for the proposed interconnection scheme will be given in the upcoming Sections.

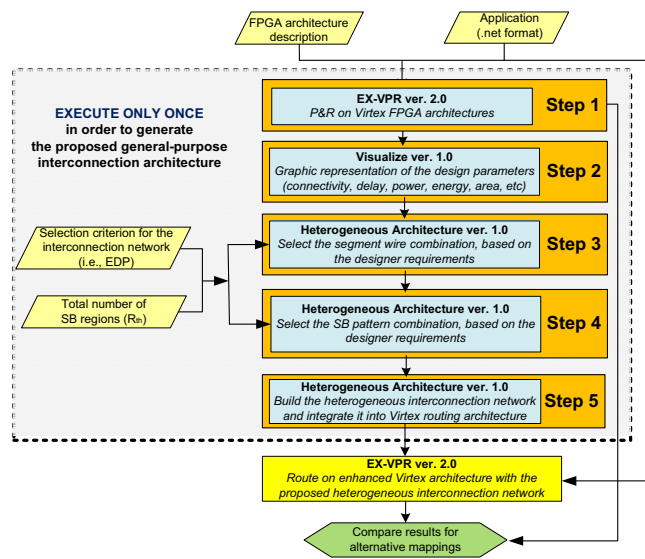


Fig. 1 Design methodology for realizing the proposed general-purpose interconnection network

In order to design/evaluate the proposed methodology, three new CAD tools (part of the *MEANDER* design framework [6]) have been developed (*Visualize*, *Heterogeneous Architecture* and *EX-VPR*). More specifically, the *Visualize* calculate and visualize the P&R results derived by application mapping, whereas the *Heterogeneous Architecture* builds the proposed heterogeneous interconnection network, composed from multiple hardware routing resources (i.e., wire segments and SB patterns) placed together in the same device. The third tool, named *EX-VPR*, place and route (P&R) applications to the enhanced (with the proposed interconnection architecture) Virtex FPGA. The *MEANDER* flow is available for on-line execution, through [6], for non-commercial use.

III. VISUALIZE THE SPATIAL INFORMATION FROM PLACEMENT AND ROUTING

The first step of the methodology is to extract and visualize the proper data related with the spatial distribution of connectivity demands for Virtex FPGAs, considering the MCNC benchmarks. Particularly, by the term *connectivity* we define the total number of active connections, i.e. the “ON” pass-transistors, which actually form connections inside a SB. A specific map (or set of curves) can be created for this design parameter, depicting the connectivity variation across the (X,Y) -plane of the FPGA device.

Fig. 2 shows this connectivity variation in normalized values. The picture of this graph is identical to the applications functionality, whereas it depends solely on the chosen P&R algorithms [1, 5, 19]. However, similar 3D graphs can be derived for any application-domain (i.e., image processing) or for a class of applications (i.e., motion estimation). Fig. 2 proves that the connectivity varies between two arbitrary (x_1, y_1) and (x_2, y_2) points of an FPGA and the number of used pass-transistors (i.e., ‘ON’ connections) decreases gradually from the center of FPGA architecture to the I/O blocks. On other words, the interconnection resources are not utilized uniformly over any (x,y) point of FPGA. Consequently, the challenge, which should be tackled by a designer, is to choose effectively the actually-needed routing resources, considering the associated spatial information from the P&R algorithms. Thus, employing the appropriate amount of hardware, significant energy consumption, leakage and delay reduction can be achieved.

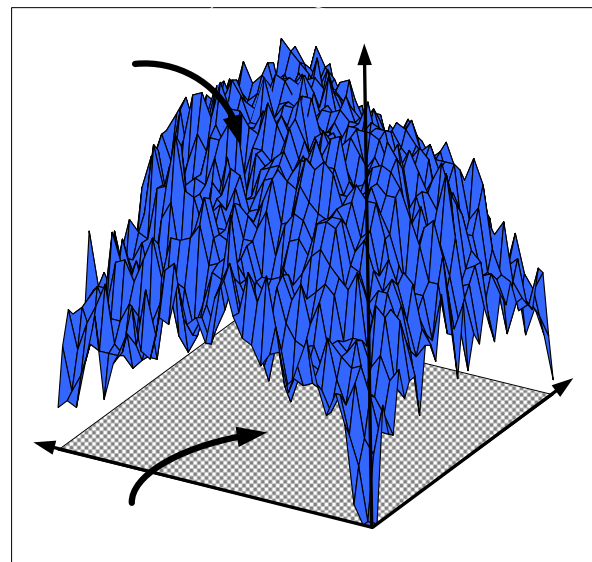


Fig. 2 Connectivity demands across the whole FPGA

We have to mention that in order to derive the upcoming graphs, we employ numerous applications (with floor-planning) from [3], appropriately connected, in order to cover as much as possible the Virtex FPGA. Almost all the existing FPGA devices are supported by dedicated P&R algorithms that maximize their performance. For the interconnection scheme proposed in this paper, the employed P&R algorithms

have mapping constraints, as they are shown in Fig. 2. However, depending on the chosen P&R algorithms, different regions of the device may exhibit higher (or lower) connectivity demands compared to the rest device.

Additionally, a second important conclusion is drawn from Fig. 2. Although a Virtex FPGA exhibits a homogeneous and regular interconnection architecture (i.e., just repetition of routing wires and SBs), the actually-utilized hardware resources provide a non-homogeneous and irregular picture. Ideally, we had to employ different interconnection fabric at each (x,y) point of the FPGA, which would lead to a totally irregular device increasing, among others, the NRE fabrication costs. However, such “*extreme*” architecture is the optimum solution for an application-domain specific FPGA, but apparently it is not a practical and cost-effective implementation for any class of applications (e.g., DSP). Instead of this, we propose a piecewise-homogeneous interconnection architecture, consisting of a few homogeneous regions.

Considering a certain threshold of the connectivity value, R_{th} , and projecting the 3D diagram to (X,Y) -plane of the FPGA, we can derive maps which depict the corresponding connectivity requirements. Assuming $R_{th}=2$ and $R_{th}=3$, Fig. 3(a) and (b) quantizes the applications connectivity requirements, mapped on Virtex FPGAs, in two and three regions, respectively. Each of these regions is supposed to have different interconnection architecture (i.e., routing channel width, SB pattern, etc). In these graphs, the different colors show regions with different interconnection demands. The values in Z-axis are normalized over the maximum connectivity value that appears on the device. For instance, the SBs placed on *Region₁* of Fig. 3(a) have connectivity values that range between 0% and 50% of the maximum connectivity value of the device, whereas the SB connectivity value for *Region₂* ranges between 50% and 100%, respectively. The number of distinct regions is based on the design tradeoffs. By increasing this value, the FPGA becomes more heterogeneous, since it consists of several regions. On the other hand, this increase leads to performance and energy improvement for the device, due to the better routing resource utilization.

The energy consumption is a critical issue of modern FPGA designs. Due to this, the proposed interconnection network aims at energy savings through efficient selection of segment wires and SB patterns, based on the actual connectivity demands. Thus, in regions with smaller connectivity demands (i.e., *Region₁*) we can use the appropriate combination of routing wires and SB patterns which results into reduced energy consumption. The connectivity degree of (x,y) point of FPGA array is straightforward-related with the energy consumption of (x,y) location, since less active SB connections means smaller resistance/capacitance and thus, less energy consumption. Fig. 4(a) and 4(b) depicts the energy consumption of interconnection network for a Virtex like FPGA device with two and three regions, respectively. The corresponding estimations of energy consumption are provided by the models presented in [7]. The introduction of the energy consumption map is a very useful instrument to FPGA device designers in order to specify the energy requirements over each (x,y) point of the FPGA.

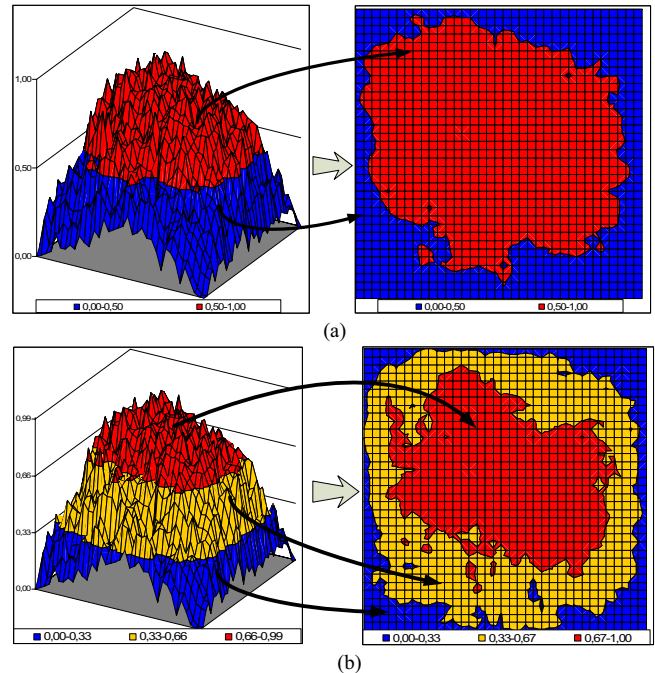


Fig. 3 Connectivity requirements for (a) two and (b) three regions

Determining the “*hotspot*” locations of the FPGA, the designer can concentrate his/her efforts in the reduction of the energy consumption of certain regions only, but not on the whole device, thus reducing among others the design-time costs and alleviating the time-to-market pressure. Comparing the maps that depict the connectivity (Fig. 3(a) and 3(b)) with the energy consumption of the interconnection resources (Fig. 4(a) and 4(b)), it can be easily concluded that these are quite similar, due to proportional relationship between the connectivity degree and the energy consumption.

Depending on the chosen class of applications used for the visualization, we can derive alternative FPGA architectures. More specifically:

- a) Performing exploration with *all* type of applications (i.e., combinatorial, sequential and FSM), the derived 3D graphs provide a global view of (almost) all possible applications, which can be mapped on an FPGA. Therefore, the proposed heterogeneous architecture with the spatially-varied routing features can be considered as a general-purpose FPGA platform.
- b) Visualizing the spatial information of a certain application domain, such as DSP applications and block matching algorithms [19], we can derive an application-domain specific FPGA platform which is specialized and optimized under a set of specific constraints.
- c) Depending on the fabrication costs and the volume number of chips, the proposed methodology may be used for the description of an FPGA architecture optimized for a specific application only, for instance, MPEG-2. This option might be considered as an alternative solution to Structured-ASICs [22].

Here, we provide comparison results assuming the FPGA architecture as a general-purpose platform (i.e., option (a)).

Regarding with the second choice, extensive comparison results for the DSP applications can be found in [19]. The last choice will be studied in the near future.

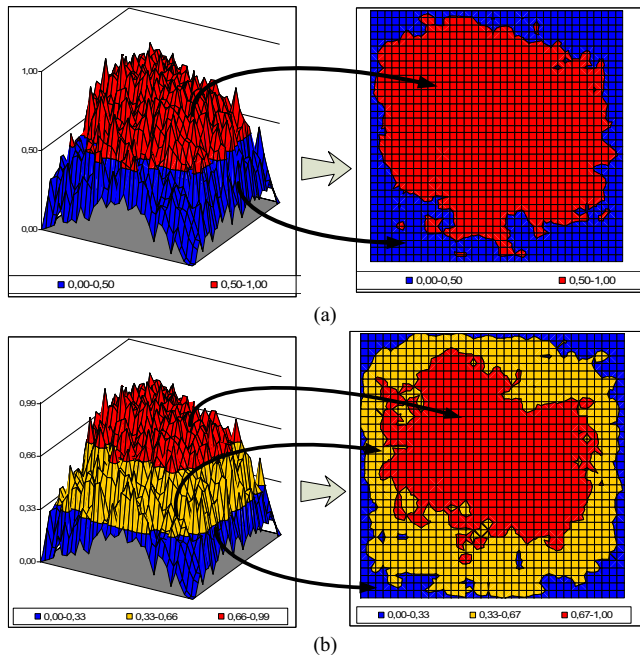


Fig. 4 Energy consumption of interconnection network (a) for two regions, (b) for three regions

The next two Sections describe the exploration and the selection procedure of the appropriate segment length and SB pattern combination, in terms of various design parameters. In order to evaluate these parameters, the proposed heterogeneous interconnection network is integrated into a Virtex-style FPGA. Since our major objective is the design of a high-performance and low-energy routing architecture, we adopt the well-known Energy×Delay Product (EDP) criterion for these design steps. For the rest of the paper, we use $R_{th}=2$.

IV. DEFINING MULTIPLE REGIONS ON THE FPGA

The spatial interconnection utilization and power distribution results from Fig. 3 and 4 steer us to divide the FPGA into a number of regions, each of which has different interconnection fabric. As the target architecture balances the performance with energy requirements, the hardware resources are classified in regions based on the EDP value. This value is calculated for each slice placed on spatial location (x,y) of the device grid. Given the total number of distinct regions as input, the proposed methodology finds the minimum (EDP_{min}) and maximum (EDP_{max}) EDP values for each region. For every $slice(x,y)$ placed on (x,y) that belongs to $Region_k$, we have:

$$EDP_{Region_k _min} \leq EDP(x,y) \leq EDP_{Region_k _max} \quad (1)$$

As we mentioned previously, our proposed interconnection architecture is composed by two Regions ($R_{th}=2$). Employing Eq. (1) in such architecture, we obtain the quantization criterion for the hardware as follows:

$$EDP_{min} \leq EDP_{Region1} \leq EDP_{R_{th}=2} \leq EDP_{Region2} \leq EDP_{max} \quad (2)$$

where $EDP_{Region1}$ and $EDP_{Region2}$ denotes the EDP values for slices that belong to $Region_1$ and $Region_2$, respectively. The EDP_{min} and EDP_{max} is the minimum and maximum EDP values, respectively, over the whole device, whereas the $EDP_{R_{th}=2}$ corresponds to border value (i.e., criterion) between the two regions.

In order to describe the proposed heterogeneous FPGA, we introduce a new term, $Area_Region_k$, which describes the percentage of silicon area of the k -th region over the whole FPGA. The mathematic expression is:

$$Area_Region_k = \frac{Number_of_slices_in_Region_k}{Total_number_of_slices_into_FPGA} \quad (3)$$

where $k=1,2, \dots, R_{th}$ defines the total number of distinct device regions, $Number_of_slices_in_Region_k$ is the number of slices that belong to $Region_k$, $Total_number_of_slices_into_FPGA$ corresponds to the total number of slices on the device (it is equal to $M \times M$), $Area_Region_k$ denotes the percentage of area coverage of $Region_k$ over the whole device, whereas

$$\sum_{k=1}^{R_{th}} Area_Region_k = 1.$$

As we mentioned previously, different regions have different routing resources, providing among others different connectivity efficiency, performance and energy consumption.

Fig. 5 shows the proposed heterogeneous FPGA architecture with multiple SB interconnection architecture. This figure illustrates the idea of combining more than one segment wires and SB patterns simultaneously onto the same device, leading to different connectivity efficiency across the FPGA. For illustration purposes, a 5×5 FPGA is considered. The innermost region of such a device is designated as $Region_2$, whereas the outermost belongs to $Region_1$. In this example, the area coverage of $Region_2$ is equal to $\frac{4}{36}$ and the

$Region_1$ covers the rest $\frac{32}{36}$ of the FPGA. Moreover, having a

combination of two regions with percentage of area coverage $Area_Region_1$ and $Area_Region_2$, respectively, then the foregoing region is assigned to the center of the FPGA ($Region_2$), whereas the latter region is assigned to the remaining part of FPGA ($Region_1$).

The number of distinct regions is based on the design tradeoffs. By increasing this value, the FPGA becomes more heterogeneous (as it incorporates more segment wires and SB patterns), allowing the specification of the connectivity requirements, in more detailed manner (better routing resource utilization) at the expense of the increased fabrication cost. To the best of our knowledge, no one up to now has proposed FPGA architecture with both multiple segment wires and SB patterns placed simultaneously on the same device, based on the spatial restrictions introduced by the P&R algorithms. During the exploration procedure, we found that the increase of R_{th} value more than 3 leads to negligible gains in device efficiency.

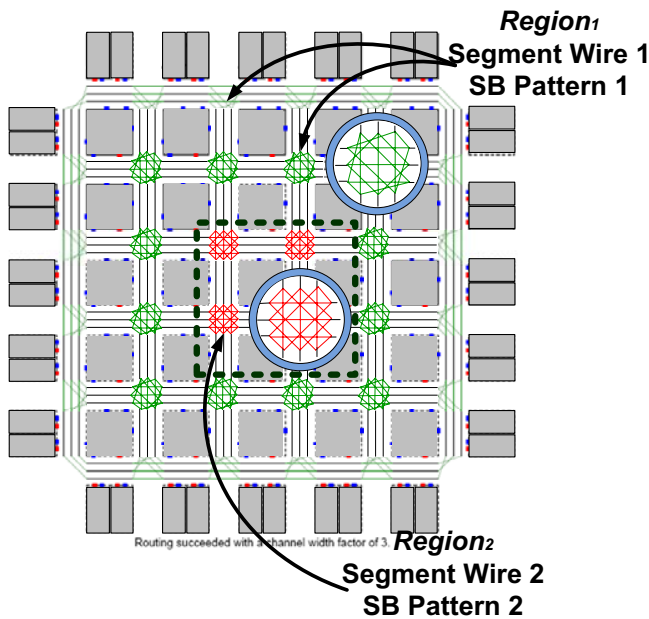


Fig. 5 A 5x5 FPGA array composed from two regions with different routing resources

V. COMBINATION OF MULTIPLE SEGMENT WIRES

The routing resources that dominate the FPGA performance and energy consumption are the wire segments and the SBs. Since the wires exhibit higher values for resistance/capacitance compared to SBs, firstly we have to define the appropriate wire length distribution for a Virtex-style FPGA.

In this paragraph the impact of different routing wire lengths is explored under numerous design parameters, as it is shown in Fig. 6. More specifically, we plot the variation of application delay, leakage power, energy consumption, minimum required silicon area, as well as the EDP parameter over different wire distribution across the device. The horizontal axis of Fig. 6 shows the alternative segment wire lengths, whereas the vertical one corresponds to the normalized value of each design parameter. A segment length (i.e., L_2) indicates how many slices are spanned by a wire. Also, whenever an interconnection architecture consists by more than one segment wires (i.e., L_1 & L_2), then half of the device (in the center of the FPGA) has segments with length L_1 , whereas the second half of the FPGA (in the device periphery) forms connections with segment wires L_2 .

Some conclusions are drawn from Fig. 6. First of all, the interconnection network that contains long segments (e.g., L_8) exhibit increased values for all the design parameters, compared to the rest solutions. This occurs as such a network, in order to form connections between logic elements (even for adjacent blocks), needs to employ long wires, increasing among others the interconnection resistance/capacitance, leading in turn to increased delay and energy consumption.

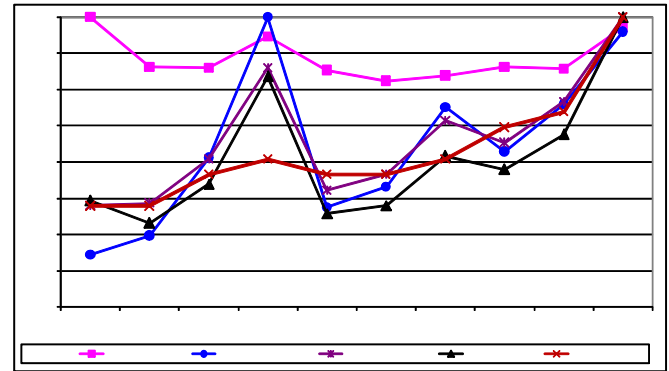


Fig. 6 Segment length exploration in terms of delay, leakage power, energy, EDP and silicon area

Also, the delay (i.e., maximum operation frequency) exhibits similar results for (almost) all the segment combinations, except for these that contain length L_8 . Moreover, as the segment length increases, the static power consumption (i.e., leakage power) and the silicon area increase almost linearly. Our selection criterion for the interconnection network is the minimal EDP value. Based on the curves shown in Fig. 6, the L_1 & L_2 solution exhibits the smaller EDP value. Based on this, in the part of device which exhibits low-connectivity demands (*Region₁*) we assign the segments with length L_2 , whereas in the rest part of the interconnection network (*Region₂*) we have L_1 wires.

More efficient combinations of routing wires (i.e., additional segment lengths, ratio, etc.) can be found in relevant bibliography [1, 5, 8, 12]. However, this step of the proposed methodology (Fig. 1) allows to the designer to build a full-custom wire distribution, composed by multiple segments, based on the statistical/spatial demands introduced by the P&R algorithms.

Up to now we study the routing wires of the interconnection architecture. Next section gives detailed description regarding with the forth step of the proposed methodology, which is about the selection of the appropriate combination of SB patterns under the EDP criterion.

VI. COMBINATION OF MULTIPLE SWITCH BOXES

As described above, we design an efficient routing structure in terms of EDP by controlling the interconnection capacitance over the different FPGA regions. Employing the spatial information of a SB location, this section provides detailed data regarding with the selection procedure of the optimal combination of multiple SB patterns.

A. Characterization of alternative SB patterns

Even though numerous non-square SBs were proposed [1, 5, 12], we choose to use square SBs with W tracks on each side and $F_s=3$, as this leads to better routing resource utilization for devices composed by more than one region. Also, although non-square SBs might be useful for some application domains, however, square blocks lead to more area-efficient interconnect fabric.

The connections among routing tracks into SB can be defined by the *permutation mapping function* between each

pair of sides. Fig. 7 shows the different mapping functions, as well as their forward direction.

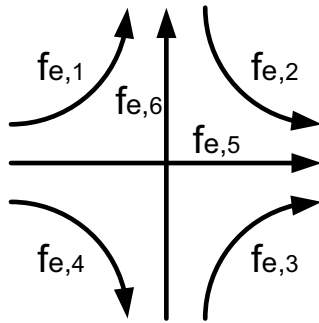


Fig. 7 Switch box mapping functions

Here, $f_{e,i}(t)$, or simply $f_{e,i}$, represents the mapping function for an endpoint turn of type i . A switch connects the wire originating at track t on one side to track $f_{e,i}(t)$ on the destination track. In the reverse direction to those indicated are represented as $f_{e,i}^{-1}$ such that $f_{e,i}^{-1}(f_{e,i}(t)) = t$. This means that there is a one-to-one correspondence between the originating and the destination track. Based on this mathematical description of the mapping function, each SB is bidirectional. Table 1 shows examples of mapping functions for various SBs. Each of these functions are modulo W .

TABLE I MAPPING FUNCTIONS FOR SWITCH BOX STYLES

Mapping function	Subset SB	Wilton SB	Universal SB
$f_{e,1}(t)$	t	$W-t$	$W-t-1$
$f_{e,2}(t)$	t	$t+1$	t
$f_{e,3}(t)$	t	$W-t-2$	$W-t-1$
$f_{e,4}(t)$	t	$t-1$	t
$f_{e,5}(t)$	t	t	t
$f_{e,6}(t)$	t	t	t

All the SBs that are explored here, are composed by W transistors, where W is the routing channel width. The Subset switch box is the simplest among the three SBs. Its functionality is similar to the one that used in the Xilinx XC4000 FPGAs [1]. The Universal SB leads to better routability compared to Subset SB. Moreover, based on experimental results [5, 12] this SB pattern leads to smaller devices, as it requires fewer tracks for successful P&R. Finally, the Wilton SB design tries to solve the limitation that exhibits the other two SBs (Subset and Universal). This limitation regards the restriction of a network to remain on the same track or pair of tracks, respectively, by changing the track assignment on connections that turn. This permits overall track changes to be accomplished by permuting the global route, leading to greater flexibility in the initial track selection near the source. Experimental results [5] showed that the combination of Wilton SB, with routing wires longer than L_1 , requires about 5% and 14% less tracks compared to Subset and Universal SB, respectively. Despite the area requirements, most of the applications exhibit similar delay, regardless of the

chosen SB pattern, when all the routing tracks are formed by length L_1 wires [5, 12]. In addition to that, the Wilton SB results in better routability [14], as it requires narrow channel width (i.e., composed by fewer wires) for successful P&R. However, as the segment length increases, the Subset SB leads to faster, to lower power as well as to area efficient solutions than the other two alternative SBs.

We chose the three SBs (Wilton, Universal and Subset) for our exploration process due to fact that these SBs are widely-used and they can be supported by the *EX-VPR* tool. It should be noted that more efficient SBs can be found in relevant references and therefore, they may result into an SB combination with more efficient solutions. However, the primary goal of the proposed methodology is to prove that a combination of SBs results into reduced delay and energy consumption.

B. Switch Box Selection Procedure

The exploration procedure for determining the most appropriate SB pattern combination for the proposed interconnection network was done by the *MEANDER* design framework [6, 9]. As mentioned previously, the selection criterion was the EDP value. The results are summarized in Fig. (8) and (9), where the horizontal axis shows the percentage of area coverage between the alternative SB pattern combinations, while the vertical axis shows normalized values over the maximum EDP value. The normalized value for each SB combination is calculated by:

$$Normalized_EDP_{i,j} = \frac{EDP(SB_pattern_combination_k, SB_ratio_{k,l})}{\max_{i,j}\{EDP(SB_pattern_combination_k, SB_ratio_{k,l})\}} \quad (4)$$

where the variable $SB_pattern_combination_k$ denotes the k -th SB pattern combination, whereas the $SB_ratio_{k,l}$ gives the l -th SB pattern ratio of the k -th SB combination, with $0 \leq Normalized_EDP_{i,j} \leq 1$. In order to select the combination of multiple SB patterns, that will form the wires connections in our proposed general-purpose heterogeneous interconnection architecture, we employ the following methodology:

- Step a) For each one of the available SB pattern combinations, calculate the EDP for a number of different ratios between the SBs.
- Step b) Plot the results.
- Step c) Calculate the average EDP value of each combination.
- Step d) Select the SB combination with the minimum average EDP value.
- Step e) For the selected SB pattern combination (from the former step) determine the minimum value of the EDP curve. This value corresponds to the area coverage among the different SB patterns in the heterogeneous interconnection.

Assuming two distinct regions ($R_{th}=2$), we provide extensive exploration results for all possible combinations and *Area_Region* of the three different SB patterns. Fig. 8 shows the EDP exploration for the available SB combinations (Steps a and b). The horizontal axis represents the ratio of area

coverage (*Area Region*) between the two SB patterns, whereas the vertical one gives the EDP value in normalized manner.

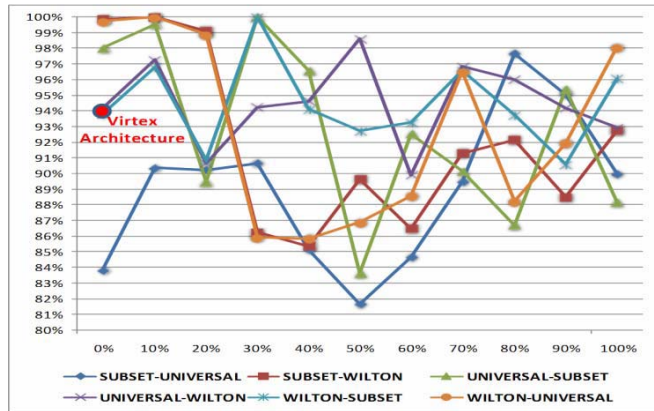


Fig. 8 The average EDP values for all the possible SB combinations with two regions

Based on this graph we calculate the average EDP value of each SB combination (step *c*). These values are summarized in Table 2. Then, we select the one that exhibits the lowest EDP value (step *d*) and for this SB pattern combination we find out the percentage of each SB pattern in the interconnection network. This percentage corresponds to the minimal value of the selected SB pattern combination curve. From Table 2 we conclude that the combination “Subset-Universal” exhibits the smallest EDP value compared to the rest solutions. The area coverage of each SB pattern can be retrieved from Fig. 9 (step *e*).

TABLE II AVERAGE EDP VALUES OVER ALTERNATIVE SB PATTERN COMBINATIONS (NORMALIZED VALUES)

SB patterns combination		Average EDP value
SB Pattern ₁	SB Pattern ₂	
Subset	Universal	0.816
Subset	Wilton	0.854
Wilton	Subset	0.906
Wilton	Universal	0.858
Universal	Subset	0.836
Universal	Wilton	0.899

More specifically, Fig. 9 plots the EDP variation for the “Subset-Universal” combination over a number of different ratios for area coverage. This graph is part from the Fig. 8. The percentage of area coverage between these two SB patterns corresponds to the minimum value of this curve. For our approach this occurs at 50%, which means that 50% of the available SBs are form connections based on the Subset SB pattern, whereas the rest 50% are Universal SBs. Such an SB pattern combination achieves to reduce the EDP value about 18% compared to the rest candidate solutions. Moreover, the proposed heterogeneous interconnection network achieves an EDP reduction by 9%, compared to the Virtex architecture.

The previous results are retrieved after P&R into smallest Virtex FPGA. These constraints imply that for some small variations of SB ratios, we may have large EDP variations (as the routing algorithm tries to find out the narrowest channel

width, it uses a more stressed approach). By varying the ratio between area coverage of the SB patterns, we modify the available routing resources, which influence the performance, the energy consumption and the silicon area of the device.

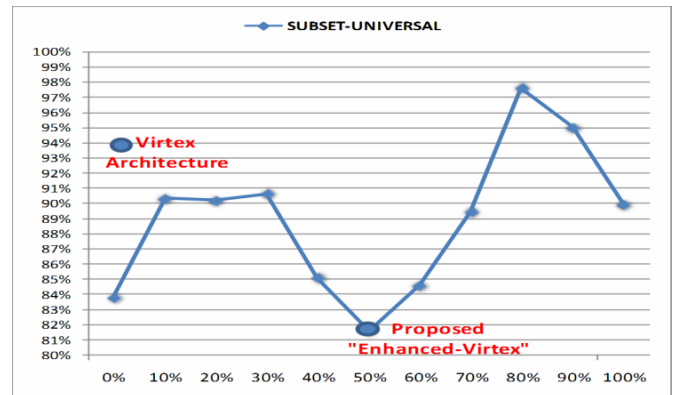


Fig. 9 Selection of the ratio between two SBs

VII. EXPERIMENTAL RESULTS

For demonstration purposes, the derived general-purpose heterogeneous interconnection network was integrated into a Virtex FPGA and the retrieved architecture named “Enhanced-Virtex”. Its efficiency was evaluated against the original Virtex architecture with the usage of the 20 biggest MCNC benchmarks. These were mapped on the smallest Virtex-style FPGA [6, 16] that fits, by using the *EX-VPR* tool. As it discussed previously, our proposed interconnection network consists of two regions, each of which occupies half of the device area ($Area_{Region_1} = Area_{Region_2} = 50\%$). Based on the exploration procedure described in Sections 5 and 6, the interconnection network in *Region₁* has wire segments with length L_2 and Subset SB pattern, whereas in *Region₂* the segments has length L_1 and the Universal SB pattern is employed. During our experimental results, both the original Virtex-based FPGAs, as well as the proposed one (*Enhanced-Virtex*) have identical amount of logic resources, with same percentage of logic utilization. Also, each of the benchmarks has same placement across the alternative devices.

The evaluation procedure was done using two alternative scenarios. The first one involves the P&R of benchmarks with the narrowest routing channel width, whereas the second one uses 20% additional tracks in each channel. Even though, the second approach is not an area efficient solution, however, it represents a low-stress situation, usually encountered in practice (e.g., [5, 12]), since designers are seldom comfortable operating near the edge of routability.

Table 3 gives the EDP values for the Virtex style architecture, using Subset, Wilton and Universal SBs, and for the proposed one which is composed by the selected segment wire distribution and SB pattern combination. The columns from two to four show the EDP value of each benchmark for the Virtex-style FPGA composed solely by one SB pattern. Columns five and six give the EDP value for the proposed *Enhanced-Virtex* device with the minimum number of routing tracks, including one that has 20% additional wires. The proposed device achieves to reduce the EDP value up to 70% compared to the Virtex-based FPGA with Universal SB

pattern, whereas the average EDP reduction over the three homogeneous solutions is 58% for the narrowest routing channel and 63% for the 20% wider channel.

The remaining Tables (4 to 7) compare specific design parameters of the benchmark implementations. All of these Tables have six columns. In particular, the first one shows the benchmark name, the next three columns (second to fourth) concern the results of homogeneous device consisted solely by Subset, Wilton or Universal SB, respectively, whereas the last two columns evaluate the proposed interconnection of the *Enhanced-Virtex* device. More specifically, the fifth column reports the results regarding the minimum number of required routing tracks for successful P&R, whereas the last one uses a 20% wider routing channel.

The gain (or loss) of the proposed interconnection architecture compared to the other Virtex-style devices with the three SB patterns is calculated by applying the following formula:

$$Gain_{vs_Virtex} = \frac{parameter_{Virtex} - parameter_{Proposed}}{parameter_{Virtex}} \times 100\% \quad (5)$$

where $Gain_{vs_Virtex}$ denote the gain (or loss) of the proposed interconnection network ($parameter_{Proposed}$) versus the average value (regarding i.e., delay, energy, area, etc) for Virtex-style devices ($parameter_{Virtex}$) with solely the Subset, Wilton and Universal SB.

Table 4 compares the alternative interconnections in terms of the minimal number of routing tracks for successful P&R. The average number of routing tracks for the three Virtex style solutions is 17.2, whereas our interconnection has negligible decrease (by 2%) when the minimal channel width is selected. On the other hand, we increase the average routing tracks (about 20%) when we route the benchmarks with a wider channel solution.

Table 5 compares the alternative interconnections in terms of the critical path (i.e., maximum operation frequency). The average delay for the Virtex style architectures with the three SB patterns (i.e., Subset, Wilton and Universal) is 78.93 nsec. The proposed interconnection scheme without and with the wider routing channel achieves to reduce the delay (i.e., increase maximum operation frequency) about 16% and 26%, respectively.

Table 6 proves that the proposed interconnection network achieves significant leakage power reduction, which range from 8.5% (for wider routing channel) up to 21% (if minimal channel width is selected) compared to Virtex-style devices. This occurs due to the better utilization of the available routing fabric. Taking into consideration that as technology scales down, the static power becomes a dominant power component, then our general-purpose heterogeneous interconnection network achieves to manage it more efficiently than the current trend about architecture design (academic or commercial) with uniform routing resource distribution across the device.

Finally, we evaluate the energy consumption. As this parameter is a function of total power and circuit delay, it is a fair metric to compare the alternative architectures. Based on Table 7, the developed heterogeneous interconnection

architecture reduces the energy requirements against to the average Virtex style devices about 11% for both cases (minimum and maximum number of tracks).

It should be stressed that we achieved to design a general-purpose high-performance interconnection network for FPGAs, without any negative impact on leakage or total energy consumption, although high-performance circuit implies high-switching activity and eventually, increased energy requirements. Even though the proposed interconnection needs less routing tracks compared to conventional Virtex style FPGAs, it also achieves to reduce other critical design parameters (i.e., delay, leakage power and energy consumption). This occurs due to the better utilization of the hardware resources that form the interconnection network. In other words, the proposed selective procedure for determining the most suitable wire distribution and SB pattern combination, leads to significant gains.

VIII. CONCLUSION

A novel interconnection network targeting to general-purpose reconfigurable architectures was presented. By taking into consideration the appropriately info regarding the statistical and spatial constraints that introduced by the P&R algorithms, we propose a multiple region device, each of them having different routing fabric. The selection criterion for the design steps was the minimum EDP value, leading to a network that achieves high operation frequencies and low-energy consumption. For evaluation purposes, we integrate the derived interconnection scheme to a Virtex-based FPGA. The comparison results prove that the proposed heterogeneous platform outperforms a Virtex FPGA. More specifically, we achieve average EDP reduction 63%, delay reduction up to 26%, leakage power reduction up to 21% and energy savings up to 11% were achieved. Furthermore, the design of the new architecture is a fully software-supported by three new CAD tools.

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TABLE III EDP VALUES FOR THE VIRTEX-STYLE ARCHITECTURE WITH SUBSET, WILTON AND UNIVERSAL SB, AS WELL AS THE TWO ENHANCED VIRTEX DEVICES (MINIMUM NUMBER OF TRACKS AND 20% WIDER ROUTING CHANNEL) WITH THE PROPOSED INTERCONNECTION SCHEME

Benchmark	Virtex-style FPGA			Enhanced (Proposed) Virtex	
	Subset SB ($\times 10^{-18}$)	Wilton SB ($\times 10^{-18}$)	Universal SB ($\times 10^{-18}$)	Minimum # of tracks ($\times 10^{-18}$)	+20% wider routing channel ($\times 10^{-18}$)
alu4	408.67	551.18	568.11	380.29	355.01
apex2	653.65	725.40	645.08	471.66	421.32
apex4	377.00	370.17	349.10	301.50	218.51
bigkey	517.14	451.77	446.19	326.23	290.76
clma	3741.03	1983.19	1866.50	1087.80	587.70
des	893.04	835.56	672.81	521.22	615.49
diffeq	287.29	269.72	287.13	258.91	287.93
dsip	477.10	341.28	437.63	312.62	299.79
elliptic	2041.60	13559.00	1525.16	1363.98	1172.30
ex5p	343.87	316.45	317.18	265.52	219.74
ex1010	3237.50	1315.37	1693.20	1444.56	1278.52
frisc	1000.92	1104.10	1090.21	929.20	982.21
misex3	498.49	435.81	358.10	323.65	294.30
pd	2900.80	1882.40	2385.20	1736.80	1413.67
s298	989.04	1037.40	970.08	768.18	912.79
s38417	2470.80	1805.76	2357.10	2109.45	1519.09
s38584	1739.91	1615.52	1632.85	1211.18	1041.03
seq	502.94	482.11	400.67	393.59	340.75
spla	1806.00	1150.50	1715.70	1067.65	915.11
tseg	268.24	244.57	247.30	217.66	296.94
Average:	1257.75	1523.86	998.27	774.58	673.15

TABLE IV AREA COMPARISONS (IN TERMS OF REQUIRED NUMBER OF TRACKS FOR SUCCESSFUL P&R) BETWEEN THE VIRTEX-STYLE ARCHITECTURE WITH SUBSET, WILTON AND UNIVERSAL SB, AS WELL AS THE TWO ENHANCED VIRTEX DEVICES (MINIMUM NUMBER OF TRACKS AND 20% WIDER ROUTING CHANNEL) WITH THE PROPOSED INTERCONNECTION SCHEME

Benchmark	Virtex-style FPGA			Enhanced (Proposed) Virtex	
	Subset SB (# of tracks)	Wilton SB (# of tracks)	Universal SB (# of tracks)	Minimum # of tracks (# of tracks)	+20% wider routing channel (# of tracks)
alu4	19	16	16	17	20

apex2	21	18	18	19	23
apex4	22	18	18	19	23
bigkey	14	9	10	11	13
clma	24	19	19	18	22
des	18	11	13	13	16
diffeq	15	12	13	13	16
dsip	14	9	10	12	14
elliptic	21	16	17	18	22
ex5p	21	18	19	19	23
ex1010	19	18	18	19	23
frisc	23	19	19	21	25
misex3	20	17	18	18	22
pdc	32	25	25	26	31
s298	18	12	13	13	16
s38417	17	13	13	15	18
s38584	16	13	14	12	14
seq	20	17	18	19	23
spla	28	21	23	24	29
tseg	15	12	12	12	14
Average:	19.85	15.65	16.30	16.90	20.35

TABLE V COMPARISON IN TERMS OF APPLICATION DELAY BETWEEN THE VIRTEX-STYLE ARCHITECTURE WITH SUBSET, WILTON AND UNIVERSAL SB, AS WELL AS THE TWO ENHANCED VIRTEX DEVICES (MINIMUM NUMBER OF TRACKS AND 20% WIDER ROUTING CHANNEL) WITH THE PROPOSED INTERCONNECTION SCHEME

Benchmark	Virtex-style FPGA			Enhanced (Proposed) Virtex	
	Subset SB (nsec)	Wilton SB (nsec)	Universal SB (nsec)	Minimum # of tracks (nsec)	+20% wider routing channel (nsec)
alu4	59.4	62.0	65.3	51.6	48.9
apex2	76.9	77.5	72.4	55.1	50.7
apex4	75.4	71.6	71.1	64.7	47.4
bigkey	44.2	40.7	41.7	32.3	29.7
clma	197.0	95.3	90.3	111.0	64.3
des	73.2	63.3	54.7	43.8	49.2
diffeq	53.4	54.6	52.3	52.2	51.6
dsip	36.7	31.6	40.9	31.9	32.8
elliptic	116.0	74.5	83.8	76.2	65.2
ex5p	70.9	63.8	67.2	59.4	45.4
ex1010	175.0	81.7	99.6	92.6	83.4
frisc	87.8	90.5	90.1	92.0	84.6
misex3	73.2	57.8	51.6	50.1	45.0
pdc	148.0	104.0	134.0	104.0	84.6
s298	95.1	98.8	97.3	82.6	87.6
s38417	85.2	62.7	81.0	73.5	55.3
s38584	88.5	87.8	86.9	72.7	62.3
seq	67.6	59.3	51.9	52.2	45.8
spla	129	88.5	129	81.5	76.9
tseg	54.3	53.4	48.3	50.5	53.6
Average:	90.34	70.97	75.47	66.50	58.22

TABLE VI COMPARISON IN TERMS OF LEAKAGE POWER CONSUMPTION BETWEEN THE VIRTEX-STYLE ARCHITECTURE WITH SUBSET, WILTON AND UNIVERSAL SB, AS WELL AS THE TWO ENHANCED VIRTEX DEVICES (MINIMUM NUMBER OF TRACKS AND 20% WIDER ROUTING CHANNEL) WITH THE PROPOSED INTERCONNECTION SCHEME

Benchmark	Virtex-style FPGA			Enhanced (Proposed) Virtex	
	Subset SB (mWatt)	Wilton SB (mWatt)	Universal SB (mWatt)	Minimum # of tracks (mWatt)	+20% wider routing channel (mWatt)
alu4	8.58	8.08	8.17	6.09	7.45
apex2	9.96	10.69	11.05	8.71	9.98
apex4	6.75	7.48	7.64	6.05	6.66
bigkey	10.71	8.96	9.98	7.96	10.28

clma	10.62	8.57	9.72	8.33	10.24
des	19.44	12.48	16.77	11.88	14.26
diffeq	5.70	6.29	7.05	5.16	5.67
dsip	10.62	8.57	9.72	8.33	10.24
elliptic	17.84	17.82	18.94	14.81	16.49
ex5p	5.72	6.37	7.14	5.17	5.50
ex1010	20.92	25.95	25.56	19.63	23.22
frisc	18.83	21.18	21.79	16.61	17.54
misex3	7.38	7.54	8.37	6.04	7.11
pdc	31.11	33.23	33.74	24.48	27.66
s298	8.69	7.96	9.06	6.44	7.17
s38417	25.17	28.31	28.73	22.48	28.25
s38584	32.11	34.23	34.74	24.48	27.66
seq	8.80	9.24	10.13	8.08	9.11
spla	22.80	24.12	25.76	18.83	22.04
tseg	4.22	4.51	4.55	3.36	3.79
Average:	14.30	14.58	15.43	11.65	13.52

TABLE VII COMPARISON IN TERMS OF TOTAL ENERGY CONSUMPTION BETWEEN THE VIRTEX-STYLE ARCHITECTURE WITH SUBSET, WILTON AND UNIVERSAL SB, AS WELL AS THE TWO ENHANCED VIRTEX DEVICES (MINIMUM NUMBER OF TRACKS AND 20% WIDER ROUTING CHANNEL) WITH THE PROPOSED INTERCONNECTION SCHEME

Benchmark	Virtex-style FPGA			Enhanced (Proposed) Virtex	
	Subset SB (nJoule)	Wilton SB (nJoule)	Universal SB (nJoule)	Minimum # of tracks (nJoule)	+20% wider routing channel (nJoule)
alu4	6.88	8.89	8.70	7.37	7.26
apex2	8.50	9.36	8.91	8.56	8.31
apex4	5.00	5.17	4.91	4.66	4.61
bigkey	11.70	11.10	10.7	10.10	9.79
clma	18.99	20.81	20.67	9.80	9.14
des	12.20	13.20	12.30	11.90	12.51
diffeq	5.38	4.94	5.49	4.96	5.58
dsip	13.00	10.80	10.70	9.80	9.14
elliptic	17.60	18.20	18.20	17.90	17.98
ex5p	4.85	4.96	4.72	4.47	4.84
ex1010	18.50	16.10	17.00	15.60	15.33
frisc	11.40	12.2	12.10	10.10	11.61
misex3	6.810	7.54	6.94	6.46	6.54
pdc	19.60	18.10	17.80	16.70	16.71
s298	10.40	10.50	9.97	9.30	10.42
s38417	29.0	28.80	29.10	28.70	27.47
s38584	19.66	18.40	18.79	16.66	16.71
seq	7.44	8.13	7.72	7.54	7.44
spla	14.0	13.00	13.3	13.10	11.90
tseg	4.94	4.58	5.12	4.31	5.54
Average:	12.29	12.29	12.16	10.90	10.94

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