Impact of Process Variations on the Vertical Silicon Nanowire Tunneling FET (TFET)

Z. X. Chen, T. S. Phua, X. P. Wang, G. -Q. Lo, and D. -L. Kwong

Abstract—This paper presents device simulations on the vertical silicon nanowire tunneling FET (VSiNW TFET). Simulations show that a narrow nanowire and thin gate oxide is required for good performance, which is expected even for conventional MOSFETs. The gate length also needs to be more than the nanowire diameter to prevent short channel effects. An effect more unique to TFET is the need for abrupt source to channel junction, which is shown to improve the performance. The ambipolar effect suppression by reducing drain doping concentration is also explored and shown to have little or no effect on performance.

Keywords—Device simulation, MEDICI, tunneling FET (TFET), vertical silicon nanowire.

I. Introduction

AS devices scale down, operating voltage (V_{DD}) is required to scale as well in order to prevent high power consumption as device and interconnect capacitances increase. However, V_{DD} scaling has slowed with each technology node as transistor threshold voltage (V_t) needs to scale as well to maintain circuit speed. With a subthreshold swing (SS) of 60 mV/dec, for example, a V_t reduction of 60mV will cause an increase in the off current, I_{off}, by ten times. So voltage scaling is limited by SS and has thus slowed with each technology node. The SS, in turn, is limited to kT/q for MOSFETs, and so there is a need for a new, unconventional device to provide a low SS.

Much interest has gone into tunneling FETs (TFETs) due to their capability of providing low off current (I_{off}) [1]-[14], SS not limited to kT/q [3] and a weak temperature dependence [2]. The main drawback of the TFET is the low tunneling efficiency in large or indirect band gap semiconductors. So silicon-based TFETs typically exhibit low drive currents.

Silicon nanowires (SiNWs) have been shown to have high drive current, low leakage current, low DIBL, near ideal subthreshold behavior, and reduced temperature sensitivity [15]-[17]. This is due to the excellent gate electrostatic control over the narrow channel provided by the gate-all-around (GAA) structure. Furthermore, vertical SiNW (VSiNW) MOSFETs, either synthesized [18] or fabricated using CMOS compatible technology [19], allow the possibility of high device density or device stacking on a single SiNW.

By combining the two technologies of TFETs and VSiNWs, a VSiNW TFET is produced, which is an excellent candidate for low power, high-density applications.

This paper presents VSiNW TFET simulations to determine the impact certain process changes, like gate length, nanowire diameter, doping level and doping abruptness, would have on the device performance.

II. Device Simulations

MEDICI device simulations were performed on the *n*-type VSiNW TFET to determine the effects of process variations, namely the nanowire diameter (d), gate oxide thickness (t_{ox}), gate length (L_g), doping levels and junction abruptness. The junction abruptness is varied through MEDICI parameter Y.CHAR, defined as the length where the dopant concentration degrades by 1/e of the maximum concentration.

Fig. 1 shows the structure used in the MEDICI simulations. The *n*-type TFET defined in this paper has an *n+* drain, *p* channel and *p+* source. The device dimensions are varied throughout the various design simulations. Unless otherwise mentioned, default values and dimensions used in the simulations are:

Gate length (L_g)	:100 nm
Gate oxide thickness (t_{ox})	:4.5 nm
Nanowire diameter (d)	:70 nm
Channel doping (*p*-type)	:10^{15} cm^{-3}
Source doping (*p*-type)	:10^{20} cm^{-3}
Drain doping (*n*-type)	:10^{20} cm^{-3}
Junction abruptness (Y.CHAR)	:0 nm

A V_{ds} of 1.2 V is also used. The band-to-band tunnelling (BTBT) model in MEDICI uses Kane's model [20]. For simplicity, *n*-type poly-Si gate was used for all simulations.

A. Effects of Physical Parameters

The effects of nanowire diameter were first simulated (Fig. 2). With a narrower nanowire, the V_t and SS are both reduced, and I_{on} is also higher. This is expected as a narrower nanowire would give the gate a better electrostatic control over the channel and help decrease the SS, V_t and increase I_{on}. The gate oxide thickness, t_{ox}, similarly affects the gate electrostatic control and hence TFET performance (Fig. 3).

The gate length was also found to influence the TFET characteristics, as shown in Fig. 4, but only when it becomes comparable to or less than the nanowire diameter. At L_g of 100 nm or higher, no change is observed. But at L_g of 50 nm, the SS increases due to short channel effects.

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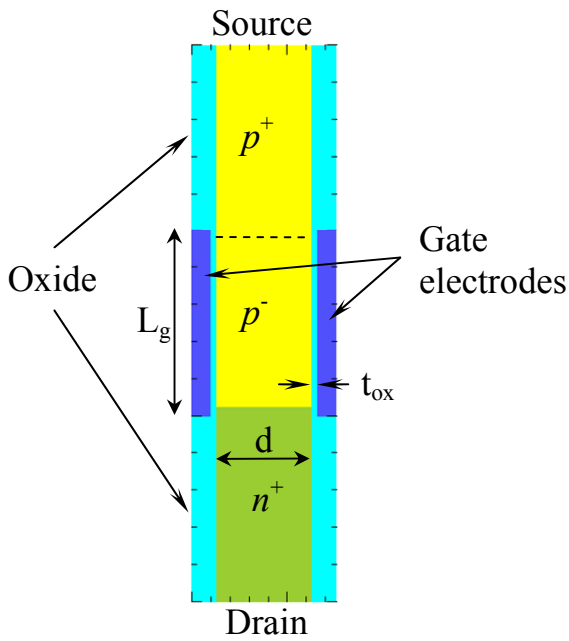Vol:7, No:9, 2013

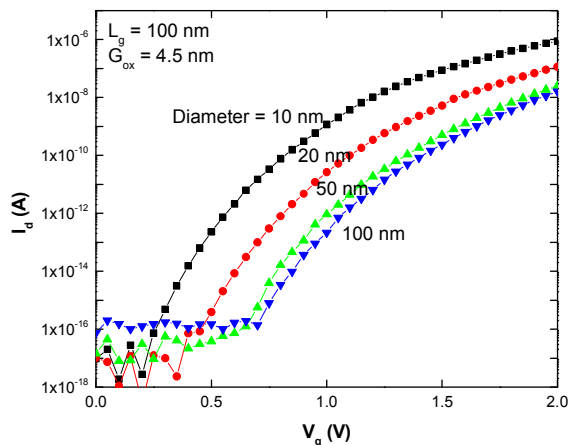Fig. 1 Vertical silicon nanowire TFET MEDICI simulation structure

Fig. 2 Simulated characteristics of a VSiNW TFET with different
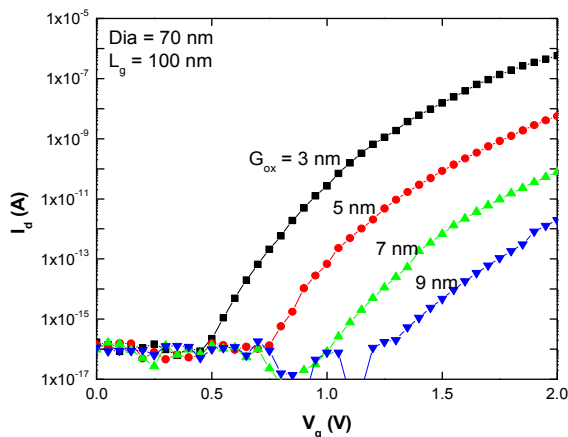nanowire diameters

Fig. 3 Simulated characteristics of a VSiNW TFET with different
gate oxide thicknesses

The effects of junction abruptness on TFET performance were also investigated. The characteristic length (Y.CHAR) of the doping profile at the $n+$-i junction, modelled as a Gaussian function, is varied. Based on the MEDICI simulations shown in Fig. 5, the device performs poorer as the doping profile of the tunnelling junction is less abrupt, or Y.CHAR is larger. The results agree with that of [12].

B. Effects of Doping Levels

Next, the effects of source/drain doping are investigated. Fig. 6 shows the drain ($n+$) doping effects on the I_d-V_g characteristics. No effects are observed for $V_g > 0$ as the tunneling junction in this case is at the $p+$-i junction, which will remain unaffected by the $n+$ doping concentration. However, the effects can be seen for $V_g < 0$ where performance is clearly degraded, with an increase in V_t, and a decrease in I_{on} and SS. Conversely in Fig. 7, the $p+$ doping concentration variation does not affect the characteristics for $V_g < 0$, but only for $V_g > 0$. So drain doping concentration should be kept low to suppress ambipolar properties, if required, and source doping concentration should be kept high to maximise the TFET performance.

With the above results in mind, a high performance VSiNW TFET is simulated with the following parameters:

Gate length (L_g)	100 nm
Gate oxide thickness (t_{ox})	3 nm
Nanowire diameter (d)	10 nm
Channel doping (p-type)	10^{15} cm^{-3}
Source doping (p-type)	10^{20} cm^{-3}
Drain doping (n-type)	10^{20} cm^{-3}
Junction abruptness (Y.CHAR)	0 nm

The resulting I_d-V_g curve is shown in Fig. 8 (black squares). I_{on} is of the order 10 μA or ~1000 μA/μm, I_{off} is less than 10^{-16} A, and SS is 40 mV/dec. This high performance TFET also has excellent $V_g<0$ characteristics, making it nearly symmetrical. The same structure is simulated with ambipolar effect suppression through lower drain ($p+$) doping (red circles in Fig. 8), and with lower drain doping and non-abrupt junction (green triangles in Fig. 8). Although the I_{off} increases very slightly, ambipolar effect suppression is achieved without affecting the performance. This shows that a VSiNW TFET provides a very low I_{off} and SS, and still be able to match, or even better, the drive current of conventional MOSFETS.

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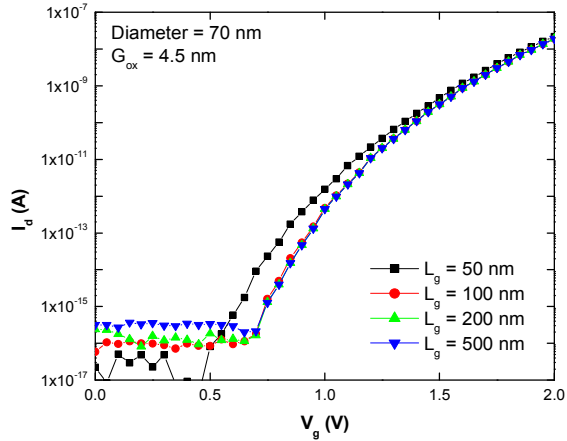Vol:7, No:9, 2013

Fig. 4 Simulated characteristics of a VSiNW TFET with different gate lengths
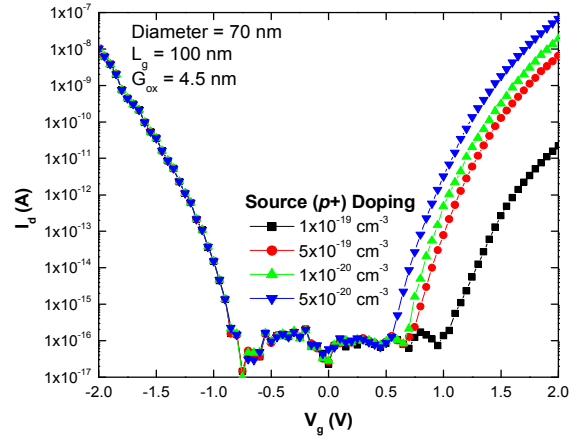

Fig. 7 Simulation data of VSiNW TFETs with different source doping concentrations
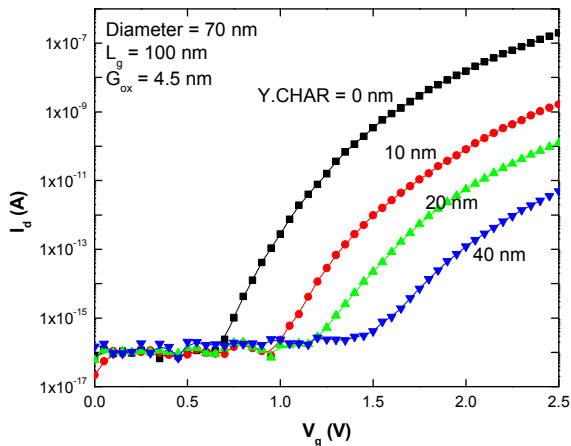

Fig. 5 Simulation data of a VSiNW TFET with different doping profile abruptness at the bottom *p-i* junction. Y.CHAR represents the depth where the impurity concentration degrades by 1/e
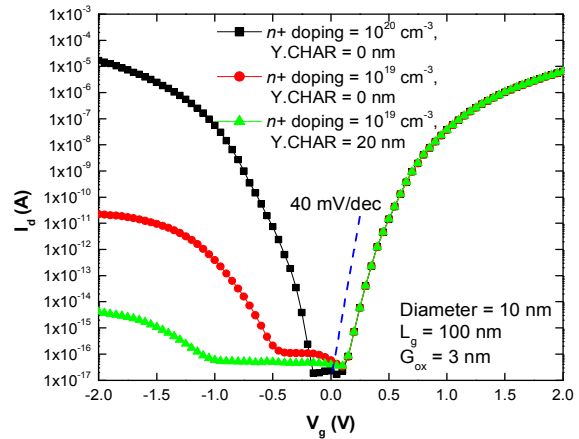

Fig. 8 Simulation data of high performance VSiNW TFETs showing ambipolar effect suppression by decreasing drain doping concentration and/or characteristic length, Y.CHAR
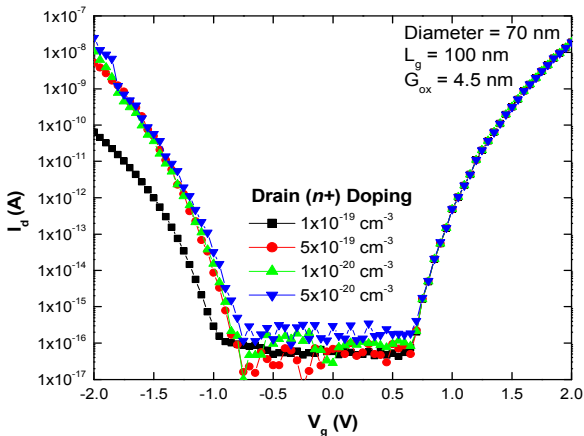
III. CONCLUSION

Device simulations on VSiNW TFET were presented. By realizing the TFET on 10nm diameter nanowire and 3nm gate oxide thickness with abrupt junctions, the performance could potentially be good enough to replace MOSFETs. The ambipolar effect suppression by reducing drain doping is also possible.

Fig. 6 Simulation data of VSiNW TFETs with different drain doping concentrations

REFERENCES

[1] C. Hu, "Green transistor as a solution to the IC power crisis," in *9th International Conference on Solid-State and Integrated-Circuit Technology, 2008*, pp. 16-20.
[2] W. M. Reddick and G. A. J. Amaratunga, "Silicon surface tunnel transistor," *Applied Physics Letters,* vol. 67, no. 4, pp. 494-496, 1995.

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International Journal of Electronics and Communication Engineering
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[3]   M. Born, *et al.*, "Tunnel FET: A CMOS Device for high Temperature Applications," in *25th International Conference on Microelectronics, 2006*, pp. 124-127.

[4]   W. Y. Choi, B.-G. Park, J. D. Lee, and T.-J. K. Liu, "Tunneling Field-Effect Transistors (TFETs) With Subthreshold Swing (SS) Less Than 60 mV/dec," *IEEE Electron Device Letters,* vol. 28, no. 8, pp. 743-745, 2007.

[5]   K. Boucart and A. M. Ionescu, "Double-Gate Tunnel FET With High-κ Gate Dielectric," *IEEE Transactions on Electron Devices,* vol. 54, no. 7, pp. 1725-1733, 2007.

[6]   P.-F. Wang, *et al.*, "Complementary tunneling transistor for low power application," *Solid-State Electronics,* vol. 48, no. 12, pp. 2281-2286, 2004.

[7]   N. B. Patel, A. Ramesha, and S. Mahapatra, "Performance enhancement of the tunnel field effect transistor using a SiGe source," in *International Workshop on Physics of Semiconductor Devices,* 2007, pp. 111-114.

[8]   K. K. Bhuwalka, J. Schulze, and I. Eisele, "Scaling the vertical tunnel FET with tunnel bandgap modulation and gate workfunction engineering," *IEEE Transactions on Electron Devices,* vol. 52, no. 5, pp. 909-917, 2005.

[9]   T. Krishnamohan, D. Kim, S. Raghunathan, and K. C. Saraswat, "Double-gate strained-Ge heterostructure tunneling FET (TFET) with record high drive current and <60mV/dec subthreshold slope," in *International Electron Device Meeting*, 2008, pp. 947-949.

[10] O. M. Nayfeh, *et al.*, "Design of Tunneling Field-Effect Transistors Using Strained-Silicon/Strained-Germanium Type-II Staggered Heterojunctions," *IEEE Electron Device Letters,* vol. 29, no. 9, pp. 1074-1077, 2008.

[11] A. S. Verhulst, *et al.*, "Complementary Silicon-Based Heterostructure Tunnel-FETs With High Tunnel Rates," *IEEE Electron Device Letters,* vol. 29, no. 12, pp. 1398-1401, 2008.

[12] E.-H. Toh, G. H. Wang, L. Chan, G. Samudra, and Y.-C. Yeo, "Device physics and guiding principles for the design of double-gate tunneling field effect transistor with silicon-germanium source heterojunction," *Applied Physics Letters,* vol. 91, no. 24, p. 243505, 2007.

[13] P.-F. Wang, T. Nirschl, D. Schmitt-Landsiedel, and W. Hansch, "Simulation of the Esaki-tunneling FET," *Solid-State Electronics,* vol. 47, no. 7, pp. 1187-1192, 2003.

[14] S. O. Koswatta, D. E. Nikonov, and M. S. Lundstrom, "Computational study of carbon nanotube p-i-n tunnel FETs," in *IEEE International Electron Devices Meeting*, 2005, pp. 518-521.

[15] N. Singh, *et al.*, "Ultra-Narrow Silicon Nanowire Gate-All-Around CMOS Devices: Impact of Diameter, Channel-Orientation and Low Temperature on Device Performance," in *International Electron Devices Meeting*, 2006, pp. 1-4.

[16] N. Singh, *et al.*, "High-performance fully depleted silicon nanowire (diameter < 5 nm) gate-all-around CMOS devices," *IEEE Electron Device Letters,* vol. 27, no. 5, pp. 383-386, 2006.

[17] N. Singh, *et al.*, "Si, SiGe Nanowire Devices by Top-Down Technology and Their Applications," *IEEE Transactions on Electron Devices,* vol. 55, no. 11, pp. 3107-3118, 2008.

[18] J. Goldberger, A. I. Hochbaum, R. Fan, and P. Yang, "Silicon Vertically Integrated Nanowire Field Effect Transistors," *Nano Letters,* vol. 6, no. 5, pp. 973-977, 2006.

[19] B. Yang, *et al.*, "Vertical Silicon-Nanowire Formation and Gate-All-Around MOSFET," *IEEE Electron Device Letters,* vol. 29, no. 7, pp. 791-794, 2008.

[20] E. O. Kane, "Zener tunneling in semiconductors," *Journal of Physics and Chemistry of Solids,* vol. 12, no. 2, pp. 181-188, 1960.