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Oxide Based Resistive Random Access Memory Device for High Density Non Volatile Memory Applications

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Abstract**—**In this work, we demonstrated vertical RRAM device fabricated at the sidewall of contact hole structures for possible future 3-D stacking integrations. The fabricated devices exhibit polarity dependent bipolar resistive switching with small operation voltage of less than 1V for both set and reset process. A good retention of memory window ~50 times is maintained after 1000s voltage bias.

Keywords**—**Bipolar switching, non volatile memory, resistive random access memory, 3-D stacking.

I. Introduction

DATA storage has been crucial for all kinds of human activities, especially after entering the age of internet technology. To date, storage class memory devices are an indispensable component in our fast developing technological world. In the recent years of advancements with portable electronic devices such as smart phones and tablets, the main driving force in non-volatile memory had been the Flash technology, being numerously scaled aggressively to meet the ever growing demand for physically smaller, larger capacity and faster read/write memory chips. However, it is expected that the current Flash technology will soon meet up with bottleneck in terms of scalability although numerous breakthroughs in the past had sailed the mentioned to its leading position in today's non-volatile memory market.

Alternative memory concepts have been widely explored and studied by researchers and market competitors over the past decade, resistive random access memory (RRAM) being one of the most promising candidates [1]-[3]. Oxide based RRAM has been give extensive attentions due to the excellent memory performances such as lower operating voltage, high switching speed, and great potential of scalability and high density 3-D integration [4]-[6]. In this work, we demonstrated vertical RRAM device fabricated at the sidewall of contact hole structures for possible future 3-D stacking integrations.

II. Fabrication Process Flow

Vertical RRAM device fabrication is done with 8" complementary metal–oxide–semiconductor (CMOS) platform by using all CMOS compatible material stacks. Schematics of process flow are shown in Fig. 1. First step, after standard clean of 8" silicon wafer, lateral electrode metal 1 and an isolation dielectric is deposited by physical vapor deposition (PVD) and plasma enhanced physical vapor deposition (PECVD). After that contact hole structure is patterned with lithography of deep ultraviolet (DUV) light from excimer lasers with wavelengths of 248 nm etched with deep reactive-ion etching (RIE). Second step is to deposit resistive switching (RS) layer and fill the contact hole with vertical electrode of metal 2. Then chemical mechanical polishing (CMP) is used to planarize the wafer surface. Then another layer of isolation dielectric is deposited, and patterned with contact holes. Last step is metal deposition and patterned into measurement pads.

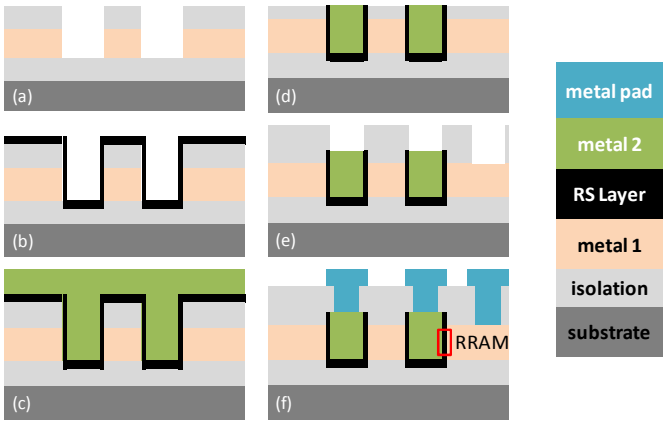

Fig. 1 Schematics of vertical device fabrication process flow: (a) metal 1 and isolation dielectric deposition and vertical electrode hole structure etch; (b) resistive switching layer deposition by PVD or ALD; (c) vertical electrode metal deposition; (d) metal chemical mechanical polishing to stop on isolation dielectric layer; (e) another isolation dielectric deposition and metal contact hole etch; (f) metallization to form measurement pads

Fig. 2 is the scanning electron microscope (SEM) images taken during device fabrication. Figs. 2 (a) and (b) are corresponding to Fig. 1 (a), which is the inspection during isolation dielectric etch and lateral electrode TiN etch. The contact hole size is about 680 nm in diameter. Fig. 2 (c) is contact to Ta vertical electrode etch, corresponding to Fig. 1 (e), and the contact hole size is about 510nm in diameter.

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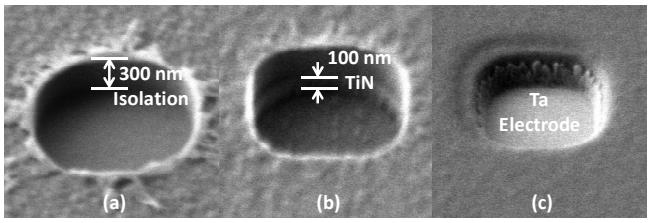

Fig. 2 SEM images taken during device fabrication: (a) 300 nm isolation dielectric etch; (b) 100 nm lateral electrode TiN etch; (c) vertical electrode Ta contact etch

III. Results and Discussion

In order to study the resistive switching behavior and verify the performance of vertical RRAM devices, electrical characterization is carried out mainly on an Agilent B1500A Semiconductor Device Analyzer (SCS) connected to a 200 mm manual probe station setup. The most common measurement method is voltage sweep controlled switching. In the vertical RRAM device testing, gradually changing voltage bias is applied to the vertical electrode with constants steps and lateral electrode is grounded. During voltage sweep, resistance changes from high resistance state (HRS) to low resistance state (LRS) and vice versa, as so this is called voltage sweep mode (VSM).

Polarity dependent bipolar resistive switching phenomenon is observed in the fabricated vertical RRAM devices. As the fresh RRAM device is usually at a very high resistance level, it usually requires a forming process to initiate the resistive switching, after the successful electrical forming, device exhibits bipolar resistive switching as shown in Fig. 3. During positive voltage sweep 1 (set process), current suddenly jumps at 0.5V, this is defined as set voltage. To avoid permanent breakdown of the device, compliance current is set at 1mA in the test by analyzer. The LRS state retains even voltage bias is removed. While in negative sweep 3, current starts to drop at -0.55V, this peak value of current is defined as reset current and the voltage point is defined as reset voltage.

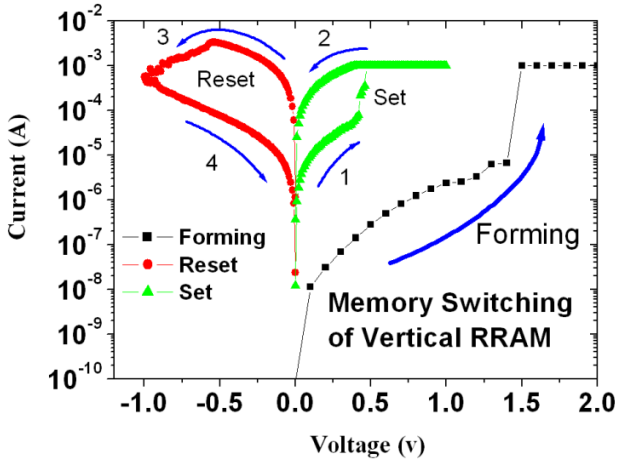

Fig. 3 Bipolar resistive switching current-voltage characteristics of fabricated vertical RRAM device. The voltage sweep sequence and three switching process of forming, set and reset are indicated in the figure

Data retention is referred to the ability of the memory cell to retain its state over long time period regardless of whether power is on or off. It is an important specification of nonvolatile memory. In general, a minimum of 10 years data retention time is required for commercial memory chip. Retention testing in this work is measured with constant voltage stress at 0.2V as shown in Fig. 4. Stable resistance retention has been observed in the plot for over 1000s, especially for LRS, resistance value keeps near at a constant value.

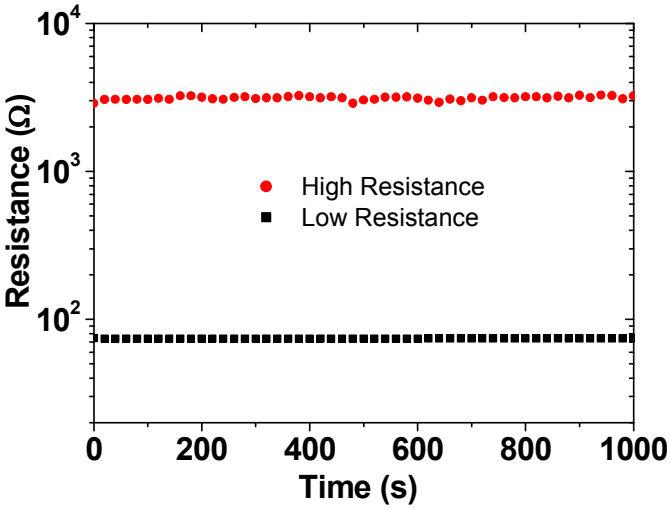

Fig. 4 Data retention measurement at 0.2V for 1000s at room temperature. Stable resistance retention has been observed in the plot for over 1000s, especially for LRS, resistance value keeps near at a constant value

The resistive switching phenomenon can be explained by formation and rupture of oxygen vacancies related conduction filaments [7], [8]. In detail, the set process is considered as percolation-like effect which forces oxygen ions to be depleted from oxide and thus form a conduction path with oxygen vacancies (V_o), this process is similar to dielectric soft breakdown. Correspondingly, the reset process depletes electrons in the vacancies and recovers them with oxygen ions from interfacial layer or interstitials.

IV. Conclusion

Vertical RRAM device formed at the sidewall of contact hole structures has been demonstrated in this work. The fabricated devices exhibit polarity dependent bipolar resistive switching with small operation voltage of less than 1V for both set and reset process. A good retention of memory window ~50 times is maintained after 1000s voltage bias. This vertical RRAM structure is suitable for future 3-D high density memory stacking, however, to achieve that a proper selection device is necessary to prevent sneak current leakage.

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