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An Area-Efficient and Low-Power Digital Pulse-Width Modulation Controller for DC-DC Switching Power Converter

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***Abstract*—**In this paper, a low-power digital controller for DC-DC power conversion was presented. The controller generates the pulse-width modulated (PWM) signal from digital inputs provided by analog-to-digital converter (ADC). An efficient and simple design scheme to develop the control unit was discussed. This method allows minimization of the consumed resources of the chip and it is based on direct digital design approach. In this application, with the proposed scheme, nearly half area and two-third of the power consumption was saved compared to the conventional schemes. This work illustrates the possibility of implementing low-power and area-efficient power management circuit using direct digital design based approach.

***Keywords*—**Buck converter, DC-DC power conversion, digital control, proportional-integral (PI) controller.

I. Introduction

IN today's industries, portable applications such as notebook and mobile phone require system with very small size, low power consumption, and high efficiency. As decrease of the supply voltage of circuits system, high efficiency DC-DC conversion circuits which can deliver low-power levels are desired. Thus, in recent years, in order to improve the efficiency of system, significant research has been conducted on DC-DC converters [1], [2]. This leads to improvement in device performance and energy efficiency. But, as so far, low-power DC-DC converters using digital microcontroller are few. One of the challenges for the application of DC-DC power conversion in low-power range is the control design to meet the system demands.

A fully digital controller is suitable for DC-DC power conversion application when the digital feedback signal is available [3]. It is well known that using digital controller offers many advantages over analog controller such as reducing areas of silicon, re-configurability, and lower power consumption [4]. Another obvious advantage of a digital system is that the design can easily be modified to a different controller and easily be implemented in different technologies, whereas the designers have to modify the hardware in the analog system [5]. Therefore, this type of controller is a good choice for DC-DC converter and to be integrated with other systems.

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In this work, we present a low-power digital controller for DC-DC power conversion. A brief overview of the digital controller used in DC-DC converter is given in this section. Section II presents the architecture of the implemented DC-DC converter and the functional description of the proportional-integral (PI) controller used in the converter is given. In Section III, the control scheme for DC-DC converter and the mathematical equations involved in its operation are discussed. Section IV describes detailed implementation of the proposed design. The validation result and performance analysis are also provided. Finally, Section V summarizes the conclusion of the work and discusses the future work.

II. Proposed Converter with Digital Controller

In order to obtain the required output voltage from the given input voltage, DC-DC converters are used in circuits system. Typically, buck converter topology is used to achieve an output voltage lower than the input voltage. The architecture of the proposed buck converter with digital controller is illustrated in Fig. 1. The system comprises of the power stage with the given input voltage, one analog-to-digital converter (ADC) to monitor the output voltage for feedback, an averaging filter to smooth out short-term variations and highlight longer-term trends, a programmable digital controller to generate the switch duty ratio and a digital pulse-width modulator (DPWM) that convert the computed duty ratio to a modulated pulse waveform output that controls the switch in the converter.

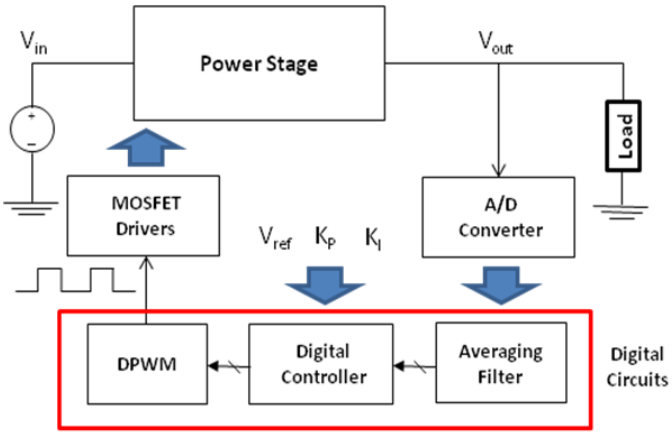

Fig. 1 Architecture of the proposed converter with digital controller

The operation of the buck converter is described as follows. The desired output voltage is first set on the DC-DC converter controller and then the ADC will sample the output voltage of the converter and sent the output data to the averaging filter. With the variation smoothed averaging result the digital controller determines the switching duty ratio. Finally, the DPWM serves as a digital-to-analog converter (DAC) in the control loop which converts the duty ratio into the pulse-width modulated (PWM) signal that controls the switch.

III. Control Design and Strategies

Both analog and digital control algorithms can be used to implement a voltage loop controller. In this design, a digital controller is used due to the flexibility in implementing a digital controller over its analog counterpart [6]. In the control system, the digital controller compares the feedback output voltage V_{out} from ADC with the digital voltage reference V_{ref}. Then the duty ratio $D(k)$ is updated based on the computed voltage error

$$e(k) = V_{ref} - V_{out}(k) \quad (1)$$

This duty ratio is then fed to DPWM to produce the switching pulses for the converter. The digital voltage controller can be implemented on the FPGA board, which is based on the given control algorithm. The digital control strategies used in this design are introduced below.

A. Proportional Control (P-Control)

One of the simplest ways of implementing a control loop is P-Control [7]. In such a control algorithm, the output switching duty ratio is proportional to the error of the output voltage, that is

$$D(k) = K_P \times e(k) \quad (2)$$

where K_P is the given proportional gain. A P-controller will provide sufficient settling time. However, it does not eliminate the steady-state error.

B. Integral Control (I-Control)

In order to eliminate the steady state error, an integral control is required [7]. In this control algorithm, the switching duty ratio is proportional to the integral of the error in the output voltage, which is

$$D(k) = K_I \times \sum_0^k e(k) \quad (3)$$

where K_I is the given integral gain. Equation (3) can be re-written in the following form

$$D(k) = D(k-1) + K_I \times e(k) \quad (4)$$

The new expression is simpler. An I-controller will eliminate the steady-state error. However, it will not provide fast transient response.

C. PI Control

In order to eliminate the steady state error and at the same time achieve fast transient response, a P-control algorithm and an I-control algorithm may be combined [7]. In this control algorithm, the duty ratio is obtained as

$$D(k) = K_P \times e(k) + K_I \times \sum_0^k e(k) \quad (5)$$

where K_P is the proportional gain and K_I is the integral gain. Using the relation of $D(k)$ and $D(k-1)$, we obtain the following expression

$$D(k) = D(k-1) + K_P \times (e(k) - e(k-1)) + K_I \times e(k) \quad (6)$$

which is easier to implement. This requires the information about the present error and the previous error. The new duty ratio updates based on these input.

D. Data Flow Graph

After discussing the control scheme and the mathematical equations involved, the next step is to determine the suitable Data Flow Graph (DFG) of the digital control algorithm. Since the voltage error $e(k)$ can be expressed as (1), so the duty ratio is re-written as

$$D(k) = D(k-1) + K_P \times \left(V_{out}(k-1) - V_{out}(k)\right) + K_I \times (V_{ref} - V_{out}(k)) \quad (7)$$

The first DFG of the control algorithm is concluded from the PI Control duty ratio expression which is shown in Fig. 2. Although this DFG satisfies design constraints, it does not achieve the optimized implementation and operation. Therefore, it is necessary to find out another DFG which satisfies an optimized implementation of the control algorithm. One of the power consumption operations in the digital controller is the multiplication, so some optimization is necessary in order to achieve low-power control algorithm.

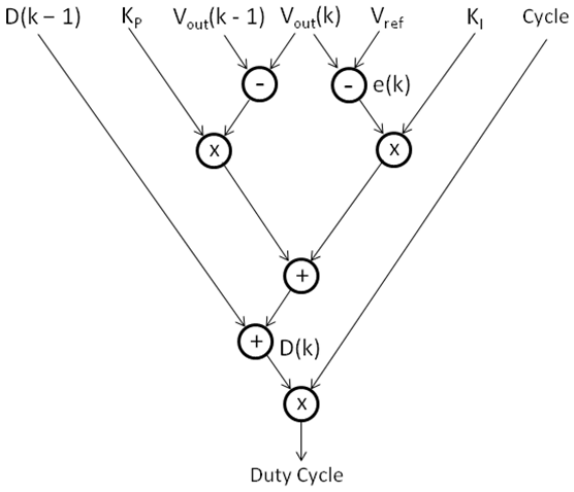

Fig. 2 DFG of the PI controller with (7)

As illustrated in Fig. 2, in this control algorithm, totally three multiply operations are conducted in a calculation cycle, those are, $K_P \times (V_{out}(k-1) - V_{out}(k))$, $K_I \times e(k)$, and duty ratio multiplication. In order to minimize the multiplication in the algorithm, the duty ratio is expanded and can be re-written in the following form

$$D(k) = D(k-1) + (K_P + K_I) \times (e(k) - e(k-1)) + K_I \times e(k-1) \quad (8)$$

where K_P is the proportional gain and K_I is the integral gain. Using $(k+1)$ replace k in the equation, we can further obtain the following expression

$$D(k+1) = D(k) + (K_P + K_I) \times (e(k+1) - e(k)) + K_I \times e(k) \quad (9)$$

With the comparison between (6) and (9), it can be found that the last item of two expressions is the same. That means it is possible to obtain $D(k+1)$ in the control scheme with only two multiplications if (9) is used for $D(k+1)$, which are $(K_P + K_I) \times (e(k+1) - e(k))$ and duty ratio multiplication. Also, the voltage error $e(k)$ can be expressed as (1), the duty ratio can be re-written as

$$D(k+1) = D(k) + (K_P + K_I) \times (V_{out}(k) - V_{out}(k+1)) + K_I \times (V_{ref} - V_{out}(k)) \quad (9)$$

The DFG of the digital PI controller with new $D(k+1)$ expression is presented in Fig. 3, which consists of only two multiply operations instead of three. These two DFG is then used to implement the control algorithm.

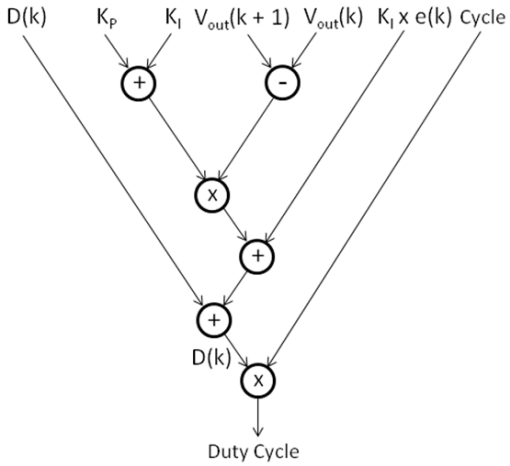

Fig. 3 DFG of the PI controller with (10)

IV. Implementation And Simulation Results

The structures of the PI controller have been considered in order to achieve optimized design of above PI control algorithm. The implementation circuit consists of registers, multiplexors, and arithmetic blocks. Each operation in the DFG is replaced by the correspondent circuit. One of the large hardware resources consumption blocks in the digital controller is the multiplier, so the repetitive multiply operations in the control scheme are found out and are replaced by using only one multiplier. The same multiplier can be reused for different multiply calculation as many times as needed. The new digital PI controller is implemented using only one multiplier instead of previous three multipliers.

A. Control Unit Design

Since multiplier reuse is involved in the controller, a control unit must develop to control the input and output of the multiplier. The control unit consists of a mealy finite state machine (FSM) and the instruction register. In this design, the control section is a six-state state machine, as shown in Fig. 4.

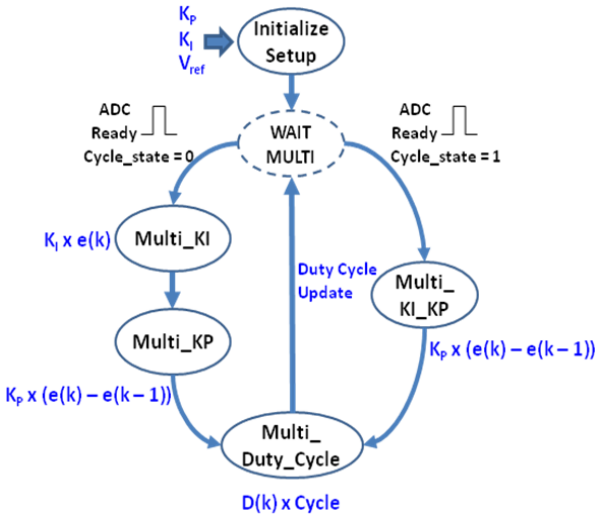

Fig. 4 State diagram of digital controller

At the beginning, the initial setup has been conducted and after which, the multiplier controller will be in the WAIT_MULTI state. Then the ADC status will be checked and the multiplication cycle starts upon receiving an ADC_Ready signal. As discussed above, two multiplication cycles are employed here which represent these two DFG: 1) (7) and 2) (10). These two multiplication cycles are conducted alternatively, which is controlled by the Cycle_state register.

B. DPWM

The control algorithm is described in above section. However, in order to obtain the modulated pulse, a DPWM needs to be used. The counter and comparator based approach is commonly employed in a DPWM system. For the switching frequency of f_s, the DPWM counter shall be clocked at least $N \times f_s$, where N is the dynamic range of the duty ratio $D(k)$. The counter counts from 0 to $N-1$ and the comparator compares the counter output with the required duty ratio which is obtain from the digital controller. The output of the DPWM keeps on being '1' when the counter is less than $D(k)$ and becomes '0' otherwise. The switching frequency keeps being constant and the duty ratio of the pulses will be updated accordingly when there is new ADC input.

C. Simulation Results

The whole function of the digital controller was designed in Verilog hardware description language (HDL) code and initially tested in Simvision to verify its operation. The Simulation results of the converter are as shown in Fig. 5. Upon the start-up of the simulation, the controller is initialized based on requirement. The digital voltage reference V_{ref}, the proportional gain K_P, and the integral gain K_P in this case have been setup according to the input signal and configuration. When the ADC is ready to sample voltage data, the controller begins to update the duty ratio D(k) based on the computed voltage error e(k). A sine signal is employed to be the input test signal.

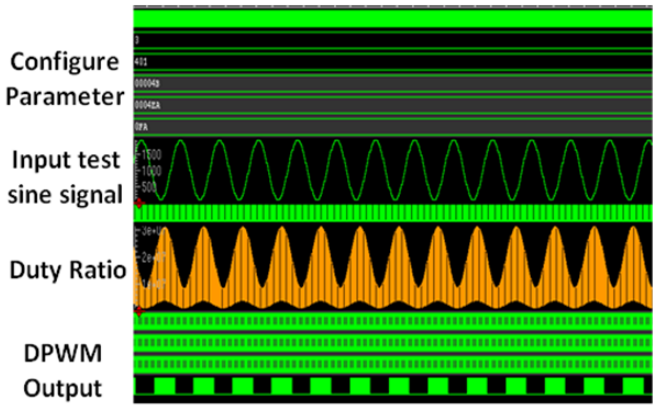

Fig. 5 Simulation Result of digital controller

As illustrated in Fig. 5, the digital controller functions within expectation. As the variation of the input sine signal, the value of duty ratio changed accordingly. The DPWM uses this duty ratio to produce the switching pulses for the converter. The length of the pulse updates as the duty ratio change. This controller was described in Verilog HDL code and synthesis was performed in order to compare the design result. From the synthesis report, nearly half area was saved through multiplier reuse for different multiply calculation. Since the decrease of the area consumption, the leakage power is also 50% lower than the original design. The total power consumption is reduced by around two-third after the multiplier reuse and multiplication control state machine optimization.

V. Conclusion

In this paper, a digital controller for DC-DC power conversion was presented. The controller generates the PWM signal from digital inputs provided by ADC. A simple and efficient design method to develop the control circuit was discussed. The scheme is based on direct digital design approach and allows minimization of the consumed resources of the system. The control unit meets the requirements such as fast transient response, low steady state error and re-configurability. Verification of the proposed controller was conducted using simulation tools. From the simulation results, it is concluded that the proposed scheme is effective in improving the efficiency of the controller. Using the proposed scheme, nearly half area and two-third of the power consumption was saved through the optimization compared to the conventional schemes. This work illustrates the possibility of implementing low-power and area-efficient power management circuit using direct digital design based approach. As the decrease of the controller cost, it is inevitable that digital controllers will become an integral part of DC-DC converter design.

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