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Low Frequency Noise Behavior of Independent Gate Junctionless FinFET

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***Abstract*—**In this paper we use low frequency noise analysis to understand and map the current conduction path in a multi gate junctionless FinFET. The device used in this study behaves as a gated resistor and shows excellent short channel effect suppression due to its multi gate structure. Generally for a bulk conduction device like the junctionless device studied in this work, the low frequency noise can be modeled using the mobility fluctuation model; however for this device we can also see the effect of carrier fluctuations on the LFN characteristic. The noise characteristic at different gate bias and also the possible location of the traps is explained.

***Keywords*—**LFN analysis, junctionless, Current conduction path, FinFET.

I. Introduction

SCALING of traditional planar transistor is limited by the short channel effects. The main reason for short channel effect is poor gate control. To counter this, the current research direction is to have channel in the third dimension in the form of vertical Fin or Nano wires, controlled by gate around the channel. Hence FinFET [1], tri-gate MOSFET [2], and gate-all-around (GAA) Nano wire MOSFET [3], [4] have been researched extensively as solutions. Though promising from a scalability perspective, all these devices might suffer from fabrication or reliability related issues. For example, the FinFET requires gate to be patterned across the fin. Three-dimensional devices also require doping to be conformal, increasing the complexity of junction formation, which, in any case, becomes more challenging with every new technology node [5], [6]. Junctionless devices have started to gain research focus to tackle junction related issues [7]-[9].

Apart from obvious process related advantages of these junctionless devices, these devices have lower Low frequency noise amplitude compared to traditional junction based devices [10]. Reduced Low frequency noise is an important figure of merit for electronic devices in RF applications. The bulk conduction of junctionless devices, instead of surface conduction in junction based devices, is the reason for lower noise amplitude.

In surface conduction based transistors the noise source is the carrier number fluctuation at the oxide channel interface. However in bulk conduction based junction less devices the noise source is attributed to the mobility fluctuations of the carriers. The Low frequency noise in junctionless transistors is generally explained using Hooge mobility fluctuation model [10].

In this study, we characterize the low frequency behavior of an independent gate junctionless device, the cross section of which is shown in Fig. 1. It has its channel in the form a vertical FIN, with resistance modulated by two independent gates formed on the side walls to exhibit transistor action. Being a junctionless device, this device is free from doped-junctions, which generally cause speed degradation, unnecessary energy consumption, and increasingly difficult fabrication challenges with scaling. In addition, this device is less expensive to fabricate due to lesser process steps.

II. Device Fabrication

The devices were fabricated on standard 8" boron-doped (10^{15} cm^{-3}) SOI wafers with 117nm top silicon layer and a 145nm buried oxide. Wafers were first implanted with phosphorus and annealed to yield uniform doping concentration of $5x10^{17}cm^{-3}$, the optimum concentration obtained through TCAD simulations for slit widths of 50nm easily achieved using 200nm technology lithography tool. Silicon nitride was then deposited using LPCVD process on a 3nm thermally grown pad oxide. Fins were patterned by DUV lithography and etched into silicon nitride, which acted as a (1) hard mask for the actual silicon slit etch, (2) stop layer for gate CMP process and (3) ion implant blocking mask to stop dopants from entering into the channel during poly-gate implant. The underlying silicon was then dry-etched using nitride as hard mask. To further reduce the Fin width and to reduce the sidewall surface roughness of the Fin, a layer of sacrificial oxide was thermally grown and subsequently removed by diluted HF wet etch. Gate oxide (4.5nm) was grown by dry oxidation, followed by deposition of LPCVD amorphous silicon as gate material. The deposited amorphous silicon on the top surface was removed by selective CMP until nitride hard mask was exposed to isolate the two gates. Gate was then implanted with BF_2 and activated, with the source/drain and channel slit protected by the nitride hard mask. Source and Drain were isolated by subsequent active area patterning and etching. A pre-metal dielectric oxide layer was deposited followed by contact hole etching and standard metallization processes.

To ensure ohmic source/drain contacts, the source and drain contact holes were patterned separately from the gate contacts and heavily implanted with arsenic. The TEM image across the FIN is as shown in Fig. 1.

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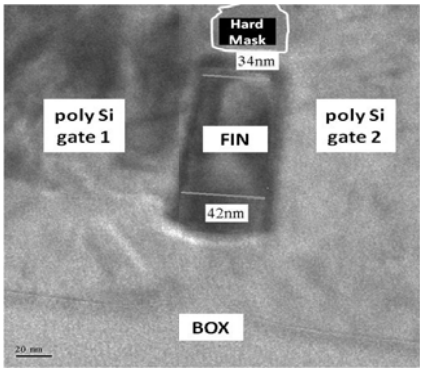


Fig. 1 Cross section of the device taken across the FIN, showing the two isolated gates

III. Result

The device under test is a junctionless device. The Source, drain and the channel is all doped N type (in this case) and the gate is doped P+ type. Due to the work function difference between the channel and the gate material there is a depletion region in the channel as shown in the figure. When both the gates is unbiased (0V) the depletion region from both the gates completely fills up the FiN width, hence there is very low OFF current. When a higher voltage (say 1V) is applied on either gate the corresponding depletion region recedes and there is a path for the current to flow from source to drain. Similarly when a higher voltage is applied to both the gates the channel (FiN in this device) is completely (relatively) opened. This device essentially operates as a gated resistor.

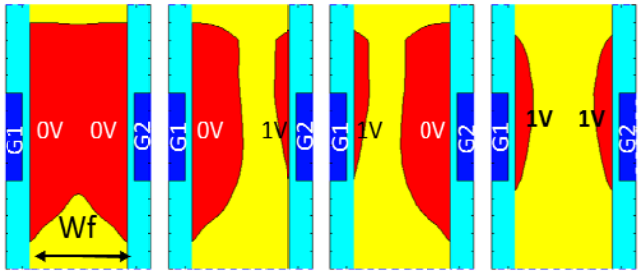
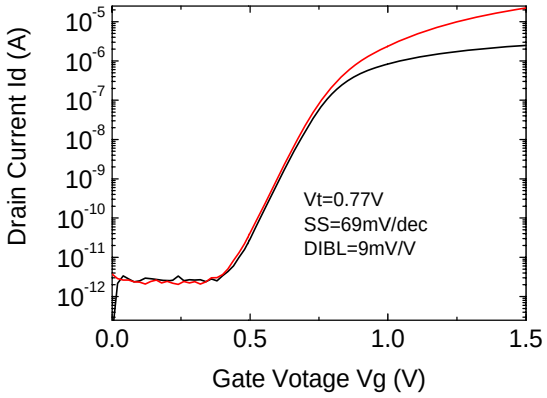
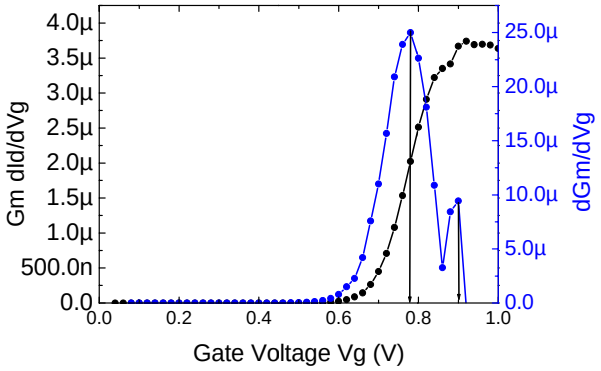


Fig. 2 2 D MEDICI simulation results showing the device operation

Fig. 3 (a) shows the Id Vg curve for the measured device. We see that, as expected, there is excellent short channel effect suppression (SS of 69mV/dec and DIBL of 9mV/V) due to its multi gate architecture. Fig 3 (b) shows the trans-conductance (Gm) and the rate of change of Gm with gate voltage. From the dGm/dVg curve we can extract the threshold voltage and the flat band voltage. The threshold voltage (Vt) is 0.77V and the flat band voltage (Vfb) is 0.88V. Please note in this IdVg measurement both the gate are swept together. Vt being less than Vfb is typical of a junctionless device. Hence we can assume that the main source of noise in this type of device is essentially due to mobility fluctuation of the carrier in the bulk. However many recent work on noise characterization of junction less device reports that carrier fluctuation based noise characteristics can be also observed in these devices. [10] We also report similar observation in our devices as evident from Fig. 4.



(a)



(b)

Fig. 3 (a) Measured Id-Vg characteristic (b) Gm, dGm/dVg curve

The noise amplitude (Sid) plots are shown for various gate biases is shown in Fig. 4. Our main objective was to study the effect of the second gate voltage on the current conduction path. Fig 4 (a) shows the noise amplitude when there is no bias on both the gates; this can be treated as the white noise (of either the device or the measurement system). This noise is inherently present in all the systems. When voltage is increased on one of the gates to a voltage greater than the threshold voltage we can see (from Fig. 4 (b)) that the noise characteristic assumes the form of g-r noise characteristic. G-R noise is the noise when there is carrier number fluctuation due to the trapping –de trapping of the carriers at trap locations. These traps have a forbidden energy level and are generally found in between the conduction band and the valence band. Since from the characteristic we see that till 500Hz the noise amplitude is not affected by frequency we can assume that the trapping- de trapping of the carriers occurs faster than the change in the applied signal. This is most like caused when the trap is a shallow (fast) trap hence we conclude that the traps are present in the depletion region surrounding the current path. Hence for this voltage bias condition, the conduction is still at the center of the Fin The difference in the noise amplitude for the two gates can be

explained due to higher leakage in one of the gates hence lower gate current, consequently lower noise amplitude.

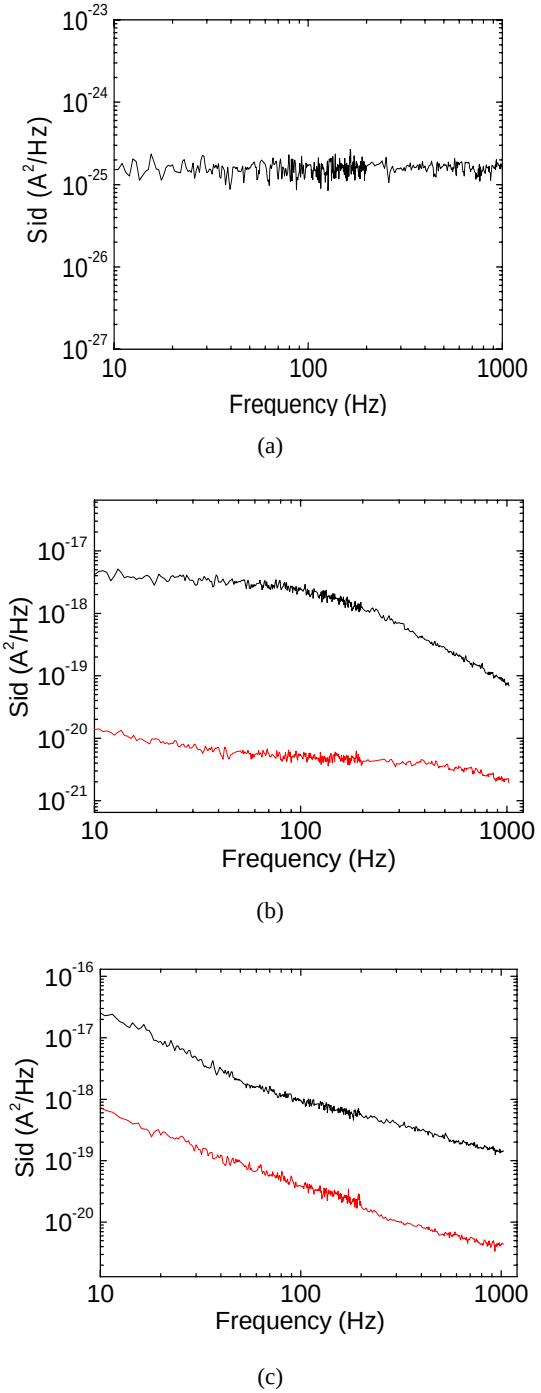


Fig. 4 Noise characteristics observed at different gate bias (a) When no bias is applied on both gates (b) When one of the gate bias is more than Vt (c) When voltage on one of the gates is increased to 1.2V

When the voltage on one of the gates is increased to 1.2V the noise characteristic (as seen in Fig. 4 (c)) assumes the form of 1/f in nature. This characteristic indicates that there is carrier fluctuation due to trapping and de trapping at the slow (deeper) oxide traps at the channel – oxide interface. Hence we can conclude that the current path for this voltage bias has reached either of the two gate/channel interface at the edge of the Fin. This observation closely agrees with the simulation result.

IV. Conclusion

In this paper we have studied the noise characteristic of a multi gate junctionless FinFET to understand the position of the current conduction path at various gate bias. We found for a gate voltage slightly greater than the threshold voltage the noise source is mainly the carrier fluctuations occurring due to trapping, de-trapping of carriers at shallow traps most likely in the depletion region, hence the current path is roughly at the center of the Fin For higher voltage, the 1/f nature of the noise characteristic indicates that the noise source is the carrier fluctuations occurring due to trapping, de-trapping at the slow traps most likely in the oxide–channel interface, hence the current path has reached the edge of the Fin However from data obtained we can see the level of noise obtained is generally lower than the conventional planar MoSFETs.

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