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Characterization of the Energy Band Diagram of Fabricated SnO_2/CdS/CdTe Thin Film Solar Cells

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Abstract—A SnO_2/CdS/CdTe heterojunction was fabricated by thermal evaporation technique. The fabricated cells were annealed at 573K for periods of 60, 120 and 180 minutes. The structural properties of the solar cells have been studied by using X-ray diffraction. Capacitance- voltage measurements were studied for the as-prepared and annealed cells at a frequency of 10^2 Hz. The capacitance- voltage measurements indicated that these cells are abrupt. The capacitance decreases with increasing annealing time. The zero bias depletion region width and the carrier concentration increased with increasing annealing time. The carrier transport mechanism for the CdS/CdTe heterojunction in dark is tunneling recombination. The ideality factor is 1.56 and the reverse bias saturation current is 9.6×10^{-10}A. The energy band lineup for the n-CdS/p-CdTe heterojunction was investigated using current - voltage and capacitance - voltage characteristics.

Keywords—SnO_2/CdS/CdTe heterojunction, XRD, *C-V* measurement, *I-V* measurement, energy band diagram.

I. Introduction

CDS/CdTe photovoltaic (PV) thin films play a key rule in the fast growing PV industry [1]. The ideal preparation parameters for solar cell samples, such as maximum processing temperature, are not known [2]. Using a low preparation temperature of about 373K will reduce the cost and time of device fabrication, in addition enabling the use a thermally sensitive substrate such as polyimide film [2].

CdTe is stable in the environment and has no toxicity, and its cost is relatively low compared to other crystalline based solar cell materials such as Si which currently dominating solar cell market [3]. Due to its direct band gap (E_g), CdTe becomes one of the attractive materials for PV applications. The absorber thickness in commercial CdS/CdTe PVs is in the range of 5-10μm [4].In the current study it is found that the absorbance of incident solar radiation is about 90% for 1μm CdTe film thickness.

CdS is also one of the promising materials for optoelectronic applications [5]. Measurements of capacitance – voltage (*C-V*) and current – voltage (*I-V*) are used to study the transport mechanism in the heterostructure and to determine the basic physical parameters (such as the ideality factor) and the junction features (such as band discontinuity and charge interface). In order to improve the efficiency of PV devices, the loss mechanism must be determined [6].

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II. Experimental Work

CdS/CdTe heterojunctions were produced using thermal evaporation. Corning glass was used as a substrate, coated by 0.05μm thick of gold layer as a back contact. A p-CdTe layer with a thickness of about 1.2±0.05μm was evaporated on gold layer then an n-CdS layer with thickness of about 0.2±0.05μm was evaporated on CdTe layer. A 0.05μm thick SnO_2 layer of was evaporated on the n-CdS as an antireflection and transparent conducting oxide. Finally a conducting electrode of 0.05μm thick Alwas evaporated as shown in Fig. 1. The films were deposited at a substrate temperature of 373±5K. All materials used in this work were 99.999% purity. The thicknesses of the deposited films were measured using the Fizue method. As shown in Fig. 1, CdS, CdTe, and SnO_2 were been prepared in a sandwich configuration between Al and Au electrodes, using an Edwards E306A coating system for the deposition processes, under a vacuum of about 10^{-6} mbar. The prepared CdS/CdTe heterojunction devices were annealed at 573±5 K for periods of 60, 120 and 180 minutes under vacuum of 30 mbar.

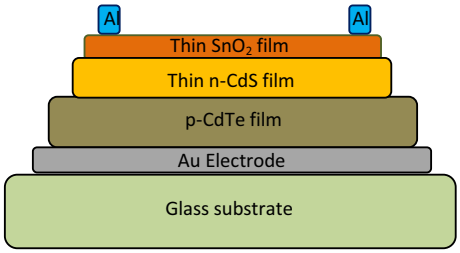

Fig. 1 Basic structure of a typical SnO_2/CdS/CdTe heterojunction

The structures of CdS/CdTe films were examined by X-ray diffraction (XRD) with Cu_{k_α} a wavelength of 0.0154μm. A Keithley 616 digital electrometer has been used to measure the resistance of the CdTe film. *C-V* measurements were made on the CdS/CdTe heteroguction under reverse bias voltage between zero and 1 volt at a frequency of 10^2Hz using a model 4274A HP-2RC unit and a 4275A multi frequency LCR meter .*I-V* curves were measured in the dark with forward and reverse bias.

I-V characteristics of the CdS/CdTe heterojunctions were measured at 40, 60, 80 and 100mW/cm^2 illumination

intensities using a 120 W Philips halogen lamp, and a Keithley model 2425 source meter.

The absorbance spectra for CdS and CdTe films were recorded for wavelengths in the range 0.3-1.1 μm using a double beam UV-VIS Perkin-Elmer Lambda 900 spectrophotometer.

III. Results and Discussions

A. X-ray Diffraction Analysis

X-ray diffraction spectra were taken for the as-prepared and CdS/CdTe heterojunctions annealed for different annealing times are shown in Fig. 2. The spectra of CdTe and CdS films were compared with ASTM (American Standard for Testing Materials) cards of CdTe and CdS structures which give a polycrystalline structure of CdTe cubic phase and CdS hexagonal phase. X-ray diffraction spectra for the as-prepared CdS/CdTe heterojunctions and those annealed for different times exhibit a strong preferred orientation along the CdTe (111) planes, as well as weak reflections at CdTe (220), CdTe (311) and CdS (002) planes. Similar data have been obtained by Chun et al [7] and Zhu et al [8]. The XRD spectra for CdS/CdTe heterojunction films annealed at 523K for different time durations show crystallinityim provement, the intensity of the (111) cubic plane has been increased, indicating that the degree of preferential orientation toward this direction increased, as shown in Fig. 2. The full width at half maximum (FWHM) intensity of the (220) plane has decreased. The observation that increasing annealing time improves the crystallite is in line with the observation of Al-Dhafiri [9] and Enriques and Mathew [10], while CdS (002) and CdTe (311) planes show the opposite behavior without affecting the preferred orientation. The crystal structure improvement due to the annealing produces an excess of Te atoms which are not bonded to the CdTe site this leading to an enhanced density of Cd vacancies, then Cd and Te atoms will rearrange themselves into CdTe crystallites [9]. Fig. 3 shows that the intensity increases with increasing annealing times, and this may be due to better grain growth by maintaining the preference for the (111) plane [10]. The degree of preferred orientation of CdS/CdTe films can be estimated from the peak intensities using the method of Harris for texture analysis [11].

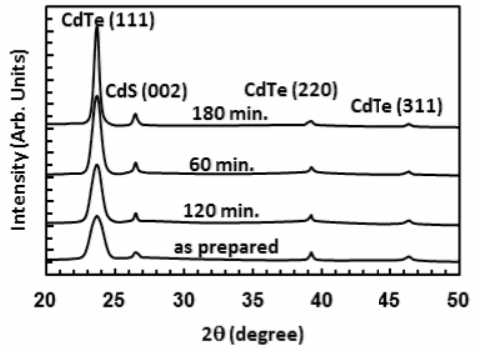

Fig. 2 X ray diffraction spectra for the as prepared and annealed CdS/CdTe heterojunction

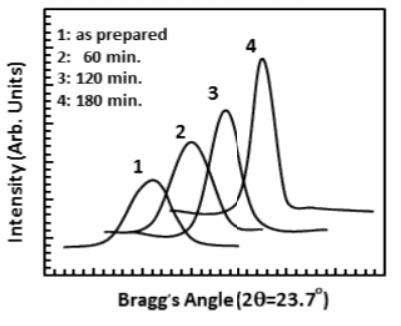

Fig. 3 X ray diffraction spectra of (111) CdTe peak for the as prepared and annealed CdS/CdTe films

The degree of the preferred orientation, that is,the orientation parameter of a certain crystal plane (*hkl*) in a polycrystalline films can be determined from the following equation:

$$T_c(hkl) = \frac{n\left(\frac{I_{(hkl)}}{I_{o(hkl)}}\right)}{\sum_n \left(\frac{I_{(hkl)}}{I_{o(hkl)}}\right)} \quad (1)$$

where $T_{c(hkl)}$ is the texture coefficient, $I_{(hkl)}$ is the measured intensity of the peak (*khl*), $I_{o(hkl)}$ is the relative intensity of the corresponding peak from the powder reference and n is the number of peaks (hence n =4 for each spectrum). When $T_c(111) = n$, this means that all the grains of CdTe films are oriented in the (111) plane, and lower values of $T_c(111)$ more random orientation. With increasing annealing time the $T_c(111)$ increases and become close to 4, as shown in Fig. 4, which shows variation of texture coefficient and crystallite orientation ($I_{(111)}/\Sigma I_{(hkl)}$) versus the annealing time. Similar behavior has been found by Nakamura et al [11] and Lee et al [12], namely crystallite orientation behaved like the texture coefficient.

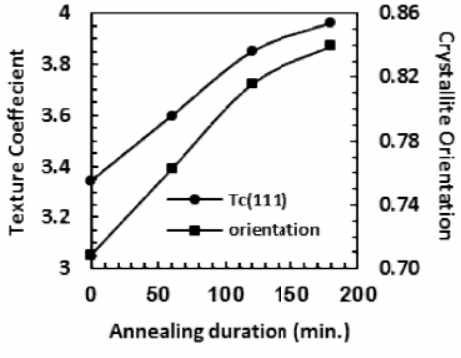

Fig. 4 The effect of annealing temperature on the texture coefficient of the as deposited and the annealed CdS/CdTe films

B. C-V Characteristics of CdS/CdTe Heterojunction

The Mott-Shottky plot (C^{-2} vs. V) for a CdS/CdTe heterojunction for different annealing times is shown in Fig. 6.

The straight line relationships mean that the junction was an abrupt type [13]-[15]. The as-prepared and CdS/CdTe heterojunctions annealed for 60 and 120 minutes show minor change in the reverse bias capacitance, suggesting that the back contact is incomplete, and this causes a reduction in the value of the capacitance. The reverse bias voltage does not significantly change the CdS/CdTe depletion region width [16]. At 180 minutes annealing time, the capacitance strongly depends on the applied bias and on the slope of the curves shown in Fig. 6. In this case we can say that the Au/CdTe contact is well formed. Similar results have been found by Jun et al. [16]. Table I shows the variation of the depletion region width for CdS/CdTe heterojunctions at different annealing times. We can observe that the zero bias depletion region width has increased with increasing annealing times. The depletion layer width (W) is defined as [15]:

$$W = \left(\frac{2\varepsilon_1\varepsilon_2(V_{bi} - V_a)(V_A - V_D)^2}{qN_D N_A(\varepsilon_1 N_D - \varepsilon_2 N_A)} \right)^{1/2} \quad (2)$$

where ε_1 and ε_2 are the dielectric constants for the n- and p-type semiconductor, respectively, $V_{bi}$and $V_a$are the built-in and applied voltages, q is the electron charge, N_D and N_A are the donor and acceptor concentration. The doping concentration can be calculated from the following relation [15]:

$$W = \left(\frac{2(\varepsilon_1 V_A - \varepsilon_2 V_D)^2}{qA^2 N_D N_A \varepsilon_1 \varepsilon_2)} \right)^{1/2} (V_{bi} - V_a) \quad (3)$$

where A is the area of the junction. The intercept of the line that results from plotting of C^{-2} as a function of reverse bias represents the built-in potential and the carrier concentration can be calculated from the slope of this line using (3). Table I shows the variation of V_{bi} with different annealing times. The V_{bi} values decreased with increasing annealing times. It is found that the overall performance of the manufactured device is improved due to annealing.

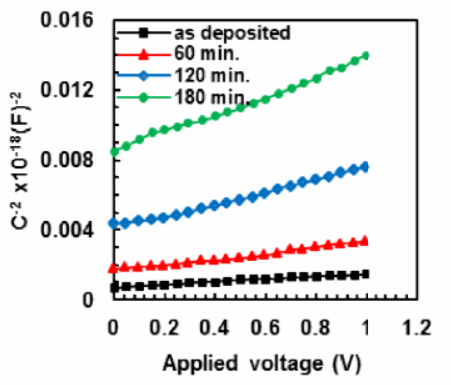

Fig. 6 Mott-Shottky plot for the as prepared and annealed CdS/CdTe heterojunctions for different annealing time durations

The higher values of V_{bi} may be attributed to midgap states that act as recombination centers that may arise either from states created as a result of junction fabrication or lattice mismatch between CdTe and CdS [17]. The capacitance measurement relies on the fact that the width of the space-charge-region (SCR) of a semiconductor device junction changes with applied voltage. The variation of depletion region width for CdS/CdTe cells with different annealing times is shown in Table I. One can observe that the zero bias depletion region with increased with increasing annealing times. Alnajjar et al. [17] found that the values of W increased with increasing annealing temperature and varied within the range (0.159-0.208)μm.

TABLE I
THE VARIATION OF C_o, V_{BI}, W AND N_A FOR AS PREPARED CDS/CDTE HETEROJUNCTIONS AT DIFFERENT ANNEALING TIMES

Annealing time	$C_o \times 10^9$ (F)	V_{bi}(V)	W(μm)	$N_A \times 10^{16}$ (cm^{-3})
As deposited	38.30	1.61	0.13	4.01
60 min	23.70	1.17	0.18	1.89
120 min	15.15	0.97	0.28	0.92
180 min	10.84	0.92	0.43	0.61

The acceptor concentration of CdS/CdTe heterojunctions decreases with increasing annealing time. Similar results have been found by Alnajjar [17]. The values of doping concentration suggest that the CdS/CdTe interface is n^+p type. Elsewhere we have shown that in the case of an n^+p type junction, recombination in the absorber space charge layer dominates over interface recombination [18].

C. I-V Characteristics of CdS/CdTe Heterojunction

Fig. 7 shows the dark *I-V* Characteristic of a CdS/CdTe heterojunction annealed at 573K for 180 minutes. In general the forward bias *I-V* characteristics for the CdS/CdTe heterojunction at show that the forward current consists of two regions; the first represents recombination currents while the second represents the tunneling currents [19]. The carrier transport mechanism for this case is of a tunneling–recombination type. The reverse saturation current was calculated from the intercept of the straight line with the current axis at zero voltage bias. The value of reverse saturation current is 9.6×10^{-10}A. These results are in agreement with Alnajjar et al. [17]. The ideality factor (β) can be calculated from the following relationship [15]:

$$\beta = \frac{q}{k_B T} \frac{V_F}{\ln\left(\frac{I_F}{I_S}\right)} \quad (4)$$

Here V_F is the forward bias voltage, I_F and I_S are the forward bias and the saturation currents respectively, β can be calculated by applying (4) to the first region of the upper curve in Fig. 7. The value ofthe is 1.58, in agreement with Huijin et al [20].

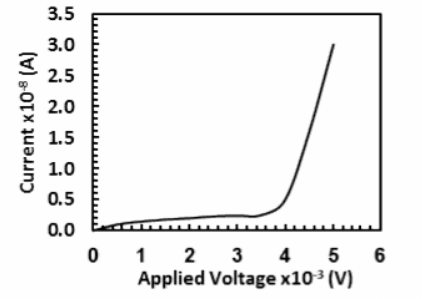

Fig. 7 Dark *I-V* characteristics (forward and reverse bias voltage) for a CdS/CdTe heterojunction annealed at 573K for 180 minutes

D.Energy Band Diagram of CdS/CdTe Solar Cell

Fig. 8 shows the optical absorbance as a function of wavelength for CdS and CdTe films deposited on glass substrates and annealed at 573K for 180 min. The absorption edge of CdS films is at 0.52μm wavelength, while for CdTe films the absorption edge is at 0.84 μm. Since CdS and CdTe are direct band gap semiconductors, the following formula can be used to estimate E_g [21];

$$\alpha = const.\frac{\left(h\nu - E_g\right)^m}{\left(h\nu\right)} \tag{5}$$

where α is the absorption coefficient, $h\nu$ is the energy of the incident radiation and m is a constant equal to 1/2 for allowed direct transition. The values of E_g are estimated from the extrapolation to zero absorption in (5). It is clear from the $(\alpha h\nu)^2$ vs. $h\nu$ curves depicted in Fig. 8 that the band gap of CdS (E_{g1}) is about 2.4eV. A similar value was found by Senthamilselvi et al [22].The band gap of CdTe (E_{g2}) is 1.44 eV, similar to the value found by Shabaan et al [21].

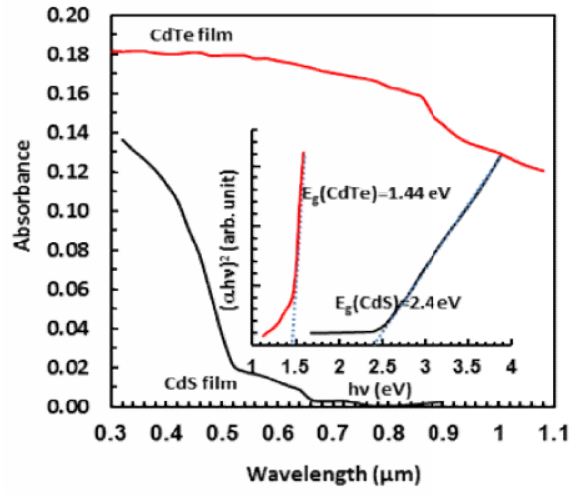

Fig. 8 The absorbance spectra vs. wavelength and $(\alpha h\nu)^2$ vs. $h\nu$ for CdS and CdTe films

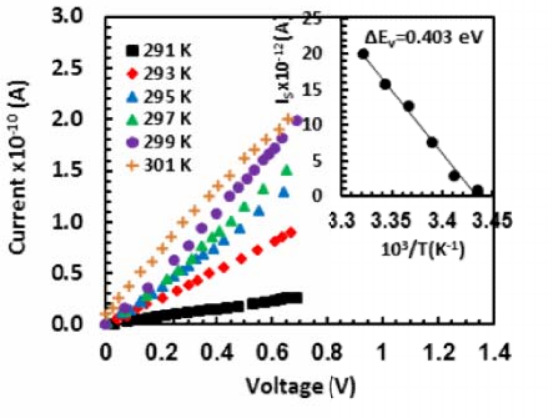

Fig. 9.*I-V* characteristics (forward bias) at different temperatures for CdS/CdTe heterojunction sample annealed at 573K for 180minutes and the related saturation current vs. $10^3/T$

CdS/CdTe heterojunctions have been investigated by using *I-V* and *C-V* measurements [23]. *I-V* measurements under forward bias in the temperature range (291-301)K are presented in Fig. 9. The measurements were taken at low voltages to cancel the role of the tunneling effect. From the inset of Fig. 9 it can be seen that I_S decreases with decreasing temperature due to resistance increasing. From the slope of this figure the value of valence band offset (ΔE_v) can be deduced using the following equation [19];

$$I_S = \exp\left(\frac{-q(V_D - \Delta E_V)}{k_B T}\right) \tag{6}$$

The value of ΔE_v which is calculated from the previous (6) is 0.40 eV. The total built-in voltage (V_{bi}) is 0.92 eV, which is due to the difference in work functions and it is equal to the sum of the built-in voltages on both sides [19]. The value of the conduction band offset (ΔE_c) is calculated from the following equation [24];

$$\Delta E_C - \Delta E_V = E_{g1} - E_{g2} \tag{7}$$

The calculated value of ΔE_c is 0.56 eV. The position of the Fermi level (E_F) in the other two sides of the heterojunction can be calculated using the following equations [24]:

$$E_C - E_F = k_B T \ln\left(\frac{N_C}{N_D}\right) \tag{8}$$

$$E_F - E_V = k_B T \ln\left(\frac{N_V}{N_A}\right) \tag{9}$$

where N_C and N_V are the density of electrons (in the conduction band) and holes (in the valence band), respectively. The values of (E_C-E_F) and (E_F-E_V) are found to

be 0.49 and 0.53 eV respectively. The band lineup model of n-CdS/p-CdTe heterojunction was constructed from our data as shown in Fig. 10 where the subscripts 1 and 2 of electron affinity χ, in Fig. 10 correspond to CdS and CdTe, respectively.

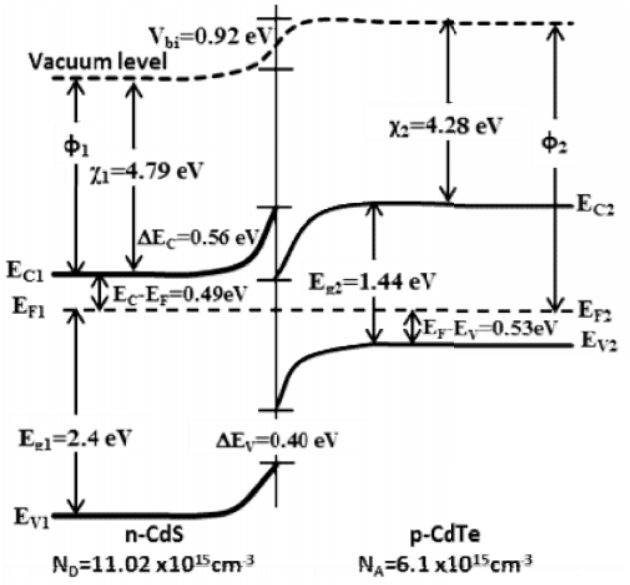

Fig. 10 Equilibrium energy band (band line up) diagram of n-CdS/p-CdTe heterojunction annealed for 180 minutes

IV. Conclusions

The X-ray diffraction spectra for the as-prepared and annealed CdS/CdTe heterojunctions gave a polycrystalline structure of cubic phase CdTe and hexagonal phase CdS. The values of dark resistivity of the bulk p-CdTe films decrease within the range (52.55- 1.89)× $10^7\Omega$.cm, with increasing annealing times. The as prepared CdS/CdTe heterojunctions are abrupt. The Au/CdTe contact was well formed by annealing for 180 minutes at 573 K. The depletion region width, built in voltage and capacitance decrease with increasing annealing time. The carrier concentration increased with increasing annealing time. The values of doping concentration suggest that the CdS/CdTe interface is n^+p type. The carrier transport mechanism is tunneling – recombination. We based our results on a modified energy band diagram which has already been proposed based on the analysis of electrical measurements.

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