Resonant-Based Capacitive Pressure Sensor Read-Out Oscillating at 1.67 GHz in 0.18 μm CMOS

Yong Wang, Wang Ling Goh, Jung Hyup Lee, Kevin T. C. Chai, and Minkyu Je

Abstract—This paper presents a resonant-based read-out circuit for capacitive pressure sensors. The proposed read-out circuit consists of an LC oscillator and a counter. The circuit detects the capacitance changes of a capacitive pressure sensor by means of frequency shifts from its nominal operation frequency. The proposed circuit is designed in 0.18μm CMOS with an estimated power consumption of 43.1mW. Simulation results show that the circuit has a capacitive resolution of 8.06kHz/fF, which enables it for high resolution pressure detection.

Keywords—Capacitance-to-frequency converter, Capacitive pressure sensor, Digital counter, LC oscillator.

I. INTRODUCTION

RECENTLY, capacitive pressure sensors are widely used in pressure measurement systems, considering the advantages in terms of high sensitivity, superior reliability and small temperature coefficients [1], [2]. To translate the changes of capacitance into analog signals, numerous circuits have been studied [3]–[9]. Many of the popular readout circuits are capacitance-to-voltage converters (CVCs) which are generally categorized with other techniques that use switch-capacitor circuit [3]–[5], transimpedance amplifier [6] and ac-bridge with voltage amplifier [7]–[9]. The first major drawbacks with such interface circuits is related to the sensitivity of the system where the minimum detectable changes of capacitance is affected by non-idealities of the readout circuit such as thermal noise, 1/f noise, parasitic capacitance or switch noise. Minimizing the effects from these non-idealities requires extra cancellation methods and consequently complicates the circuits. Furthermore, a common feature in many integrated sensor systems will have the voltage readouts converted into digital signals using an additional analog-to-digital converter (ADC). The additional ADC results in large area, which is a significant increase on power consumption and cost.

To simplify the design of readout circuits and enhance sensitivity, methods converting the capacitance into frequency domain have been studied [10]–[13]. The resolution of a capacitance-to-frequency converter (CFC) relies on the output

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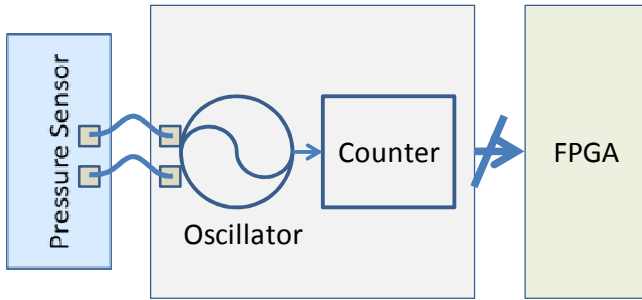
frequency range and also the phase-noise. Increasing the operation frequency of the circuit gives a higher resolution. Generally, CFCs are categorized into two techniques: technique employing a CVC followed by a voltage-to-frequency converter (VFC) [10], [11], and technique using a ring oscillator [12], [13]. The former commonly engages a switch-capacitor circuit to convert the capacitance into voltage, and the VFC translates the changes in voltage into frequency-varing signal. Circuits using this technique are supplied by input signals with multiple phases, which results in demanding requirements on signal generators. Switching speed of transistors also places a limit on the operation frequency. Hence, the latter technique, using a ring oscillator, which converts the capacitance into frequency will be difficult to operate at very high frequencies with substandard phase noise and inferior stability.

In this paper, we present the design using a cross-coupled LC oscillator together with a digital counter for capacitive pressure sensor. The design is a monolithic with on-chip inductors. The LC oscillator is designed to be suitable for wire-bonding with a stand-alone capacitive pressure sensor. The output frequencies vary from 1.6748GHz to 1.6778GHz with the sensor capacitance varying from 5.838pF to 6.206pF and the theoretically derived sensitivity of 8.06kHz/fF. The resolution of the pressure sensor system is 33.7Pa within the pressure range from 0.3 to 1.3bar and a sampling rate of 1kHz.

II. PROPOSED INTERFACE CIRCUIT FOR CAPACITIVE PRESSURE SENSOR

A. Overall Construction of Pressure Sensor Chip

The overall construction of the pressure sensor systems is shown in Fig. 1. The MEMS pressure sensor has a capacitance varying from 5.838pF to 6.206pF. The pressure sensor and read-out chip are packaged together using bonding wires. On-chip LC oscillator is designed to tolerate the bonding wires that are less than 4mm. The LC oscillator translates the capacitance changes into frequency changes. Subsequently, the counter samples output frequency of the LC oscillator with an off-chip reference frequency. The digital data can be transferred to FPGA for further calibrations.

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Fig. 1 Block diagram of the proposed pressure sensor system

Fig. 3 Models of (a) the on-chip inductor, and (b) capacitive pressure sensor

The technique shown in Fig. 1 is a possible read-out solution for any other capacitive sensors as well. The cross-coupled LC oscillator can operate normally with two short bonding wires, which enables robust and low-cost packaging.
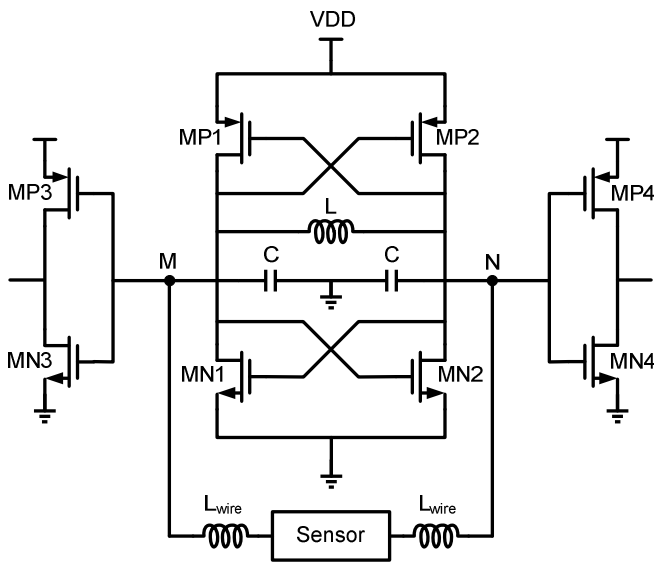

Fig. 2 Schematic of cross-coupled LC oscillator

B. Cross-Coupled LC Oscillator Circuit

The schematic of the LC oscillator is shown in Fig. 2. The on-chip octagonal inductor L is 3.8nH with Q factor of 6.1 at 1.67GHz. Model of this inductor is shown in Fig. 3 (a). The series resistance of the inductor is 2.8ohm, and the parasitic oxide capacitance is 3pF. Substrate parasitic capacitance C_{sub} and resistance R_{sub} are 50fF and 500ohm separately. A larger inductance comes with a lower Q factor and a larger area. The selection of the inductance is a tradeoff considering Q factor, as low-Q on-chip inductor always limit the Q factor of the LC tank. The capacitive pressure sensor has a typical capacitance of 5.79pF, the model of which can be found in Fig. 3 (b). Capacitor C is used to decrease the oscillation frequency of the LC tank with value of 5pF. The bonding wire is estimated as 1nH/mm, and modeled as an inductor L_{wire} with inductance of 2nH and resistance of 2ohm.
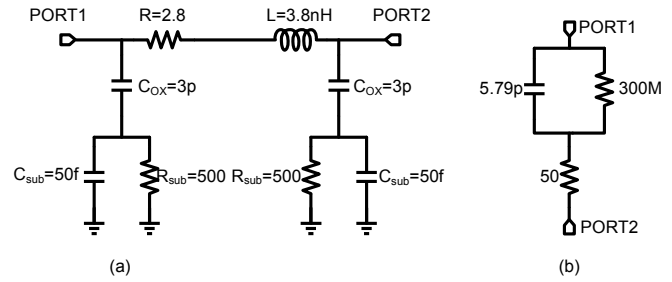
PMOS transistors MP1 and MP2 have the same length and width that are 0.18μm and 200μm correspondingly. NMOSs MN1 and MN2 have the same size with length of 0.18μm and width of 96μm. Transistor pairs, MN3-MP3 and MN4-MP4, are buffers to isolate the oscillator circuit from the load. The circuit is supplied by VDD of 1.8V. The DC biasing voltages at nodes M and N are 0.86V, close to half VDD, to reduce the signal distortion and enhance the signal swing.
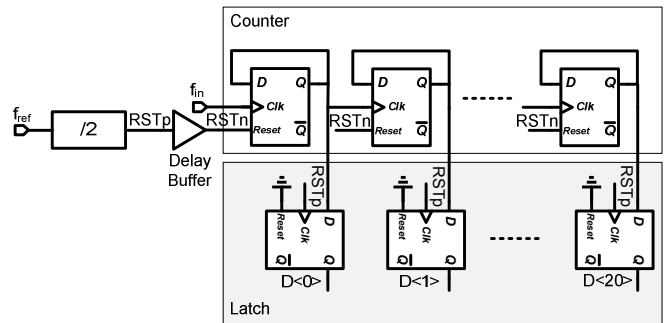

Fig. 4 Schematic of the counter

C. Digital Counter Design

After converting the changes of the capacitances into frequencies, a counter is required to further translate the frequencies into digital data. As shown in Fig. 4, the counter has an input reference frequency, f_{ref}, which will determine the sampling rate as well as the resolution. The reference frequency is supposed to provide reset signal RSTn to the flip-flops, so that the counter can count the input frequency when RSTn is low. In our design, the counter will be in reset mode when the RSTn is enabled. Meanwhile, the flip-flops of the latch circuit will lock the counted value when the positive edges of reset signal RSTp arrives. Therefore, the duty cycle of the reset signal affects the read-out value of the counter. In the proposed counter, the reference frequency is firstly divided by two to provide a 50 % duty cycle signal, RSTp. Then, RSTn is shortly delayed and inverted into RSTn. To make sure the counter and latch circuits are stable, the latch should lock the output data from the counter before counter operate in reset mode. For that reason, the delay buffer shown in Fig. 4 always makes the positive edges of RSTp arrive later than that of RSTn. The counter is designed to have 21 bits output with minimum sampling rate of 1 K/s.

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III. RESULTS

The chip is supplied with VDD of 1.8V. From simulation, the oscillator circuit together with the digital counter draws 23.96mA with total power consumption of 43.1mW. The output waveform of the LC iscillator at node-M in Fig. 2, has a voltage swing of 1.5V, as depicted in Fig. 5.
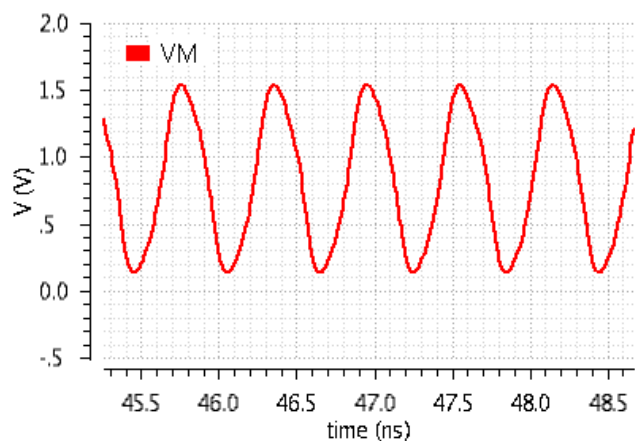

Fig. 5 The output waveform of the oscillator at node-M

The pressure sensor has a capacitance range of 5.838pF to 6.206pF for the pressure range from 0.3 bar to 1.3 bar. The first order and second order pressure coefficients (PCFs) of the sensor are 0.28 and -0.044, correspondingly. As shown in Fig. 6, the output frequency of the oscillator changes from to 1.6748 GHz to 1.6778GHz when the pressure varies from 0.3 bar to 1.3 bar. The output frequency range is 2.97MHz. The resolution is 29.7Hz/Pa when calculated with the pressure, and 8.06kHz/fF when calculated with the capacitance.

Compared with other capacitance-to-frequency converters in frequency domain (see Table I), this work obtains the best resolution that is 8.06kHz/fF. The input capacitance range is determined by pressure sensor we use. This work gives a pressure resolution of 33.7Pa at 1kHz sampling rate, and 22 bits maximum digital output.
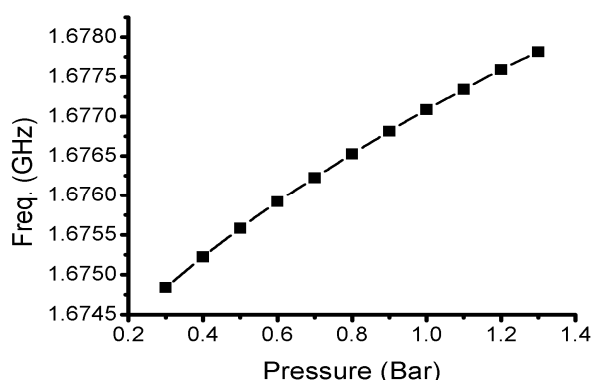

Fig 6 The output frequency vs. pressure

The chip is designed in 0.18μm CMOS process with the physical dimension of 2mm×1.5mm. The LC oscillator and the counter circuits are highlighted in Fig. 7. The four-cycle

inductor is monolithically integrated on chip using top-metal of 2.5μm thickness. Two RF pads will be connected to MEMS pressure sensor using bond wires.

TABLE I
BENCHMARKING

	[14]	[15]	[16]	[17]	This work
Tech.	NMOS 5μm	CMOS 4μm	CMOS 0.35μm	CMOS 0.35μm	CMOS 0.18μm
Cap. Range	20-50 pF	2-50 pF	4-24 pF	2 pF-7.8 nF	5.838-6.206 pF
Freq. Range	1.2KHz	1KHz	500KHz	23.6MHz	2.97MHz
Resolution	40Hz/pF	20Hz/pF	25Hz/fF	3Hz/fF	8.06KHz/fF
Chip Area	2.4mm^2	1.1mm^2	1.01mm^2	0.173mm^2	3mm^2
Power Supply	10V	1.5V	3.2V	3.2V	1.8V

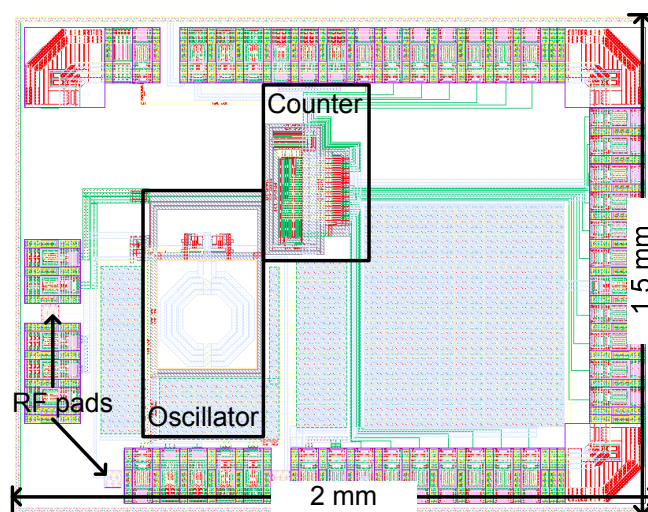* is capacitance range of the pressure sensor.

Fig. 7 Layout of the capacitive sensor read-out chip

IV. CONCLUSIONS

This paper presents a capacitive pressure sensor read-out circuit that takes use of oscillator as a capacitance-to-frequency converter. The circuit is designed in 0.18μm CMOS technology with an on-chip inductor. The circuit works together with the pressure sensor gives a 33.7Pa resolution at 1 KHz sampling rate. A superior high capacitance resolution, 8.06KHz/fF, is obtained at the oscillation frequency of 1.67 GHz, which makes it able to detect small changes in input capacitance.

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