

# Trap Assisted Tunneling Model for Gate Current in Nano Scale MOSFET with High-K Gate Dielectrics

Ashwani K. Rana, Narottam Chand and Vinod Kapoor

**Abstract**—This paper presents a new compact analytical model of the gate leakage current in high-k based nano scale MOSFET by assuming a two-step inelastic trap-assisted tunneling (ITAT) process as the conduction mechanism. This model is based on an inelastic trap-assisted tunneling (ITAT) mechanism combined with a semi-empirical gate leakage current formulation in the BSIM 4 model. The gate tunneling currents have been calculated as a function of gate voltage for different gate dielectrics structures such as  $\text{HfO}_2$ ,  $\text{Al}_2\text{O}_3$  and  $\text{Si}_3\text{N}_4$  with EOT (equivalent oxide thickness) of 1.0 nm. The proposed model is compared and contrasted with santaurus simulation results to verify the accuracy of the model and excellent agreement is found between the analytical and simulated data. It is observed that proposed analytical model is suitable for different high-k gate dielectrics simply by adjusting two fitting parameters. It was also shown that gate leakages reduced with the introduction of high-k gate dielectric in place of  $\text{SiO}_2$ .

**Keywords**—Analytical model, High-k gate dielectrics, inelastic trap assisted tunneling, metal-oxide-semiconductor (MOS) devices.

## I. INTRODUCTION

OVER the last few decades, a dramatic increase in the performance of VLSI ICs has been achieved as a result of continued scaling of MOS transistor. However, as a result of aggressing scaling to obtain high current drive and good control on short channel effect, gate oxide thickness approaches its manufacturing and physically limiting value of less than 2 nm [1]. For example, devices with oxides thinner than  $\sim 4$ -5 nm exhibit large off-state leakage currents (1 to 10 A/cm<sup>2</sup>) since carriers can easily tunnel directly between the substrate and gate electrode [2]-[3]. Consequently, gate leakage (tunneling) current has emerged as the most prominent form of leakage due to use of ever lower thickness of  $\text{SiO}_2$  layer in nano-CMOS devices, particularly in the 65 nm and below regime. This is a big concern for satellite systems and

ground-based mobile electronics where power conservation is important.

To reconcile the need for reduced off-state leakage currents in highly scaled devices, the replacement of  $\text{SiO}_2$  as gate dielectric with alternate high-k dielectric material is considered as a method to contain/reduce the gate leakage current, thus constructing a type of non-classical nano-MOS transistor [2]-[6]. The use of high- $\kappa$  gate dielectrics to replace  $\text{SiO}_2$  serves the dual purpose of reducing the gate leakage as well as scaling of future devices. The main advantage of alternative high- $\kappa$  dielectrics is that they can have higher dielectric constants which make it possible to manufacture a gate insulator that is physically thicker than  $\text{SiO}_2$ , but which maintains electrostatically similar performance<sup>2</sup> to ultrathin  $\text{SiO}_2$  layers. The increased physical thickness significantly reduces<sup>2</sup> the probability of charge tunneling across the insulator and therefore reduces the amount of off-state leakage current [5]-[6].

Research on high-k dielectrics quickly converged on the  $\text{Al}_2\text{O}_3$ ,  $\text{HfO}_2$ , and  $\text{ZrO}_2$  family, which has a band gap larger than 5.0 eV [7], [8]-[12]. However,  $\text{HfO}_2$  and  $\text{ZrO}_2$  received most attention in the late 1990s, based on their better thermal stability with Si [13]-[14].

Many high- $\kappa$  gate dielectrics have shown encouraging electrical characteristics as described above; however, other concerns for high- $\kappa$  dielectrics include several orders of magnitude more traps found in the bulk or interface [3],[6],[13]-[15]. The traps generation is believed due to high voltage stressing across the high-k gate dielectrics which lead to trap assisted tunneling [16]. These traps greatly influence the gate leakage component of the devices [17]. Therefore, trap-assisted tunneling, also supported by A. Palma et al in [18], is the main mechanism of carrier tunneling through high-k based nano scale MOSFETs when modeling the gate current for nanoscale MOS devices in modern simulators.

In the past, research has been carried out to model the gate tunneling currents through various high-k dielectrics [19]-[21]. In [19]-[21], numerical models are utilized, which neglects the trap assisted tunneling through high-k dielectrics. In addition, numerical modeling approach is time consuming and difficult to use in practice.

Huixian Wu et al [22] proposed a semi-empirical gate tunnel model based on WKB approximation which neglects the trap assisted tunneling through high-k dielectrics. In a

Ashwani K. Rana is with Department of Electronics and Communication Engineering, National Institute of Technology, Hamirpur-177005, H.P., India, (corresponding author to provide phone: 91-01972-304638; fax: 92-01972-223834; e-mail: ashwani@nitham.ac.in).

Narottam Chand is with Department of Computer Science and Engineering, National Institute of Technology, Hamirpur-177005, H.P., India (e-mail: nar@nitham.ac.in).

Vinod Kapoor is with Department of Electronics and Communication Engineering, National Institute of Technology, Hamirpur-177005, H.P., India, (e-mail: kapoor@nitham.ac.in).

recent paper [23], A. Bouazra et al established an approach to model the trap assisted tunneling through  $\text{HfO}_2/\text{SiO}_2$  multi stacks by solving a set of coupled Schrödinger-Poisson equation. The problem was treated numerically using the finite differential method.

In this work, a simplified analytical model of gate tunnel current through high-k dielectrics is presented which accounts trap assisted tunneling mechanism. This model is based on an inelastic trap-assisted tunneling mechanism combined with semi-empirical gate leakage current model of BSIM 4.

The rest of the paper is organized as follows. In Section II, theoretical modeling of trap assisted gate tunneling current is established. The high-k gate dielectric device structure and design used for simulation set up is presented in Section III. The results obtained are discussed in Section IV. Finally, concluding remarks are offered in Section V.

## II. INELASTIC TRAP ASSISTED TUNNELING (ITAT) MODEL

The schematic energy band diagram shown in Fig. 1 illustrate our model in more detail showing the conditions which lead to inelastic trap assisted tunneling. The Fig. 1 illustrate the energetic situation for a p-type Si substrate and a  $n^+$ -doped poly Si gate electrode.

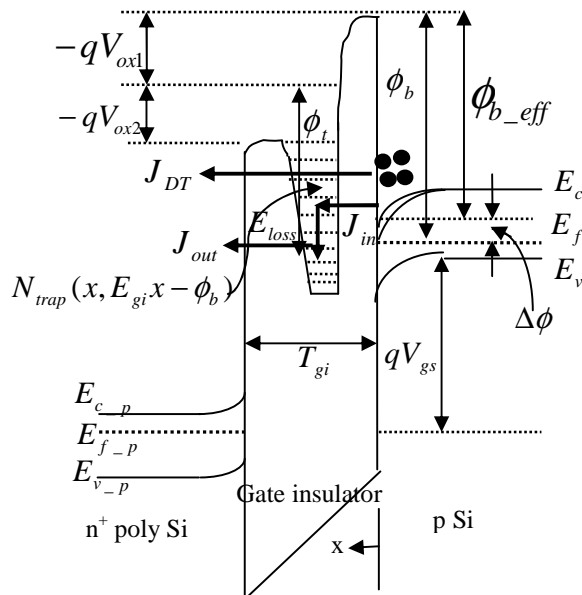


Fig. 1 Schematic energy band diagram of two-step inelastic trap-assisted tunneling through high-k gate insulator of a nano scale MOSFET Mapping nonlinear data to a higher dimensional feature space

It is observed that electrons injected from the High-k/Si interface will first tunnel to the nearer trap, then to the farther trap, and finally out of the gate insulator.

Assumptions:

- inelastic trap assisted tunneling is a two step process for simplicity
- Firstly, electrons tunnel into deep lying trap state, become released from the trap state and subsequently tunnel to gate under the influence of the applied electric field.

In this process, tunneling-in current from inversion layer to the traps and tunneling-out current from the traps to the gate are calculated by modifying the formulation of direct tunneling in the BSIM 4 model [24]-[25]. Assuming that  $x$  is the distance from the Si-high-k interface,  $N_{trap}(x, E)$  is the sheet trap density in  $\text{cm}^2$  at a distance  $x$  and having the energy level with respect to the conduction band edge of gate dielectric,  $O_t(x, E)$  is the electron occupancy of the traps at a distance of  $x$  and the energy of  $E$ ,  $\sigma_t$  is the capture cross section of the traps and  $A_g$  is the gate tunneling area. The tunnel-in current density ( $J_{in}$ ) into the traps and the tunnel-out current ( $J_{out}$ ) density from the traps are then expressed as

$$J_{in} = \frac{q}{A_g} \sigma_t N_{trap}(x, qE_{gi}x - \phi_{b\_eff}) \times [1 - O_t(x, qE_{gi}x - \phi_{b\_eff})] J_1(\phi_{b\_eff}, x, E_{gi1}) \quad (1)$$

$$J_{out} = \frac{q}{A_g} \sigma_t N_{trap}(x, qE_{gi}x - \phi_{b\_eff}) \times O_t(x, qE_{gi}x - \phi_{b\_eff}) J_2(\phi_t, t_{gi} - x, E_{gi2}) \quad (2)$$

$$\phi_t = \phi_{b\_eff} - qE_{gi}x + E_{LOSS} \quad (3)$$

where  $\phi_t$  is the barrier height of the gate insulator trap states,  $E_{gi}$  is the electric field in the gate insulator,  $E_{gi1}$  is the electric field over a distance  $x$  of the trap relative to the interface in the gate insulator and  $E_{gi2}$  is the electric field over a distance  $t_{gi} - x$  relative to the interface in the gate insulator,  $E_{LOSS}$  is the energy loss accompanied with the injection of electrons into the neutral trap sites and  $\sigma_t$  is assumed to be constant irrespective of the position and energy level of the traps.  $J_1$  and  $J_2$  are the uniform current density and are calculated by modifying the formulation of direct tunneling in the BSIM model.  $\phi_b$  is the actual barrier height of gate insulator i.e. gate dielectric and  $\phi_{b\_eff}$  is the effective barrier height, given as below,

$$\phi_{b\_eff} = \phi_b - \Delta\phi \quad (4)$$

$$\Delta\phi = \sqrt{\frac{qE_{gi}}{4\pi\epsilon_{gi}}} = \sqrt{\frac{qV_{gi}}{4\pi\epsilon_{gi}T_{gi}}} = \left( \frac{2q^3 N_{eff} \phi_{b\_eff}}{16\pi^2 \epsilon_{gi}^3} \right)^{1/4} \quad (5)$$

The  $\Delta\phi$  is the reduction in the barrier height at the high-k/Si interface [26] from  $\phi_b$  so that barrier height becomes  $\phi_{b\_eff}$ .

This reduction in barrier height is due to image charges across the interface. This barrier reduction is of great interest since it modulates the gate tunneling current.

The resulting tunneling current  $J_{ITAT}$  of this trap-assisted tunneling process is given by a detailed balance of  $J_{in}$  and  $J_{out}$ . Consequently, inelastic trap assisted tunneling current can be expressed as

$$J_{ITAT} = \frac{q}{A_g} \sigma_t N_{trap}(x, qE_{gi}x - \phi_{b\_eff}) P_{ITAT}(x, E, E_{gi}) \quad (6)$$

where  $P_{ITAT}$  can be expressed as

$$P_{ITAT} = \frac{J_1(\phi_{b\_eff}, x, E_{gi1})J_2(\phi_t, t_{gi} - x, E_{gi2})}{J_1(\phi_{b\_eff}, x, E_{gi1}) + J_2(\phi_t, t_{gi} - x, E_{gi2})} \quad (7)$$

Using Gauss's law and considering MOS capacitor equivalent circuit, the local electrical fields  $E_{gi1}$  and  $E_{gi2}$  of both the tunneling regions finally become

$$E_{gi1} = E_{gi} + \frac{t_{gi} - x}{t_{gi}} \cdot \frac{qN_{trap}}{\epsilon_{gi}} \quad (8)$$

$$E_{gi2} = E_{gi} + \frac{x}{t_{gi}} \cdot \frac{qN_{trap}}{\epsilon_{gi}} \quad (9)$$

The modified uniform current density  $J_1$  and  $J_2$  as obtained from BSIM 4 are expressed as

$$J_1(\phi_{b\_eff}, x, E_{gi1}) = A_t \frac{C(\phi_{b\_eff}, x, E_{gi1})}{\phi_{b\_eff}} \times \quad (10)$$

$$\exp\left[-\frac{8\pi\sqrt{2m_{gi}}}{3hq} \cdot \frac{\phi_{b\_eff}^{3/2}}{E_{gi1}} \beta(\phi_{b\_eff}, x, E_{gi1})\right]$$

$$J_2(\phi_{b\_eff}, x, E_{gi1}) = A_t \frac{C(\phi_t, t_{gi} - x, E_{gi2})}{\phi_t} \times \quad (11)$$

$$\exp\left[-\frac{8\pi\sqrt{2m_{gi}}}{3hq} \cdot \frac{\phi_t^{3/2}}{E_{gi2}} \beta(\phi_t, t_{gi} - x, E_{gi2})\right]$$

$$\text{where } A_t = \frac{q^3}{8\pi\phi_{b\_eff}\epsilon_{gi}}$$

$$c_{(ch,ov)}(\phi_{b\_eff}, x, E_{gi1}) = \exp\left[\frac{20}{\phi_{b\_eff}} \left(\frac{x|E_{gi1(ch,ov)}| - \phi_{b\_eff}}{\phi_{b\_eff}} + 1\right)^{\alpha(ch,ov)}\right] \cdot \left[1 - \frac{x|E_{gi1(ch,ov)}|}{\phi_{b\_eff}}\right] \times (E_{gi1}) N_{DTC(ch,ov)}$$

$$c_{(ch,ov)}(\phi_t, t_{gi} - x, E_{gi2}) = \exp\left[\frac{20}{\phi_t} \left(\frac{(t_{gi} - x)|E_{gi2(ch,ov)}| - \phi_t}{\phi_t} + 1\right)^{\alpha(ch,ov)}\right] \cdot \left[1 - \frac{(t_{gi} - x)|E_{gi2(ch,ov)}|}{\phi_t}\right] \times (E_{gi2}) N_{DTC(ch,ov)}$$

$$\beta(\phi_{b\_eff}, x, E_{gi1}) = 1 - \left(1 - \frac{qx}{\phi_{b\_eff}} |E_{gi1}|\right)^{3/2}$$

$$\beta(\phi_t, t_{gi} - x, E_{gi2}) = 1 - \left(1 - \frac{q(t_{gi} - x)}{\phi_t} |E_{gi2}|\right)^{3/2}$$

$$N_{DTC(ov)} = \begin{cases} \frac{\epsilon_{gi}}{t_{gi}} \left\{ n_{acc} v_t \cdot \ln \left[ 1 + \exp\left(-\frac{V_g}{n_{acc} v_t}\right) \right] \right\} \\ \text{for } V_g < 0 \\ \frac{\epsilon_{gi}}{t_{gi}} \left\{ n_{acc} v_t \cdot \ln \left[ 1 + \exp\left(-\frac{V_{ge}}{n_{acc} v_t}\right) \right] \right\} \\ \text{for } V_g > 0 \end{cases}$$

$$N_{DTC(ch)} = \begin{cases} \frac{\epsilon_{gi}}{t_{gi}} \left\{ n_{acc} v_t \cdot \ln \left[ 1 + \exp\left(-\frac{(V_g - V_{FB})}{n_{acc} v_t}\right) \right] \right\} \\ \text{for } V_g < 0 \\ \frac{\epsilon_{gi}}{t_{gi}} \left\{ n_{inv} v_t \cdot \ln \left[ 1 + \exp\left(-\frac{(V_g - V_{th})}{n_{inv} v_t}\right) \right] \right\} \\ \text{for } V_g > 0 \end{cases}$$

In the above equation,  $\alpha(ch,ov)$  is the fitting parameter depending upon channel or source/drain overlap tunneling,  $\phi_b$  is the actual tunneling barrier height,  $n_{inv}$  and  $n_{acc}$  are the swing parameters,  $V_{FB}$  represents the flat band voltage,  $N_{DTC(ch,ov)}$  denotes the density of carrier in channel/overlap region depending upon MOSFET biasing condition and  $V_{ge}$  is the effective gate voltage excluding poly gate non-uniformity and gate length effect and is equal to  $V_g - V_{poly}$ . The default values of  $n_{inv}$  and  $n_{acc}$  are  $\frac{S}{v_t}$  ( $S$  is the sub threshold swing) and 1 respectively. The correction  $C_{F(ch,ov)}$  and transmission probability  $(T_{WKB(ch,ov)})$  are different for channel and source/drain overlap region because both channel and overlap component have different value of  $V_{ox(ch,ov)}$  and  $N_{DTC(ch,ov)}$ . It is because of the fact that overlap region has almost zero flat band voltage as both SDE region and overlying poly-gate Si are heavily doped  $n^+$  regions. The  $N_{DTC(ch,ov)}$  has been given differently for both region as above. The gate oxide voltage for the channel and SDE overlap are calculated as follows.

Case (i): when  $V_g > 0$

In this biasing condition MOSFET device, there is a depletion layer in the poly gate thereby causing an additional potential drop across the gate. The SDE region enters into accumulation and substrate region enters into the weak inversion below  $V_{th}$  and strong inversion beyond  $V_{th}$ . Therefore both the channel and EDT component are present and are comparable.

Case (ii): when  $V_{FB} < V_g < 0$

Here, gate tunneling current is dominated by the EDT where electric field is such that electron are directed from the accumulated poly-gate into the overlap region. On other hand, substrate is in depletion /weak inversion and constitutes negligible tunneling current. This region of biasing is primarily responsible for off-state power dissipation. Thus, EDT plays an important role in the evaluation of off-state power dissipation

Case (ii): when  $V_g < V_{FB}$

In this region of operation, substrate goes into accumulation. As a result both current components become comparable. The voltage across the gate oxide for different region of operation is as follows.

$$V_{gi} = \begin{cases} (V_g - \phi_s - V_{FB}) \text{ for } V_g < 0 \\ (V_{ge} - \phi_s - V_{FB}) \text{ for } V_g > 0 \end{cases} \quad (12)$$

Where  $\phi_s$  is the surface band bending of the substrate and are calculated for channel and overlap region depending upon the biasing condition of the MOSFET device including the poly non-uniformity, gate length effects and image force barrier lowering. The accurate surface potentials expressions in case of channel in weak inversion/depletion, strong inversion and in accumulation can be taken from [27]. The gate effective voltage including the effect of nonuniform dopant distribution in the gate is derived as follows.

$$\therefore V_{ge} = (V_{FB} + \phi_{so} - \Delta V_{p1} - \Delta V_{p2}) + \frac{(q\epsilon_{si}N_{poly}T_{gi}^2)}{\epsilon_{gi}^2} \left[ \sqrt{1 + \frac{2\epsilon_{ox}^2(V_g - V_{FB} - \phi_{so})}{q\epsilon_{si}N_{poly}T_{gi}^2}} - 1 \right] \quad (13)$$

The  $\phi_{so}$ , by taking the quantization effect into account, is given [28] as follows.

$$\phi_{so} = 2\phi_s + \Delta\phi_s^{QM} - V_{BS} \quad (14)$$

Where  $\Delta\phi_s^{QM}$  can be taken from [27]. This equation (15) includes the non uniformity in the gate dopant profile through a term  $\Delta V_{p1}$  and fringing field effect *i.e* gate length effect through a term  $\Delta V_{p2}$ . The potential drop  $\Delta V_{p1}$  due to non uniform dopant profile in poly Si gate, caused by low energy implantation, is given [29] by

$$\Delta V_{p1} = \left( \frac{kT}{q} \right) \ln \left( \frac{N_{poly\_top}}{N_{poly\_bottom}} \right) \quad (15)$$

The  $N_{poly\_top}$  and  $N_{poly\_bottom}$  are the doping concentration at the top and bottom of the polysilicon gate. The potential

drop  $\Delta V_{p2}$  due to gate length effect, caused by very short gate lengths is given as below

$$\Delta V_{p2} \approx \frac{\Delta Q}{C_d} = \frac{2qAN_d}{L_g C_d} \left( v/cm \right) \quad (16)$$

$$C_d = \delta \frac{\epsilon_{gi}}{\pi} \ln \left[ \frac{3 - \cos \left\{ \pi \left( \frac{T_F - T_{gi}}{T_F} \right) \right\}}{1 + \left\{ \pi \left( \frac{T_F - T_{gi}}{T_F} \right) \right\}} \right] \quad (17)$$

where A denote the triangular area of the additional charge,  $L_g$  is the gate length,  $C_d$  is the depletion capacitance in the sidewalls [30],  $\epsilon_{gi}$  is the permittivity of the gate insulator,  $T_F$  is the thickness of the field oxide,  $T_{gi}$  is the thickness of the gate insulator and  $\delta$  is fitting parameter equal to 0.95 normally.

### III. SIMULATION SET UP

Figure 2 shows the schematic of device structure of N-MOSFET with high-k gate dielectric used in this study.

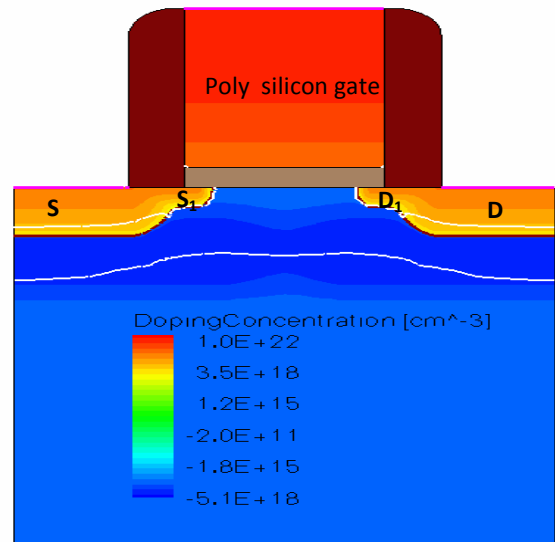


Fig. 2. NMOSFET device structure with high-k gate dielectrics used in simulation

The deep S/D region is composed of a heavily doped silicon and a silicide contact. The doping of the silicon S/D region is assumed to be very high,  $1 \times 10^{20} \text{ cm}^{-3}$ , which is close to the solid solubility limit and introduces negligible silicon resistance. The dimension of the silicon S/D region is taken as 20 nm long and 50 nm high. This gives a large contact area resulting in a small contact resistance.

The heavily doped silicon called deep S/D region extend into the silicon film at both ends and constitute the extended S/D for the device (labelled by ‘‘S<sub>1</sub>’’ and ‘‘D<sub>1</sub>’’ in Fig. 2). The lengths of these extended regions at both ends are equal and are denoted by S<sub>1</sub> and D<sub>1</sub>. S/D implantation is performed after defining the gate and the oxide spacer. Boron ions were implanted into the channel region to reduce the leakage current and to keep a low acceptor concentration in the non-

overlapped channel region. The doping concentration of the acceptors in silicon channel region is assumed to be graded due to diffusion of dopant ions from heavily doped S/D region with a peak value of  $1 \times 10^{18} \text{ cm}^{-3}$  and  $1 \times 10^{17} \text{ cm}^{-3}$  near the channel. The halo implantation done around the S/D also reduces short-channel effects, such as the punch-through current, DIBL, and threshold voltage roll-off, for different non-overlap lengths.

The MOSFET has a 50-nm-thick n+ poly-Si gate with metallurgical gate length of 25 nm and a 1-nm gate oxide. The oxide spacer has been assumed to reduce the gate capacitance. Here,  $L_o$  represents the overlap length, which is controlled by the S/D implantation energy.  $L_o = 5 \text{ nm}$  optimized with off current is used in this work. The MOSFET with  $L_{\text{met}}$  of 25 nm was designed to have a  $V_T$  of 0.19 V. We determined  $V_T$  by using a linear extrapolation of the linear portion of the  $I_{\text{DS}}-V_{\text{GS}}$  curve at low drain voltages. The operating voltage for the devices is 1V. The simulation study has been conducted in two dimensions, hence all the results are in the units of per unit channel width. The simulation of the device is performed by using Santaurus design suite [31]-[32] with drift-diffusion, density gradient quantum correction and advanced physical model being turned on.

#### IV. RESULTS AND DISCUSSION

In this section, computation of gate tunneling currents for a n-channel fully depleted nanoscale MOSFET through different dielectric structures have been carried out. This model is computationally efficient and easy to realize. This model calculates the gate tunneling current with energy loss ( $E_{\text{loss}}$ ) during inelastic trap assisted tunneling process and  $\alpha_{(\text{ch/ov})}$  as fitting parameters. It also assume in our calculation that  $N_{\text{trap}}(x, E)$  is a constant irrespective of position and energy level. Thus, present model is applicable to many alternate high-k nano MOSFET simply by adjusting the two fitting parameter. The variation of total gate tunneling current with gate bias for a given values of gate insulator thickness has been presented for possible alternative gate dielectrics such as  $\text{Si}_3\text{N}_4$ ,  $\text{Al}_2\text{O}_3$  and  $\text{HfO}_2$ . The impact of dielectric constant (K) of gate dielectric on total gate tunneling current is reported in results.

The comparison between the simulated data and the model value for gate tunneling current is presented in Fig.3, 4 and 5 for  $\text{HfO}_2$ ,  $\text{Al}_2\text{O}_3$  and  $\text{Si}_3\text{N}_4$  gate dielectrics respectively. Fig. 3 shows the gate tunneling current versus gate bias for  $\text{HfO}_2$  gate dielectric materials with the equivalent oxide thickness (EOT) of 1 nm at substrate doping (Na) of  $1 \times 10^{17} \text{ cm}^{-3}$  while that of polysilicon gate is  $1 \times 10^{22} \text{ cm}^{-3}$  at the top and  $1 \times 10^{20} \text{ cm}^{-3}$  at bottom of the polysilicon gate i.e. interface of high-k gate dielectric and silicon. The comparison between the simulated data and the model value for gate tunneling current is presented in Fig.3, 4 and 5 for  $\text{HfO}_2$ ,  $\text{Al}_2\text{O}_3$  and  $\text{Si}_3\text{N}_4$  gate dielectrics respectively. Fig. 3 shows the gate tunneling current versus gate bias for  $\text{HfO}_2$  gate dielectric materials with the equivalent oxide thickness (EOT) of 1 nm at substrate doping (Na) of  $1 \times 10^{17} \text{ cm}^{-3}$  while that of polysilicon gate is  $1 \times 10^{22} \text{ cm}^{-3}$  at the top and  $1 \times 10^{20} \text{ cm}^{-3}$  at bottom of the polysilicon

gate i.e. interface of high-k gate dielectric and silicon. The simulation was carried out with  $L_{\text{met}} = 25 \text{ nm}$ ,  $L_{\text{ov}} = 5 \text{ nm}$ ,  $t_{\text{HfO}_2} = 5.64 \text{ nm}$ ,  $\phi_b(\text{HfO}_2) = 1.5 \text{ eV}$  [33],  $m_{\text{eff}} = 0.18 m_0$  [33],  $\sigma_t = 9.3 \times 10^{-16} \text{ cm}^2$  [34],  $N_{\text{trap}} = 7.67 \times 10^{12} \text{ cm}^{-2}$  [34]. The trap position ( $x_t$ ) is extracted to be  $0.43 t_{\text{HfO}_2}$  in the inelastic tunneling model by comparing the magnitude of  $J_{\text{ITAT}}$  with that of direct tunneling current of MOS capacitors with gate oxides of 5.64 nm. The fitting parameters  $E_{\text{loss}}$ ,  $\alpha_{(\text{ch})}$  and  $\alpha_{(\text{ov})}$  has been taken to 0.2 eV, 0.75 and 0.45 respectively to fit the model with the simulated value.

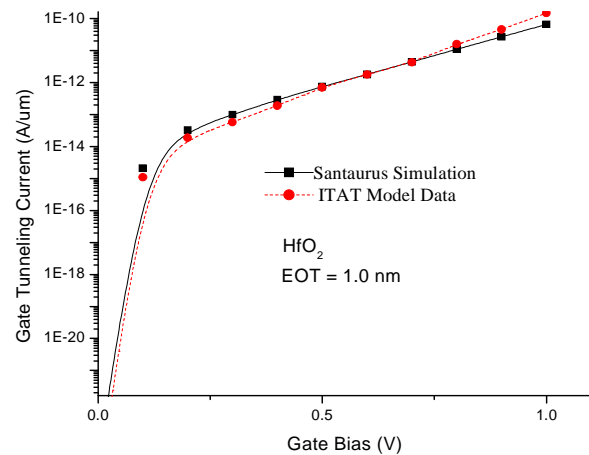


Fig 3. Comparison of analytical model data with Santaurus simulated data for  $\text{HfO}_2$  based high-k MOSFET with equivalent oxide thickness (EOT) of 1.0 nm, metallurgical gate length of  $L_{\text{met}}=25 \text{ nm}$  and S/D overlap length of  $L_{\text{ov}}=5 \text{ nm}$  in nano scale regime

The model result obtained analytically through inelastic trap assisted tunneling current model is compared with the simulated data for  $\text{HfO}_2$  gate dielectrics in Fig. 3. It is shown in Fig. 3 that results calculated by ITAT have better agreement with the simulated results. This shows that for high-k gate dielectrics the dominant tunneling mechanism is trap assisted tunneling. This may be due to the fact that the possibility of carrier tunneling directly from channel to gate is low at large physical thickness of gate insulator (high-k gate dielectric) for a given equivalent oxide thickness (EOT).

Fig. 4 shows the gate tunneling current versus gate bias for  $\text{Al}_2\text{O}_3$  gate dielectric materials with the equivalent oxide thickness (EOT) of 1 nm at substrate doping (Na) of  $1 \times 10^{17} \text{ cm}^{-3}$  while that of polysilicon gate is  $1 \times 10^{22} \text{ cm}^{-3}$  at the top and  $1 \times 10^{20} \text{ cm}^{-3}$  at bottom of the polysilicon gate i.e. interface of high-k gate dielectric and silicon. The simulation was carried out with  $L_{\text{met}} = 25 \text{ nm}$ ,  $L_{\text{ov}} = 5 \text{ nm}$ ,  $t_{\text{Al}_2\text{O}_3} = 2.31 \text{ nm}$ ,  $\phi_b(\text{Al}_2\text{O}_3) = 2.8 \text{ eV}$  [33],  $m_{\text{eff}} = 0.30 m_0$  [33],  $\sigma_t = 7.03 \times 10^{-17} \text{ cm}^2$  [35],  $N_{\text{trap}} = 2.4 \times 10^{12} \text{ cm}^{-2}$  [35]. The trap position ( $x_t$ ) is extracted to be  $0.45 t_{\text{Al}_2\text{O}_3}$  in the inelastic tunneling model by comparing the magnitude of  $J_{\text{ITAT}}$  with that of direct tunneling

current of MOS capacitors with gate oxides of 2.31 nm. The fitting parameters  $E_{loss}$ ,  $\alpha_{(ch)}$  and  $\alpha_{(ov)}$  has been taken to 0.4 eV, 0.55 and 0.38 respectively to fit the model with the simulated value.

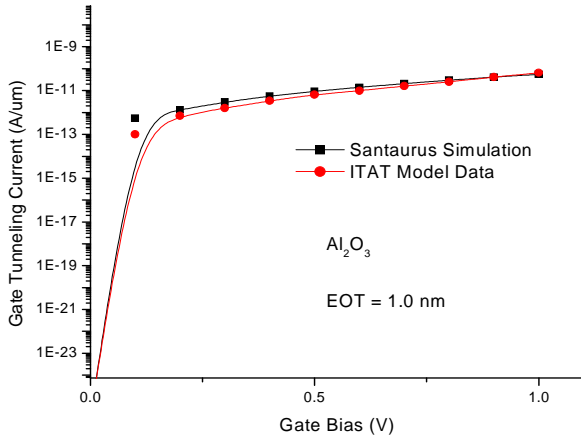


Fig 4. Comparison of analytical model data with Santaurus simulated data for  $Al_2O_3$  based high-k MOSFET with equivalent oxide thickness (EOT) of 1.0 nm, metallurgical gate length of  $L_{met}=25nm$  and S/D overlap length of  $L_{ov}=5 nm$  in nano scale regime

It is shown in Fig. 4 that ITAT model shows good agreement with the santaurus simulation. Again, it is observed that for high-k gate insulator dominant gate tunneling mechanism is inelastic trap assisted tunneling ITAT. This is because of the fact that high-k gate dielectrics have higher trap density through which the tunneling of carrier becomes easier that results in increased tunneling current from channel to gate through traps.

Fig. 5 shows the gate tunneling current versus gate bias for  $Si_3N_4$  gate dielectric materials with the equivalent oxide thickness (EOT) of 1 nm at substrate doping (Na) of  $1 \times 10^{17} cm^{-3}$  while that of polysilicon gate is  $1 \times 10^{22} cm^{-3}$  at the top and  $1 \times 10^{20} cm^{-3}$  at bottom of the polysilicon gate i.e. interface of high-k gate dielectric and silicon. The simulation was carried out with  $L_{met} = 25 nm$ ,  $L_{ov} = 5nm$ ,  $t_{Si_3N_4}=1.92 nm$ ,  $\phi_b(Si_3N_4)=2.0 eV$  [33],  $m_{eff} = 0.20 m_0$ [33],  $\sigma_i = 3 \times 10^{-13} cm^{-2}$  [36-37],  $N_{trap} = 3 \times 10^{11} cm^{-2}$  [38-39]. The trap position ( $x_t$ ) is extracted to be  $0.47 t_{Si_3N_4}$  in the inelastic tunneling model by comparing the magnitude of  $J_{ITAT}$  with that of direct tunneling current of MOS capacitors with gate oxides of 1.92 nm. The fitting parameters  $E_{loss}$ ,  $\alpha_{(ch)}$  and  $\alpha_{(ov)}$  has been taken to 0.2 eV, 0.87 and 0.64 respectively to fit the model with the simulated value.

The Figure 5 shows that present ITAT model produces agreeable results between modeled gate current and santaurus simulation data for  $Si_3N_4$  high-k gate insulator structures. This is obvious as discussed above. Thus it is clear from Fig.3,4 and 5 that ITAT model is dominant for high-k gate insulator structures of MOSFET and is used throughout this work.

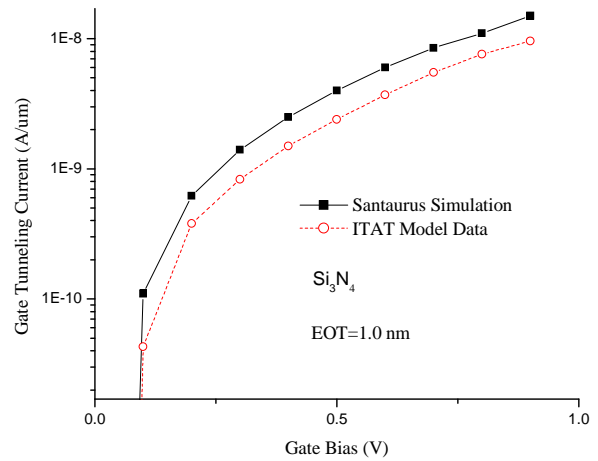


Fig 5. Comparison of analytical model data with Santaurus simulated data for  $Si_3N_4$  based high-k MOSFET with equivalent oxide thickness (EOT) of 1.0 nm, metallurgical gate length of  $L_{met}=25nm$  and S/D overlap length of  $L_{ov}=5 nm$  in nano scale regime.

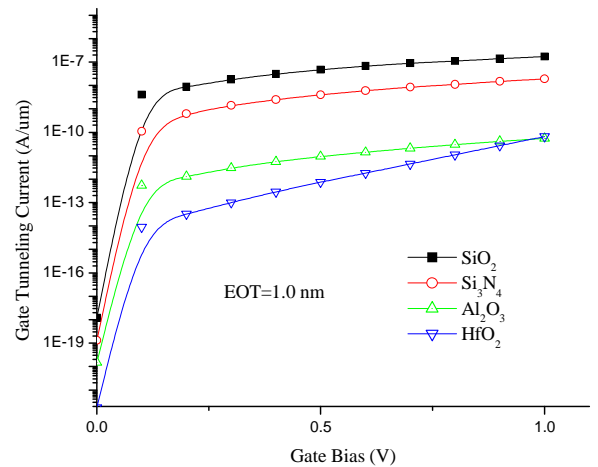


Fig 6. Gate tunneling current vs gate bias for different high-k gate dielectrics- $HfO_2, Al_2O_3, Si_3N_4$  in nano scale regime with EOT of 1.0 nm at  $L_{met}=25nm$  and  $L_{ov}=5.0 nm$

The calculated gate current of various high-k gate insulator structures with different high-k dielectrics as a function of the gate voltage are plotted in Fig.6. For all the various high-k materials being studied, the equivalent oxide thickness (EOT) is taken to be 1.0 nm. Other device parameters mentioned earlier are used. Fig.6 shows that  $HfO_2, Al_2O_3, Si_3N_4$  high-k gate dielectrics demonstrate significant gate leakage reduction compared to  $SiO_2$  gate dielectric. This is because vertical electric field responsible for carrier tunneling decreases as the physical thickness of gate insulator increases with increase in dielectric constant(k). The reduction of gate tunnel current is ineffective somewhere near and above the barrier height of the high-k dielectric layer ( $HfO_2$ ,  $K=22$ ), due to the dominating tunneling near and over the barrier height of the high-k layer, although this is not a serious concern for the bias range of nanoscale MOS devices. Thus, the resulting gate current is

determined by the interplay among the barrier height, dielectric constant and gate bias voltage as well.

#### V. CONCLUSION

A simplified physical model applicable to gate leakage current in high-k based MOSFETs was presented. The model is based on inelastic trap-assisted tunneling (ITAT) mechanism combined with a semi-empirical direct tunneling current model. It was found that the results simulated by the ITAT model show good agreement with the santaurus simulated results for different gate-dielectric simply by adjusting two fitting parameters.

#### REFERENCES

- [1] Buchanan, D., IBM J. Res. Develop. (1999) 43, 245
- [2] J. A. Felix, D. M. Fleetwood, R. D. Schrimpf, J. G. Hong, G. Lucovsky, J. R. Schwank, and M. R. Shaneyfelt, "Total-dose radiation response of hafnium- silicate capacitors," *IEEE Transactions on Nuclear Science*, vol. 49, no. 6, pp. 3191-3196, Dec. 2002.
- [3] J. A. Felix, M. R. Shaneyfelt, D. M. Fleetwood, T. L. Meisenheimer, J. R. Schwank, R. D. Schrimpf, P. E. Dodd, E. P. Gusev, and C. D' Emeric, "Radiation-induced charge trapping in thin AlO/SiO N/Si(100) gate dielectric stacks," *IEEE Transactions on Nuclear Science*, vol. 50, no. 6, pp. 1910-1918, Dec. 2003.
- [4] M. Houssa, G. Pourtois, M. M. Heyns and A. Stesmans, "Defect generation in high  $\kappa$  gate dielectric stacks under electrical stress: the impact of hydrogen," *Journal of Physics: Condensed Matter*, vol.17, pp. s2075-s2088, 2005
- [5] E. P. Gusev, E. Cartier, D. A. Buchanan, M. Gribelyuk, M. Copel, H. Okorn-Schmidt, and C. D'Emic, "Ultrathin high- $\kappa$  metal oxides on silicon: processing, characterization and integration issues," *Microelectronic Engineering*, vol. 59, no.1-4, pp. 341-349, 2001.
- [6] G. D. Wilk, R. M. Wallace, and J. M. Anthony, "High- $\kappa$  gate dielectrics: current status and materials properties considerations," *Applied Physics Letters*, vol. 89, pp. 5243-5275, 2001.
- [7] B. H. Lee, L. Kang, W. J. Qi, R. Nieh, Y. Jeon, K. Onishi, and J. C. Lee, "Ultrathin hafnium oxide with low leakage and excellent reliability for alternative gate dielectric application," *IEEE International Electron Devices Meeting (IEDM) Technical Digest*, pp.133-135, 1999.
- [8] Lee, W., et al., Tech. Dig. IEDM (1998), 605.
- [9] Wilk, G. D., and Wallace, R. M., Appl. Phys. Lett. (2000) 76, 112
- [10] Qi, W.-J., et al., Tech. Dig. IEDM (1999), 145
- [11] Lee, B. H., et al., Appl. Phys. Lett. (2000) 76, 1926.
- [12] Buchanan, D. A., et al., Tech. Dig. IEDM (2000), 223.
- [13] E. P. Gusev, C. Cabral, Jr., B. P. Linder, Y.H. Kim, K. Maitra, E. Cartier, and Y. Zhang, "Advanced gate stacks with fully silicided (FUSI) gates and high- $\kappa$  dielectrics: enhanced performance at reduced gate leakage," *IEEE International Electron Devices Meeting (IEDM) Technical Digest*, pp. 79-82, Dec. 2004.
- [14] A. Aziz, K. Kassami, Ka. Kassami, F. Olivie, " Modelling of the influence of charges trapped in the oxide on the  $I(V_g)$  characteristics of metal-ultra-thin oxide-semiconductor structures." *Semicond. Sci. Technol.* 19 (2004) 877-884.
- [15] D. Heh, C.-D. Young, G.-A. Brown, P.-Y. Hung, E.-M. Vogel, J.-B. Bernstein, "Spatial distribution of trapping centers in  $HfO_2/SiO_2$  ." *Appl. Phys. Lett.* 88 (2006) 152907.
- [16] D. J. DiMaria and E. Cartier, *Journal of Applied. Physics.* 78,3883, (1995)
- [17] V. Fomenko, E. P. Gusev, E. Borguet, "Optical second harmonic generation studies of ultrathin high- $\kappa$  dielectric stacks," *Journal of Applied Physics*, vol. 97, article no. 083711, 2005.
- [18] A. Palma, F. Jimenez-Molinos, F. Gámiz, P. Cartujo, and J. A. López-Villanueva, "Direct and trap-assisted elastic tunneling through ultrathin gate oxides," *J. Appl. Phys.*, Vol. 91, No. 8, April 2002, pp 5116-5124
- [19] Eric M. Vogel, Khaled Z. Ahmed, Brian Hornung, W. Kirklen Henson, Peter K. McLarty, Gerry Lucovsky, John R. Hauserand Jimmie J. Wortman, " Modeled Tunnel Current for High Dielectric Constant Dielectrics." *IEEE Transactions on Electron Devices*, Vol. 45, No. 6, pp 1350-1355, June 1998.
- [20] Mudanai S, Fan Y, Ouyang Q, Tasch AF, Banerjee SK., "Modeling of direct tunneling current through gate dielectric stacks. *IEEE Transaction on Electron Device* 2000;Vol 47, No (10):1851.
- [21] Wei Wang , Ning Gu, J.P. Sun, P. Mazumder, "Gate current modeling of high-k stack nanoscale MOSFETs." *Solid-State Electronics* 50 (2006) 1489–1494—paper 20
- [22] Huixian Wu, Yijie (Sandy) Zhao, Marvin H. White , "Quantum mechanical modeling of MOSFET gate leakage for high-k gate dielectrics." *Solid-State Electronics* 50 (2006) 1164–1169.
- [23] A. Bouazra, S. Abdi-Ben Vassallah, A. Poncet and M. Said, " Current tunneling through MOS devices." *Materials Science and Engineering: C*, Vol. 28, Issues 5-6, July 2008, pp 662-665.
- [24] W.-C. Lee and C. Hu, "Modeling gate and substrate currents due to conduction- and valence-band electron and hole tunneling," *Symposium on VLSI Technology Digest of Technical Papers*, pp. 198, 2000.
- [25] W.-C. Lee and C. Hu, "Modeling CMOS tunneling currents through ultrathin gate oxide due to conduction- and valence-band electron and hole tunneling." *IEEE Trans. Electron Devices*, vol. 48, pp. 1366–1373, June 2001
- [26] L. E. Calvet, R. G. Wheeler, and M. A. Reed, *Applied Physics Letters*, vol 80, No 10, March 2002.
- [27] Pr\_egalidiny , Christophe Lallement, Daniel Mathiot," Accounting for quantum mechanical effects from accumulation to inversion, in a fully analytical surface potential-based MOSFET model," *Solid-State Electronics* 48 (2004) 781–787
- [28] Taur, Y., and Ning, T.H.: 'Fundamentals of modern VLSI devices' (Cambridge University Press, New York, 1998).
- [29] Chang-Hoon Choi, P. R. Chidambaram, Rajesh Khamankar, Charles F. Machala, Zhiping Yu, and Robert W. Dutton, "Dopant Profile and Gate Geometric Effects on Polysilicon Gate Depletion in Scaled MOS," *IEEE Transactions on Electron Devices*, vol. 49, no. 7, July 2002
- [30] Steve Shao-Shiun Chung and Tung-Chi Li, *IEEE Transactions On Electron Devices*, Vol. 39, No. 3, March 1992
- [31] ISE TCAD: Synopsys Santaurus Device User Manual, 1995-2005, Synopsys, Mountain View, CA.
- [32] ISE TCAD: Synopsys Santaurus Device simulator
- [33] Hitender Kumar Tyagi, and P. J. George, " Tunneling currents through ultra thin  $HfO_2/Al_2O_3/HfO_2$  triple layer gate dielectrics for advanced MIS devices", *J Mater Sci: Mater Electron* (2008) 19 :902–907.
- [34] S. Y. Chen, H. W. Chen, F. C. Chiu, C. H. Liu, Z. Y. Hsieh, H. S. Huang and H. L. Hwang, "Interfacial and Electrical Characterization of  $HfO_2$ -Gated MOSCs and MOSFETs by C-V and Gated-Diode Method", *ECS Trans.*, vol 16, No. 5 October, 2008 , pp. 131-138.
- [35] V.E. Drozd A.P. Baraban and I.O. Nikiforova, "Electrical properties of Si— $Al_2O_3$  structures grown by ML-ALE" , *Applied Surface Science*, Volumes 82-83, 2 December 1994, Pages 583-586
- [36] Park, Y. C. Jackson, W. B. Johnson, N. M. Hagstrom, S. B. , " Spatial profiling of electron traps in silicon nitride thin films ", *Journal of Applied Physics*, vol 68, No 10, Nov 1990, pp 5212 – 5221
- [37] A.V. Vishnyakov , Yu.N. Novikov, V.A. Gritsenko , K.A. Nasyrov, "The charge transport mechanism in silicon nitride: Multi-phonon trap ionization", *Solid-State Electronics* vol 53, No 3, March 2009, pp 251–255.
- [38] T. P. Ma, "Making Silicon Nitride Film a Viable Gate Dielectric", *IEEE Transactions on Electron Devices*, vol. 45, No. 3, March 1998, pp 680-690
- [39] Katsuyuki Sekine, Yuji Saito, Masaki Hirayama, and Tadahiro Ohmi, "Highly Robust Ultrathin Silicon Nitride Films Grown at Low-

Temperature by Microwave-Excitation High-Density Plasma for Giga Scale Integration", IEEE Transactions on Electron Devices, Vol. 47, No. 7, July 2000, pp 1370-1374.



Ashwani K. Rana was born in Kangra, H.P., India in 1974. He received his B.Tech degree in Electronics and Communication Engineering NIT, Hamirpur, India in 1998 M.Tech degree in VLSI Technology from Indian Institute of Technology, Roorkee, India in 2006. He is currently pursuing the Ph.D degree in nano devices from National Institute of Technology, Hamirpur, India.

Presently he is with Department of Electronics and Communication Engineering, National Institute of Technology, Hamirpur, India, as an Assistant Professor.

His research interest include modeling of semiconductor devices, low power high performance VLSI circuit design and emerging integrated circuit technologies. He has more than 10 publications in International/National Journal & conferences and guided more than 10 M.Tech students in these areas. He is member of ISTE.



**Dr. Narottam Chand** received his PhD degree from IIT Roorkee in Computer Science and Engineering. Previously he received MTech and BTech degrees in Computer Science and Engineering from IIT Delhi and NIT Hamirpur respectively.

Presently he is working as Head, Department of Computer Science and Engineering, NIT Hamirpur. He also served as Head, Institute Computer Centre, NIT Hamirpur from February 2008 to July 2009. He has coordinated different key assignments at NIT Hamirpur like Campus Wide Networking, Institute Web Site, Institute Office Automation.

His current research areas of interest include mobile computing, mobile ad hoc networks and wireless sensor networks. He has published more than 50 research papers in International/National journals & conferences and guiding six PhDs in these areas. He is member of ISTE, CSI, International Association of Engineers and Internet Society.



**Dr. Vinod Kapoor** was born at Mandi town in Himachal Pradesh, India. He received his BE Degree in Electronics & Communication Engineering from National Institute of Technology (formerly Regional Engineering College), Durgapur, Bengal, in the year 1987 and Masters Degree Electronics & Control from Birla Institute of

Technology & Science, Pilani (Rajasthan) in the year 1996. He did his Ph. D. from Kurukshetra University, Kurukshetra in the field of Optical Fiber Communication in Sept.2006.He also obtained his MBA degree with specialization in Human Resources Management in the year 2002.

He is presently Professor in the Department of Electronics & Communication Engineering NIT Hamirpur, India. He has coordinated different key assignments at NIT Hamirpur like Training & Placement Officer, Chief Warden (Hostels), organizing short term courses.

His research interest includes optical fiber communication and optoelectronics/nano devices. He has published more than 15 research papers in International/National journal & conferences and guiding four Ph.Ds in these areas. He is member of ISTE, IETE and IE.