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Digital Automatic Gain Control Integrated on WLAN Platform

Emilija Miletić, Miloš Krstić, Maxim Piz, and Michael Methfessel

***Abstract*—**In this work we present a solution for DAGC (Digital Automatic Gain Control) in WLAN receivers compatible to IEEE 802.11a/g standard. Those standards define communication in 5/2.4 GHz band using Orthogonal Frequency Division Multiplexing OFDM modulation scheme. WLAN Transceiver that we have used enables gain control over Low Noise Amplifier (LNA) and a Variable Gain Amplifier (VGA). The control over those signals is performed in our digital baseband processor using dedicated hardware block DAGC. DAGC in this process is used to automatically control the VGA and LNA in order to achieve better signal-to-noise ratio, decrease FER (Frame Error Rate) and hold the average power of the baseband signal close to the desired set point. DAGC function in baseband processor is done in few steps: measuring power levels of baseband samples of an RF signal, accumulating the differences between the measured power level and actual gain setting, adjusting a gain factor of the accumulation, and applying the adjusted gain factor the baseband values. Based on the measurement results of RSSI signal dependence to input power we have concluded that this digital AGC can be implemented applying the simple linearization of the RSSI. This solution is very simple but also effective and reduces complexity and power consumption of the DAGC. This DAGC is implemented and tested both in FPGA and in ASIC as a part of our WLAN baseband processor. Finally, we have integrated this circuit in a compact WLAN PCMCIA board based on MAC and baseband ASIC chips designed from us.

***Keywords*—**WLAN, AGC, RSSI, baseband processor.

I. Introduction

A flexible-data communications system Wireless Local Area Network (WLAN) is implemented as an extension to or as an alternative to a wired LAN. WLAN transfers data over the air, minimizing the need for wired connections. The standards defined for WLAN (IEEE 802.11a/g) have a throughput up to 54 Mbit/s by using the 5/2.4 GHz bands. By utilizing OFDM modulation the communication between devices is not limited to short distances. Depending on the transmit power, WLAN transceivers cover a broad variety of distances ranging from couple of centimeters up to several hundred meters. Therefore, the received signal strength at the receiver antenna may fluctuate up to 80 dB. To be able to cope with such signal variations in digital baseband processor it is necessary to implement automatic gain control. DAGC detects incoming power from antenna, and, based on the calculated power, generates correct LNA and VGA gain. DAGC follows the variations of received signal and constantly updates the gain level of VGA and LNA. If DAGC is not running properly, baseband processing would be very difficult because of the clipped received signal (if signal is over-amplified) or too low input signal (if signal is under-amplified).

Our implemented WLAN system is based on commercial Maxim 2829 RF front-end. This chip generates an analog RSSI signal and to analyze it in DAGC we have to apply ADC (Analog Digital Conversion). The RSSI signal is used as a basis for the calculation of the gain signals. RSSI detector is placed in RF chip between LNA and VGA, and with every change of LNA gain, the value of RSSI signal is affected. However, those changes cannot be observed immediately, and some time is needed to stabilize RSSI output for further sampling.

For our WLAN system it is very important to have highly programmable DAGC structure that can be used to cover both A and G frequency bands. Therefore, we have to introduce a set of programmable registers that have to store the all necessary information needed to operate DAGC correctly.

Finally, an important objective is to preserve the simple structure of the DAGC in order to reduce the power and area of baseband chip and with this to support the usability of our chip-set to the mobile and handheld applications.

In the following text we will describe the role of DAGC in WLAN modules, its main characteristics, and the architecture of building blocks. We will also compare our approach to the other AGC proposals for WLAN systems. Based on the provided measurement results we will explain the details of our AGC controller and algorithm. Finally, we will give the implementation results for the DAGC embedded in our integrated WLAN platform.

II. Related Work

The concept of AGC is known for decades. Also for WLAN applications there were several proposals for DAGC presented. In the following text we will focus on just few proposed solutions, which are closely related to our design. Combining the related work and the results from the measurements, we have achieved good results regarding DAGC implementation.

An interesting DAGC solution is provided for WLAN receiver based on a low intermediate frequency (IF)

Authors are with the IHP, Im Technologiepark 25, 15236 Frankfurt Oder, Germany (e-mail: {miletic, krstic, piz, methfessel}@ihp-microelectronics.com).

architecture [2]. In this case the course RSSI signal has been used, and sampled with only 6 bits. This RSSI signal is used only for the activation and power-on of more complex DAGC processing block based on the power estimation of I/Q data signal. This is a relatively slow approach since for the correct power estimation several data samples are needed. According to the provided measurements results, 3μs is needed approximately for the power estimation and gain setting. RSSI signal is used as a trigger for the power management controller. Below provided threshold AGC and Rx baseband processing is in stand-by mode in order to reduce the power consumption. Another interesting solution [3] is based on the lookup table application. Similar as the previous solution the power estimation is based on the sampling of I and Q data signals. This architecture is based on memorizing the dynamic change of the input power for optimal quantization of gain control signals. Power estimation is done precisely, but this solution introduces with LUTs a big hardware overhead.

III. DAGC Architecture

As a basis for our WLAN system development we have used Maxim 2829 RF front-end chip. The structure of the DAGC depends very much on the RF chip architecture. Block scheme of receiver architecture including DAGC is given on Fig. 1. A signal from antenna comes to LNA (Low Noise Amplifier) block. LNA amplification is programmable and it can be set to three different levels. After LNA stage the signal is mixed and transferred to the baseband frequency. The position of the RSSI detector is at the baseband stage. However, it is obvious that the values of the RSSI signal are affected by the defined level of LNA gain. Finally, signal is amplified with VGA. The changes of the VGA gain are transparent to the RSSI detector. In this case, the AGC controller for the power estimation can use in principle two sources: digitized RSSI signal, and data I/Q signals. Based on those signals the optimal values of VGA and LNA gain has to be generated.

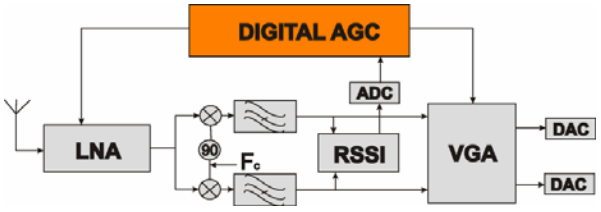

Fig. 1 DAGC placed on the front end of Receiver

The architecture that we are proposing in this paper is somewhat different to the solutions given in the previous section. The main objective that we want to achieve is the shorter time for the power estimation. Therefore, DAGC implementation is based on the linearization of RSSI curve. Based on the achieved linear power estimation the calculation of the optimal VGA and LNA level is performed. Our basic premise was that we can achieve linear dependence between the RSSI signal and input power at the receiver at the different frequency channels and bands. With this solution we can eliminate expensive memories, lookup tables, large number of multipliers, and consequently we can achieve low system complexity. Results of measurements in section IV confirm our approach and prove that linearization approach can be successfully used.

IV. Results of Measurement

Previously described DAGC is placed at the front-end of the WLAN module, integrated on evaluation board for MAXIM2829 chip. In order to evaluate the possibilities for the linearization of the RSSI curve we have made a set of measurements to evaluate the behavior of RSSI and its relation to the optimal gain values. The measurements are performed for six different frequencies in two different bands (2.4GHz and 5GHz band). We have measured the optimal VGA gain for different input power and measured RSSI. The input power range that we have covered is from -20 dBm to -90 dBm. For each measurement we have observed the behavior of RSSI signal for the different LNA and input power level. We have varied the value of the static VGA gain for different input power signal until we get the perfect reception of the data in the baseband receiver. On Fig. 2 and Fig. 3 we can see the values for each band and linearization of the curve that connects the measured RSSI and needed VGA gain signal. On those figures we didn't cover the input ranges where the LNA change has to be done. However, with highest LNA setting it is possible to cover large range of the input power from -90 dBm to – 40 dBm. On Fig.4 is shown dependency between the input power and RSSI for different LNA setting (LNA high, LNA medium, LNA low). It is clear that LNA change introduces more or less linear change of the RSSI value. Therefore, we can use the curves from Fig. 2 and 3 also for different LNA settings. The only issue that we have to take into account is that RSSI value has to be corrected for different LNA values with a constant parameter that can be extracted from measurement from Fig. 4.

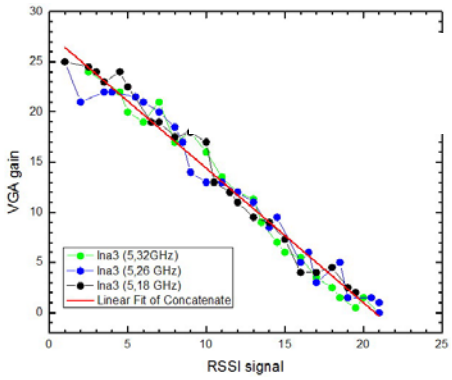

Fig. 2 Dependence between the input RSSI signal and optimal VGA gain for different channels in A band

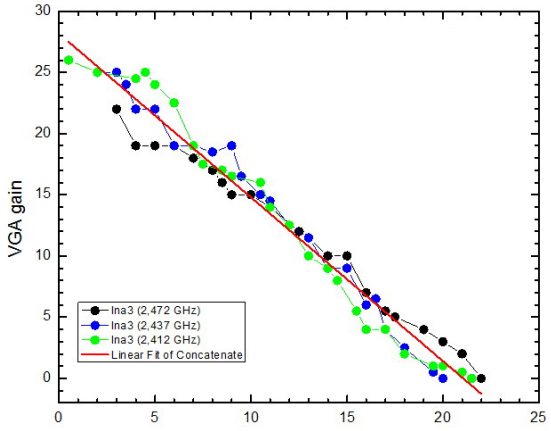

Fig. 3 Dependence between the input RSSI signal and optimal VGA gain for different channels in G band

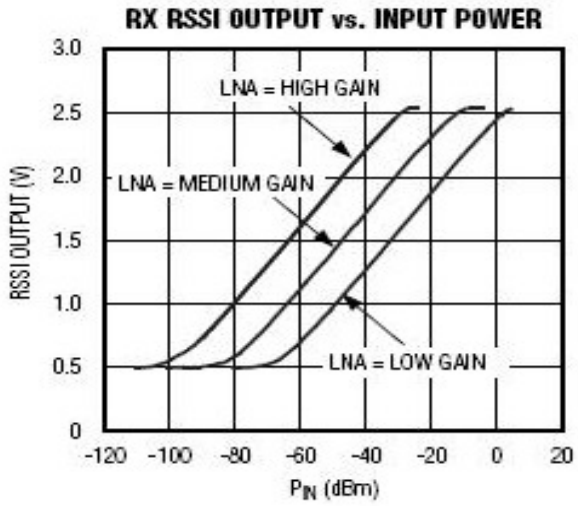

Fig. 4 Results from the measurement of RSSI output for different LNA gain levels provided in datasheet [10]

V. Main Units of DAGC Controller

DAGC is a modular design that consists of several pipelined building blocks. RSSI signal (***R***eceived ***S***ignal ***S***trength ***I***ndication) is generated in analog WLAN front-end and indicates power of incoming signal. This signal is digitized using a 10-bit parallel AD converter. Digital RSSI signal is further used for the power estimation and control of the LNA and VGA gain in digital AGC controller. In the following text we will describe the main blocks of digital AGC controller shown in Fig. 5.

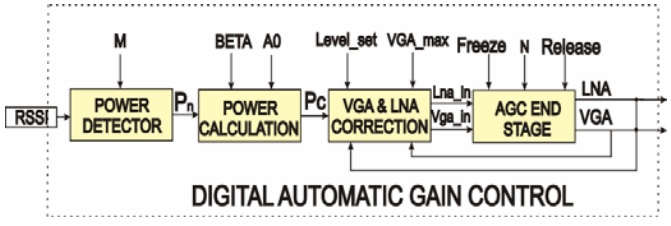

Fig. 5 Block scheme of Digital Automatic Gain Control

First block in the AGC controller chain is a ***Power Detector***. This block is driven by the input value of *RSSI* signal and the control signal *m* (both input signals). Its role is to make the averaging of the RSSI signal. Next block is a ***Power Calculation*** that linearly estimates the power of the signal based on the averaged RSSI. The values of the parameters for this linear interpolation are stored in the control registers and it can be externally programmed. They are normally extracted from the measurements results. Therefore, the value *Pc* is calculated from the input signal *Pn* and the linearization coefficients *Beta* and *A0*. With coefficient settings it is possible to get ideal fitting and to calculate this output signal. Based on the calculated power and on the current LNA we can calculate the next value for VGA and LNA in block ***VGA & LNA Correction***. In order not to overload the digital receiver with over-amplified noise we are defining also saturation level of VGA (*VGA_max)*. This parameter is also generated in the measurement phase and represents the last useful value of gain signal where we can still receive correctly data. Further increase of the gain can only lead to noise increase since the sensitivity of the receiver is already exceeded. Additionally, this block takes into account the programmable input signal *Level_set* that defines the value of the correction of VGA gain for different LNA levels. Final part of DAGC is ***DAGC End Stage***. Here it is decided when the calculated values for VGA's and LNA's has to be applied. To control this block we have used the following input signals: *freeze* (hold the value of gain signals), *release* (release the value of gain signals), and *n* (number of cycles to delay LNA change. The reason for introducing this block is the fact that after the LNA change there is a time needed to stabilize RSSI signal. Therefore, until some number of cycles after the LNA change we have to ignore calculated VGA and LNA gain values. *P*rogrammable signal *n* represents the number of cycles needed to stabilize the RSSI.

A. DAGC Block Description

Main task of the ***Power Detector*** is to produce the average value of the input power from RSSI. To generate this value we have used the following equation:

$$y_{i+1} = (1 - \alpha) \cdot y_i + x_i \cdot \alpha \quad (1)$$

Where (y_{i+1}) is next value of the averaged RSSI, (y_i) is a previous value of the averaged RSSI and (x_i) is a current value of the RSSI. To support DAGC programmability the parameter α can be changed. This parameter directly defines the timing constant of this block. If α is small, we have very good averaging but the response of the circuit is very slow, i.e. it is not possible to track fast changes of the input signal. Otherwise, when α has a greater value the response time to fast changes of the input signal is very good, however the averaging is not so effective. This coefficient α is defined as following:

$$\alpha = \frac{1}{2^m} \quad (2)$$

Signal *m* is input programmable signal. With such programmability of α parameter we are able to cover big range of the averaging factor by using only few bits for *m*.

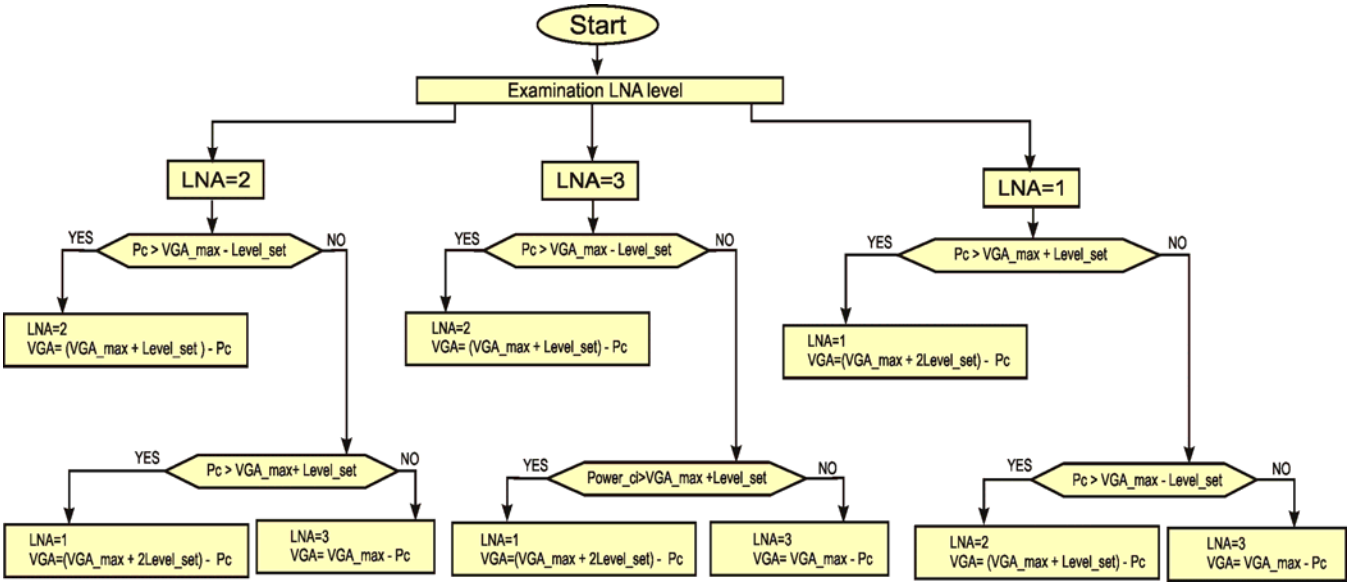

Fig. 6 Decision algorithm for DAGC

B. Power Calculation

After RSSI averaging we want to linearly estimate the power of the received signals. For this purpose we are using linear interpolation. We have defined the following input coefficients for this calculation: *Beta (*interpolation slope*)* and A_0 (interpolation correction). All those parameters are programmable. The initial values for this interpolation are based on the measurements from the evaluation board for Maxim RF chip MAX2829. The results of this approximation are already presented at Fig. 2 and Fig. 3. The equation that describes this interpolation is the following:

$$Pc = Beta \cdot P_n + A_0 \quad (3)$$

Based on the calculated value we are able to generate the gain signals in the following blocks.

C. VGA & LNA Correction

VGA Correction block based on the calculated power of the received signal decides about the needed correction of the gain signals. After the system reset, when the channel is peered, LNA gain is set to the maximum value to be able to sense even very low power signal, whereas VGA gain gets value that is defined as a saturation value of the system. This block has also programmable control signals. As defined in section IV and from Fig. 4 it is obvious that there is a constant power difference between the RSSI curves for different LNA gains. Consequently, in this block we are also performing the correction of the VGA gain signal depending on the LNA gain that is currently set. The power calculator performs always the same linear interpolation without taking into account the current LNA gain. Therefore, we perform here the correction of the results based on the current LNA gain. With this solution we have enabled simplification of the power calculation, reduced number of multipliers in the system, and finally reduced the number of parameters that have to be stored. The signal that defines the correction parameter for this is *Level_set* as shown in Fig. 5.

In this block we are also performing the quantization of the gain signal. The full algorithm of this block is given in Fig. 6.

D. DAGC End Stage

The last block in the chain, ***DAGC End Stage*** delivers the final gain control signals to the analog front-end. The role of this block is to decide when to apply the gain change and when to hold the previous state of the gain signals. In order to perform this function several input signals are used. *Freeze* signal is used to hold the states of gain signals. Gain signals are released with release signal. Normally, *freeze* signal is activated by the baseband received when some frame is detected and synchronization is achieved. From this moment until the end of the frame the gain signals have to fix to the constant value. This constant value is the value that was applied to the RF front-end in the moment when *freeze* signal is generated. When the complete frame is received or reception of the frame in cancelled the *release* signal is activated. From then on, DAGC continues to constantly update the gain values.

In the DAGC end-stage, we are utilizing the coefficient *n* that defines the number of cycles needed to stabilize RSSI signal after LNA change. During this period the gain control signals have to be also frozen.

VI. Synthesis Results

In order to estimate the complexity of design and to evaluate the performances of the system we have performed logical synthesis both for ASIC implementation is using Synopsys and for FPGA implementation using Xilinx ISE software. ASIC synthesis is performed using the library for IHP's internal 0.25 CMOS process. The complexity of the full digital AGC is approximately 2.7 K inverter gates. Provisional power analysis declares power consumption of about

0.56 mW. The complete circuit is targeted to function at 80 MHz.

The same circuit is also implemented using Xilinx ISE software for Virtex2Pro FPGA chips. The results of the synthesis are given in Table I. From this table we can observe the low complexity of implemented solution that is confirmed over the application of the single multiplier. The complete DAGC is tested on the small FPGA evaluation board. Those tests included digital emulation of AGC behavior. In addition to that DAGC is tested sensing real analog signals to the RSSI input.

TABLE I
RESULTS FROM XILINX SYNTHESIS

Number of Slices	186
Number of Slice Flip Flops	48
Number of 4 input LUTs	345
Number of MULT18X18s	1
Total equivalent gate count for design	7.039
Maximum Frequency	105.652MHz

VII. INTEGRATION OF DAGC ON WLAN BOARD

This AGC is implemented and tested on our WLAN development platform. This WLAN platform is based on the application of MAX2829 evaluation board and general purpose FPGA development board, where we have implemented complete baseband processor including DAGC. The complete system is tested using full protocol stack and we are able to use our WLAN system to transfer the lengthy files using the complex modulation schemes. Very high quality of data transfer is achieved for modulation schemes up to 16-QAM (up to 36 Mbps). The most complex 64-QAM is also possible but FER increases.

After finishing the rapid prototyping of the system we have integrated the full WLAN system including complete physical and MAC layer on a single board as shown in Fig. 7. This board is of standard PCMCIA size. Baseband/MAC processors are in this case implemented as dual-chips on the single BGA package. Both processors are fabricated using IHP 0.25 μm CMOS process. The implemented baseband processor contains also DAGC controller. However, currently tested version of the ASIC baseband processor contains an earlier and simpler version of DAGC. New version of this ASIC that includes also the more advanced DAGC, presented in this paper, is currently under fabrication. This board is tested and functions correctly and date a transfer with this integrated board is also possible. However, the better performances are expected with the next generation of the baseband chip that includes the new DAGC.

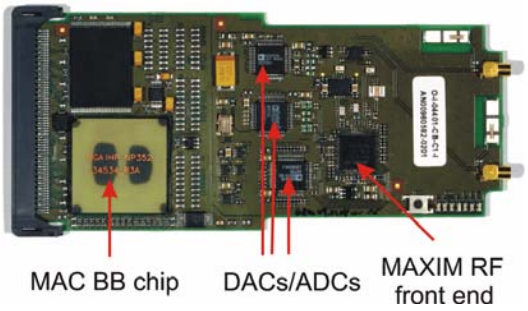

Fig. 7 Integrated DAGC on WLAN

VIII. CONCLUSION

In this paper we have presented our DAGC based on the linear power interpolation. The applied solution is simple and allows fast convergence of the gain signals. This DAGC solution doesn't require the lookup tables and memories, due to the very low complexity. For power estimation we use 10-bit RSSI signal and avoid using of I/Q data signals. This design shows good behavior under different frequency channels and bands.

The complete circuit is implemented in tested together with the full WLAN system on designed in IHP. Those tests are performed using our FPGA development platform. For this AGC we have observed very fast AGC settling time (approx. in average 1μs) with the correct functional behavior. The ASIC that includes this DAGC is currently under fabrication and we expect to test the integrated system soon.

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