World Academy of Science, Engineering and Technology
International Journal of Electronics and Communication Engineering
Vol:2, No:3, 2008

# Design and Layout of a X-Band MMIC Power Amplifier in a Phemt Technology

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Open Science Index, Electronics and Communication Engineering Vol:2, No:3, 2008 publications.waset.org/14853/pdf

***Abstract*—**The design of Class A and Class AB 2-stage X band Power Amplifier is described in this report. This power amplifier is part of a transceiver used in radar for monitoring iron characteristics in a blast furnace. The circuit was designed using foundry WIN Semiconductors. The specification requires 15dB gain in the linear region, VSWR nearly 1 at input as well as at the output, an output power of 10 dBm and good stable performance in the band 10.9-12.2 GHz. The design was implemented by using inter-stage configuration, the Class A amplifier was chosen for driver stage i.e. the first amplifier focusing on the gain and the output amplifier conducted at Class AB with more emphasis on output power.

***Keywords*—**Power amplifier, Class AB, Class A, MMIC, 2-stage, X band.

## I. Introduction

THE power amplifier designed in this project is part of the duplex transceiver shown in Fig. 1, which is used in radar for monitoring iron characteristics in a blast furnace. Overall design specifications for PA are listed in Table I.

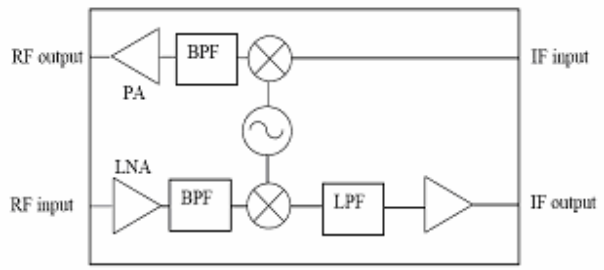



Fig. 1 Transceiver Diagram

TABLE I
Summary of Design Specifications

| | |
|---|---|
| Output Frequency | 10.9 – 12.2 GHz |
| Output Power | 10dBm |
| Gain | 15dB |
| Linearity | As good as possible |
| Power consumption | As small as possible |
| Size | As small as possible |

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The design approach is one of the major issues in modeling any power amplifier mostly when more than one amplifier is part of the design. There are three different kinds of topologies push-pull amplifier, balanced amplifier and interstage amplifier. In our case as output power was not very high and most important concern was to have output as linear as possible and chip size as small as possible, push-pull power amplifier designs was not taken into consideration as they are known for high output power and high efficiency. Similarly balanced power amplifiers are good choice for having low VSWR at input as well as output i.e. good matching still this configuration was not used as it will only increase both the chip size and the complexity of the circuit by adding some quadrature hybrids for having balanced signals which is at time hard to achieve, and also good matching was possible without them. So we implemented the power amplifier in inter-stage topology to achieve good linearity and also small size.

## II. Design Philosophy

The design of each sub-circuit components of the PA was first done using ideal lumped elements. Those ideal elements were replaced using the corresponding models from WIN design kit. Resistors and capacitors were easy to synthesize, but inductors had to be carefully modeled using an iterative tuning process. Connection of these WIN foundry components were accomplished using tee, taper, bend and microstrip transmission line also available in WIN design kit.

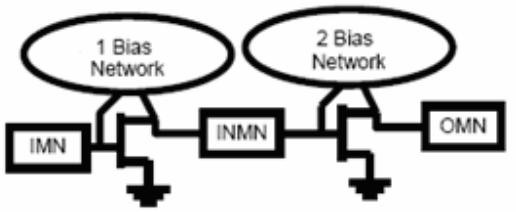



Fig. 2 Two-stage Power Amplifier Topology

As shown in Fig. 2, the power amplifier topology we used is a 2-stage cascaded design with a driver class A amplifier stage and a output class AB amplifier stage both using a 4x75um pHEMT. The 2-stage design was used since a single stage was unable to meet the gain and power specification at the design frequency.

Finally, we achieved performance for the two stage power amplifier for good linearity, 20% drain efficiency and output

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power up to 13.5dBm with about 18.5dB power gain over the bandwidth at -5dBm input power from up-converter mixer.

*A. Class A PA Design*

Class A amplifiers amplify signal over the whole of the input cycle such that the output signal is an exact scaled-up replica of the input without clipping. Class A amplifiers are the usual means of implementing small-signal amplifiers. They are not very efficient—a theoretical maximum of 50% is obtainable, but for small signals, this waste of power is still extremely small, and can be easily tolerated. Class A amplifiers are also important when the output power is required to be in linear region. Linearity was also an important part of our design. For this purpose as mentioned earlier, pHEMT transistor was used from the provided WIN kit. The gate width of 4x75um was found suitable. Class A amplifier was chosen to be first stage amplifier because a high gain was achievable within the linear region, this thing was in trade off with efficiency.

1. Operating Point

The Fig. 3 shows the Transconductance Characteristics curve for the pHEMT transistor for $V_{ds}$ 2V the pointers indicates the range for which class A amplifier can be biased. Similarly Fig. 4 shows the IV curve when $V_{ds}$ is swept from 0V to 5V, but in the final stage of design the Class A amplifier was biased at $V_{ds}$ = 2V ad $V_{gs}$ = -0.5V.

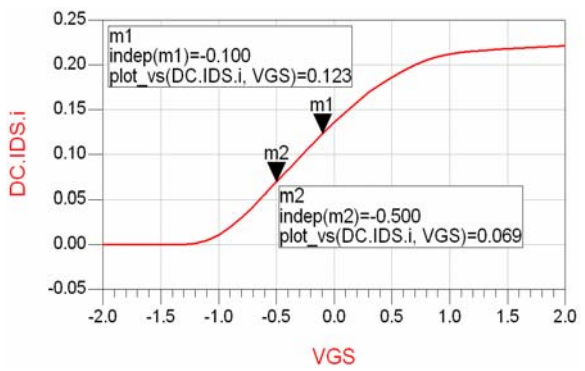



Fig. 3 Transconductance Characteristics

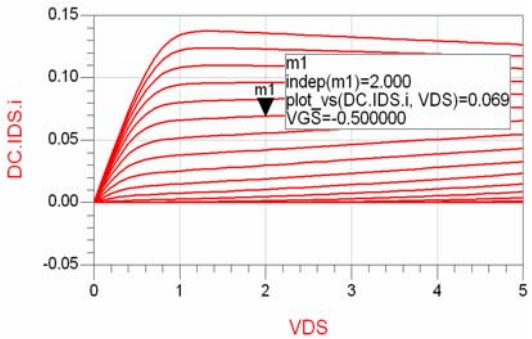



Fig. 4 IV Curve

2. Matching Network

In the following chapters, the design procedure and schematic simulation results, layout and RF momentum simulation results are presented.

The matching network was design to work over a large bandwidth. For the first amplifier the matching was done only at the input and the output matching network was the designed as interstage in the cascaded network.

3. Biasing Network

The biasing network includes high inductance RF choke a with DC block in parallel leading to the ground. After tuning and optimizing the circuit this DC feed and block at the gate bias became the part the input matching network.

4. Feedback Loop Circuitry

The transistor pHEMT was provided with feedback with a resistor and a capacitor. The capacitor is used to block the DC through the feedback it reduced the Power Added Efficiency but less power is wasted by thermal dissipation. The main purpose include this feedback network is to stabilize the output.

5. Results

The result is shown in below figures. The output power obtained was above the required and well within the linear region so the driver stage gave a high gain which made the task easier for class AB amplifier to produce required output power within the linear region with less clipping in the output voltage.

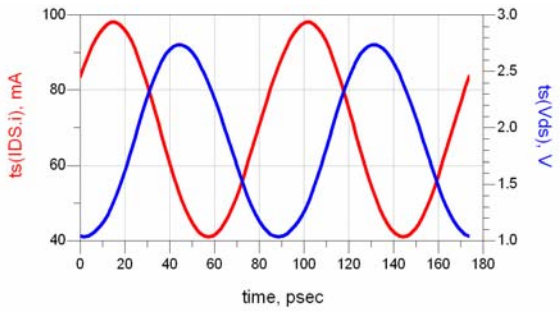



Fig. 5 $I_{ds}$ and $V_{ds}$ waveform

Fig. 5 shows the drain current $I_{ds}$ and drain voltage $V_{ds}$ before DC block at the output which good sinusoid so this predicts the circuit works as a Class A amplifier.

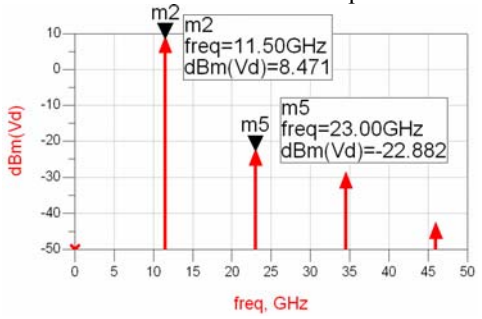



Fig. 6 Harmonics Spectrum

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The output power ($V_d$ is voltage after DC Block) is shown in the Fig. 6 for fundamental harmonics and as we can see second harmonics are well suppressed to -30dB compared to the fundamental. This output power is in the linear region as evident from the Fig. 7.

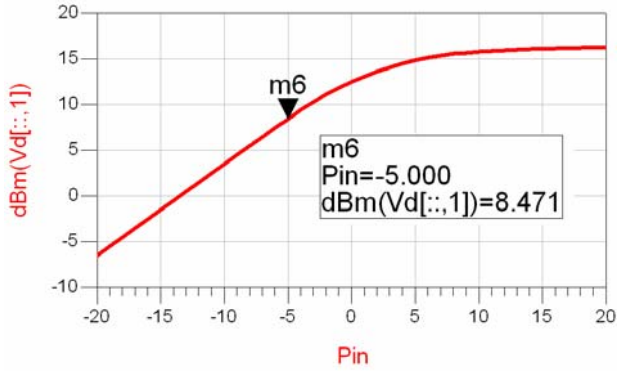



Fig. 7 Output Power vs Input Power

*B. Class AB PA Design*

A 4x75um pHEMT was chosen for the second amplifier stage to efficiently boost the power of the pre-amp stage.

1. Operating Point

The operating bias point for Class AB is shown in Fig. 8 and Fig. 9. $V_{gs}$ =-1V, $V_{ds}$=3V. It is noteworthy that the bias point for the pHEMT was chosen to balance gain, power and efficiency. Another subtle goal was to allow for bias tuning.

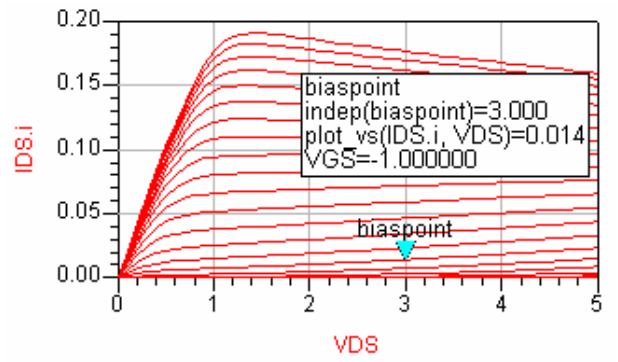



Fig. 8 Drain Current versus voltage for various gate bias

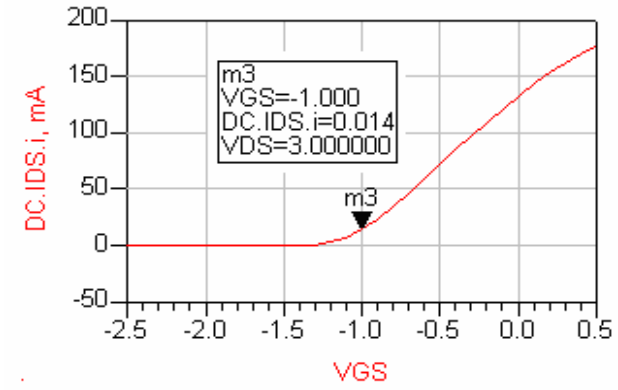



Fig. 9 Transconductance Characteristics

2. Bias Network

The bias networks for gate and drain node is both combined with a RF choke inductor to block RF signal into bias network and a bypass capacitor to ground the RF signal without interfering DC supply.

3. Band-Pass Output Matching Network

Since the input power from previous stage amplifier is 3dBm. The output power goal of 10dBm is easily reached. So we don't need Cripps load pull method to maximize the output power. Thus, we just need a band-pass filter between the output of pHEMT and 50Ohms load to decrease the harmonics to get the waveform more sinusoidal at load. We used  in ADS to define band-pass filter features to simulate ideally. Then, we used  in ADS to define band-pass lumped elements impedance matching smartcomponent features so as to design the lumped elements band-pass output matching network automatically.

Finally, after inserting the output matching lumped components circuit back into the Class AB stage amplifier and then making some tuning, we found we could use the RF choke inductor also as a part of band-pass output matching network to give satisfactory simulation results and then meanwhile save the lumped components in our circuit hence reducing the size. The Fig. 10 shows the good resulting S parameters. Furthermore, the capacitor in our band-pass output matching network also provided DC blocking.

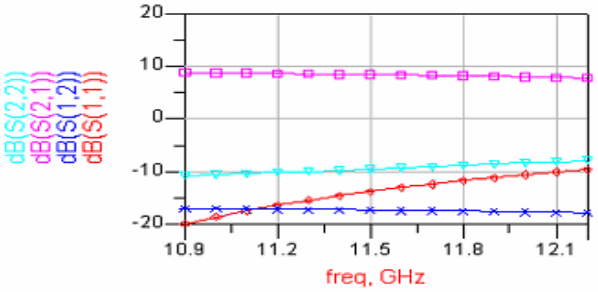



Fig. 10 S Parameters

4. Feedback

Besides, the inspired idea is that we used feedback for pHEMT. The feedback combines a resistor and a capacitor. The simulated results showed that resistor gave good stability and capacitor gave good DC blocking so as to increase efficiency.

5. Simulated Results

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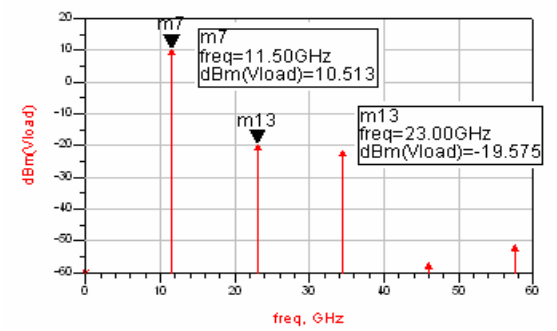



Fig. 11 Output Power

Fig. 11 shows the output power. At the fundamental frequency the power is 10.5dBm, and suppression of second harmonic is 30dB. Thus, in Fig. 12, we got the blue sinusoidal output current waveform at load after the bandpass filter.

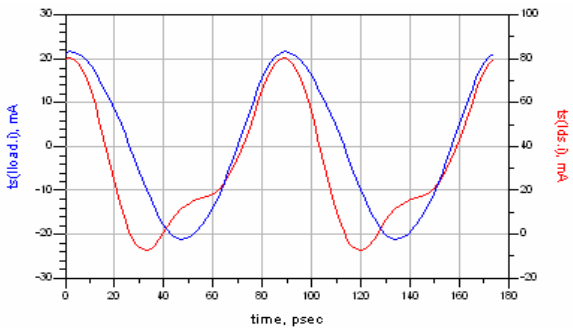



Fig. 12 Output current in time domain before & after filtering

We also got the power gain from 7.8 to 8.8dB within the bandwidth.

*C. Cascaded Power Amplifier Circuit*

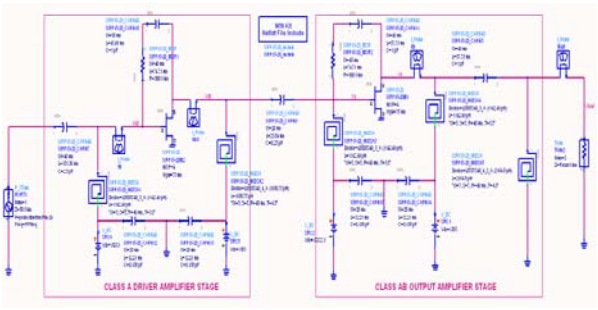



Fig. 13 Two stage power amplifier schematic

After the separate design for Class A and Class AB amplifier was completed, the following job was just to combine them together with the inter-stage connection. We conjugately match Class A stage with Class AB stage. We measured the output impedance of Class A stage and input impedance of Class AB stage in ADS and then used lumped-element match smartcomponent to design the inter-stage matching network automatically. Now, it is turn to put both class A and class AB stage together with the inter-stage matching connection in all real components from WIN design kit and then simulate. After tuning the inter-stage matching network, we got good simulated results with the inter-stage matching network consisting of a capacitor and two RF choke inductors each from bias network in pre- and post- stage. It really helps us to save the lumped components and minimize the circuit size. The capacitor in inter-stage connection also provided DC block for both pre- and post- stage. When we simulated the pre-layout schematics, we got good results, which you can see in the Table II. Then we put the schematic with the interconnection microstrip line, tee, taper and bend, after tuning the circuits, we got the better simulation results of the post-layout, which can be seen in Table I compared with pre-layout.

TABLE I
SUMMARY OF PA PERFORMANCE AT DIFFERENT DESIGN STAGES

| | Pre-Layout | Post-Layout |
|---|---|---|
| Frequency | YES | YES |
| Bandwidth | YES | YES |
| Gain | 17.3 ~ 18.1 dB | 18.6 ~ 19.1 dB |
| Output Power (-5dBm input power) | 12.63 dBm | 13.83 dBm |
| Gain Ripple | -0.3 ~ 0.3 dB | -0.2 ~ 0.2 dB |
| Efficiency | 16.86 % | 19.05 % |
| PAE | 6.95 % | 8.92 % |
| Input VSWR | 1.3 ~ 1.5 | 1.1 ~ 1.3 |
| Output VSWR | 1.26 ~ 1.45 | 1.22 ~ 1.28 |
| 2nd Harmonics Suppression | 14.78 dB | 14.485 dB |

## III. SIMULATION RESULTS

When the two amplifier stages are connected with the microstrip transmission lines, bends, tapers, tees and via holes, the entire power amplifier can be simulated for small-signal and large-signal performance. Table II shows a summary of the performance of the amplifier at the two major stages of the design process.

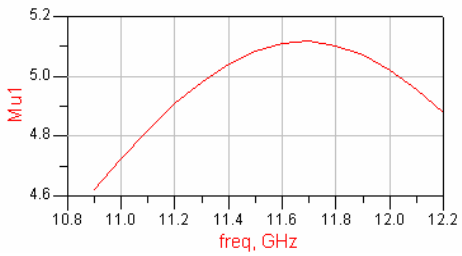



Fig. 14 Stability factor

Fig. 14 shows the power amplifier is unconditionally stable over the bandwidth. Fig. 15 shows the Large-signal performance of the PA. Note that Output Power and linear is displayed on the left y-axis and Efficiency is displayed on the right y-axis.

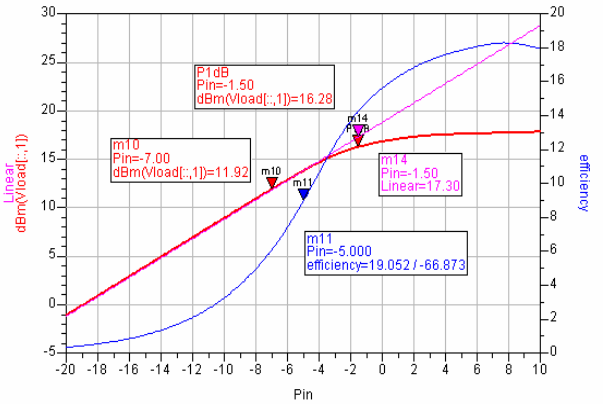



Fig. 15 Large-Signal Nonlinear Performance of PA

The simulated performance of the amplifier was very encouraging. Fig. 16 shows the S parameters for the small-signal performance.

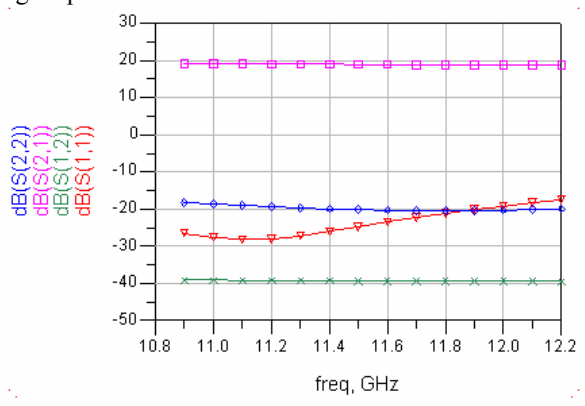



Fig. 16 S parameters

We finally got 13.8dBm load output power and second harmonics -14.5dB suppression as Fig. 17 shown.

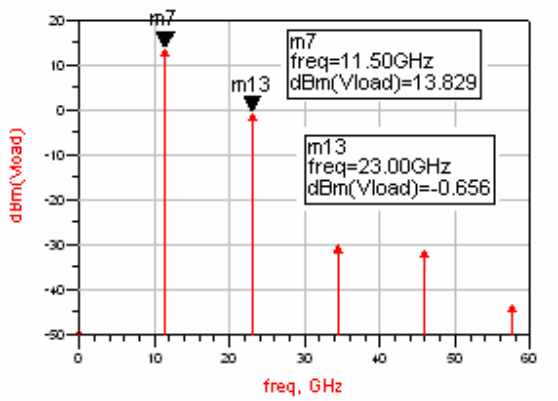



Fig. 17 Harmonics Spectrum

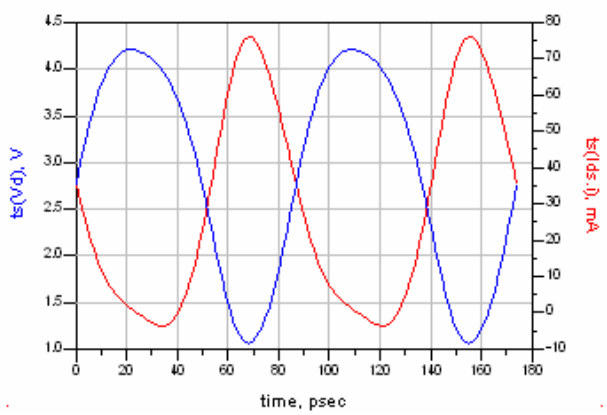



Fig. 18 Output waveform before bandpass filter

Compared to waveform before bandpass filter in Fig. 18, we got more sinusoidal waveform after bandpass filter at load in Fig. 19.

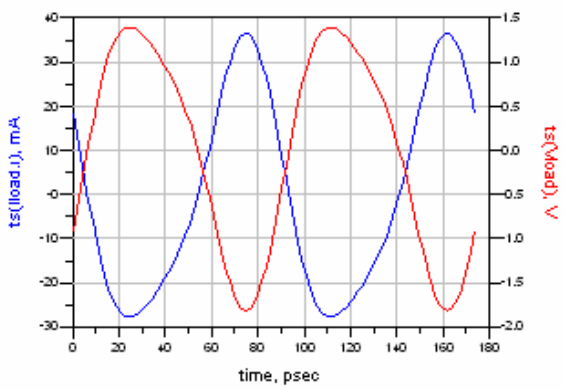



Fig. 19 output waveform after bandpass filter

Besides, more to mention, we had linear phase response and got the power efficiency around 19% and power added efficiency around 9%.

## IV. Final Schematic, Layout and RF Momentum

We use 0.75 μm pHEMT process which is based on a 0.75μm gate GaAs Pseudomorphic High Electron Mobility Transistor. The main features of the layout are

- 0.75 um T-gates
- Two global gold interconnect metal layers
- Air-bridges MIM Capacitors
- Air-bridges Square Inductors
- TaN Thin Film Resistors
- Slot substrates via hole

The layout is shown in Fig. 20. The chip size of the power amplifier is 1994um*823um.

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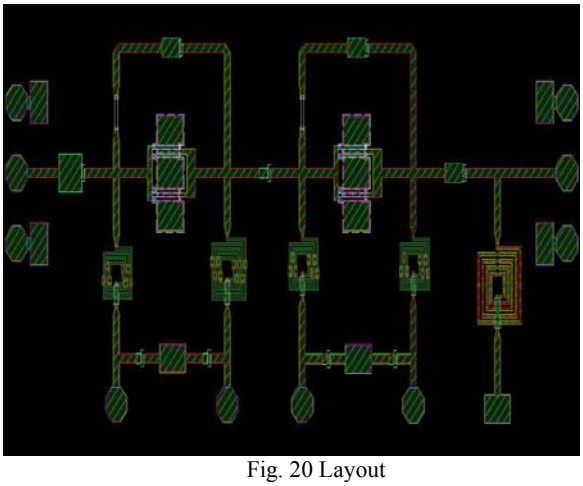


Fig. 20 Layout

The RF momentum simulation was recommended to implement on the feedback. See in Fig. 21

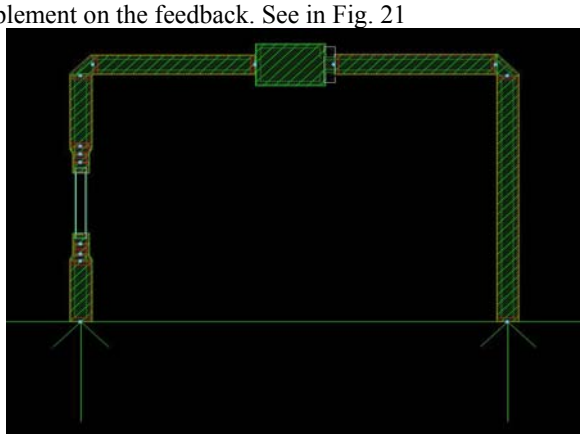


Fig. 21 Layout of Feedback

The visual current spectrum result of RF momentum simulation was shown in Fig. 22. After we replaced the feedback with momentum simulated file, the difference is very small. We can draw conclusion from the RF momentum simulation that the feedback loop seems a little bit longer than necessary; this may lead to some distributed effects.

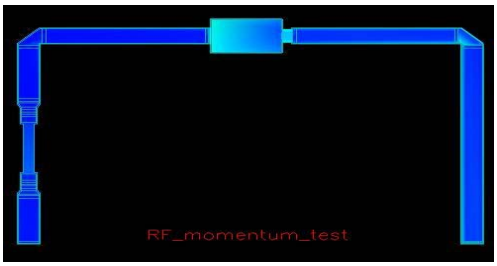



Fig. 22 Momentum Simulation

## V. Test Plan

In order to measure the power amplifier after WIN foundry fabrication it is necessary to place DC and RF pads on all sides of the chip. DC needle probes will be used to provide individual bias to the gate and drain of each transistor RF probes will come in from the top and left side of the chip for input and output, respectively.

## VI. Conclusion

The design of two-stage power amplifier for the X-band transceiver was successfully done. All the goals were met with the exception of the overall efficiency a little bit lower. Output signal is quite linear. Chip size is small but can be reduced further. Increasing the NOF or gate width can increase the linearity of output power. The momentum simulation of Inductor is not done.

## Acknowledgement

The author wishes to acknowledge the assistance and support of our supervisor Dan Kuylenstierna, and also the examiner Prof. Herbert Zirath who arranged this project.

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