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A Direct Down-conversion Receiver for Low-power Wireless Sensor Networks.

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Abstract—A direct downconversion receiver implemented in 0.13 μm 1P8M process is presented. The circuit is formed by a single-end LNA, an active balun for conversion into balanced mode, a quadrature double-balanced passive switch mixer and a quadrature voltage-controlled oscillator. The receiver operates in the 2.4 GHz ISM band and complies with IEEE 802.15.4 (ZigBee) specifications. The circuit exhibits a very low noise figure of only 2.27 dB and dissipates only 14.6 mW with a 1.2 V supply voltage and is hence suitable for low-power applications.

Keywords—LNA, Active Balun, Passive Mixer, VCO, IEEE 802.15.4(ZigBee).

I. Introduction

THE increasing demand for low-power wireless transceivers operating in the 2.4 GHz ISM band, has prompted an extensive research in this area. In such scenario CMOS technology is very appealing for low-cost, low-power solutions targeted to low-rate wireless personal area networks (WPANs) such as ZigBee. Among all the reported receiver architectures, a direct conversion architecture, is particularly appealing for monolithic implementation due to its simplicity [1]. Regardless its simplicity, a direct conversion receiver requires a careful design to counterbalance the effects of DC offsets and flicker noise at low frequencies [2]. In a direct conversion receiver, the incoming signal is shifted to baseband with no intermediate conversion steps like in heterodyne receivers; furthermore, IEEE 802.14.5 standard relies on complex modulation schemes in which data is modulated by a pair of orthogonal signals. This modulation scheme complicates the transceiver since quadrature mixer and VCO are necessary to demodulate both the in-phase and the quadrature component of the incoming signal. Fig. 1 sketches a simplified block diagram of a typical direct conversion receiver. The input passband filter reduces or eliminates the effect of the out-of-band interferers. The signal is then amplified by a low noise amplifier (LNA) that must comply with the linearity and sensitivity requirements of the target standard. In the case of ZigBee-compliant devices the required linearity, determined by the input-referred 1-dB compression point is -20 dBm [3]. ZigBee compliant devices require an input sensitivity of at least -85 dBm [11], which allows relaxing the noise figure requirements of the receiver building blocks. The relaxed standard requirements for both gain and sensitivity, makes a single-end LNA implementation preferable to a differential architecture. This, in turn, also helps reducing power consumption and the number of passives, and hence die area and costs. However, a differential signaling improves noise immunity and common mode rejection; in addition, a balanced mixer is preferable to a single-end implementation due to its superior linearity. For this reason a single-end (unbalanced) to differential (balanced) mode must be performed after the LNA by a balun. For a low-cost, low-performance application an active balun is preferable to reduce the number of passive elements. In order to reduce area occupation and power consumption, downconversion is implemented by a quadrature balanced passive switch mixer. A quadrature mixer needs both in-phase and quadrature signals in order to perform demodulation and de-embed the received signal from the carrier. There are several reported methods to perform quadrature signal generation [4]. The use of a quadrature voltage-controlled oscillator (QVCO) could be very appealing provided the number of passive elements is limited. Since ZigBee is a low-performance standard it is not necessary a particular care in the balun and QVCO design since the phase offset introduced will be corrected digitally by the modem back-end using the incoming packet preamble to perform the required phase adjustment using Kay [5] and CORDIC algorithms [6].

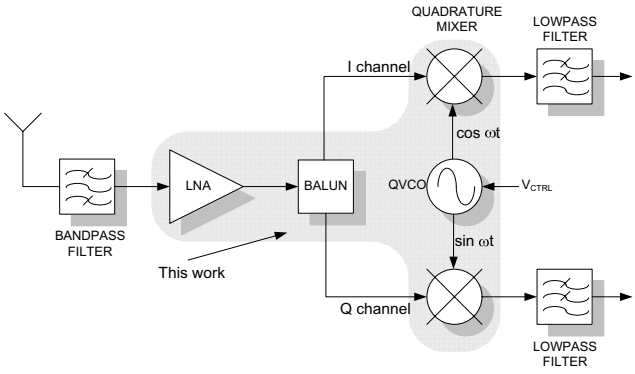

Fig. 1. Direct Downconversion Front-End.

The design of low data rate wireless sensor networks may be as challenging as high performance design. Although wireless standards targeted to low-rate WPANs such as ZigBee do not have severe restrictions for noise, sensitivity and jamming resistance, the design restriction on power consumption and die area may impact design choices and performance since the target product is a battery-operated low cost and lightweight device. All of these issues are targeted and analysed in

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this paper. The result is a design that combines excellent performances with an extremely low power consumption and area occupation, since the number of integrated passive devices is minimised. The rest of the paper is structured as follows. Section II describes in depth the front-end architecture and its basic building blocks (low-noise amplifier, balun, quadrature mixer and voltage-controlled oscillator). In a direct conversion receiver flicker noise is a major concern since it is inversely proportional to signal frequency. In Section III the proposed design is evaluated, discussed and compared with other implementations. Finally, in Section IV the conclusions are given.

II. Direct Downconversion Receiver

CMOS integrated circuits for RF applications are being intensely studied due to their potential for low cost, high scalability and integration that make them suitable for Systems on Chip (SoC) implementation [7]. The improvements experienced by RF-CMOS technology in the last years has disclosed several possible applications for wireless systems. Due to their flexibility and broad range of potential applications, wireless sensor networks operating in the unlicensed ISM band are the object of intensive research [8], [9], [10] and have been lately standardized by the IEEE [11]. The mobile nature and the low cost of such infrastructure-less networks makes power consumption and integrability of paramount importance. Among all the reported front-end architectures [12], direct conversion (homodyne) transceivers are very appealing for monolithic CMOS implementation due to the reduced number of components needed to perform down and upconversion operation. In addition, converting the RF signal directly into baseband eliminates the problem of image frequency and the need for image-rejection filters that increase design effort and complexity. Nonetheless, the major shortcoming of a direct conversion to baseband are the DC offsets that may saturate the amplifying stage. However, in spite of this limitation, direct direction transceivers are becoming very common in practical CMOS implementations [8], [9], [10]. In the sequel, the basic blocks of the proposed receiver are described. The receiver is implemented using a 130 nm UMC RF-CMOS process and a 1.2 V supply voltage.

A. LNA

Among all the reported LNA architectures, a single-end implementation is very appealing for low-power, low-cost designs due to the reduced number of passive elements, low noise figure and small bias current. A cascoded implementation with inductive source degeneration offers a good compromise between gain and linearity as well, making easier to meet ZigBee specifications. Fig. 2 depicts the proposed LNA. Transistor M1 and M2 form the cascode stage, both transistors are minimum length and have the same channel width $W = 90$ μm. Transistor M3 and resistors R_{b1} and R_{b2} are used to bias the gate of M1 with a DC voltage of about 0.4 V, so that the bias conditions are approximately the same for both M1 and M2.

Transistor M3 is minimum length and 30 μm wide, resistor R_{b1} is 10 KΩ, whereas resistor R_{b2} is 2.24 KΩ. Bias voltages

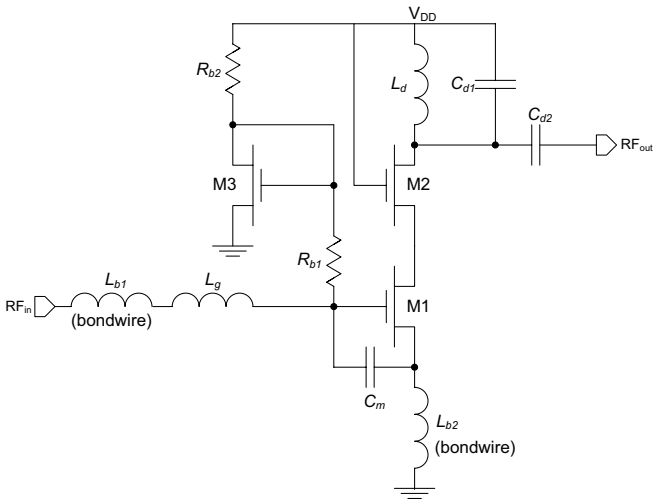


Fig. 2. The Cascode Low Noise Amplifier.

have been chosen to guarantee that both M1 and M2 operate in medium inversion and with a transconductance g_m of 27.5 mS, sufficiently high to keep transition frequency ω_T high in order not to increase excessively the noise figure NF. The bias current is 2.09 mA, which leads to 2.5 mW power consumption.

Bondwires inductance is exploited to reduce on-chip inductor size and improve circuit performance. Input matching network is implemented by the the inductor $L_1 = L_{b1}+L_g$, by source degeneration inductor $L_2 = L_{b2}$, and by the equivalent capacitor $C = C_m + C_{gs1}$ formed by the matching capacitor C_m and the gate-to-source capacitance C_{gs1} of transistor M1. The amplifier input impedance $Z_i(\omega)$ is [1]:

$$Z_i(\omega) = g_{m1}\frac{L_2}{C} + j\left[\omega(L_1 + L_2) - \frac{1}{\omega C}\right]. \qquad (1)$$

At the resonant frequency $\omega_0 = \frac{1}{\sqrt{(L_1+L_2)C}}$ the imaginary part of $Z_i(\omega)$ is canceled and the real part is matched to the source impedance $R_S = 50$ Ω by carefully sizing transistor M1 transconductance g_{m1} and the passives L_2 and C. Equation (1) is used as a starting point to size the input matching network. Output matching is performed by inductor L_d and the capacitive divider formed by the capacitors C_{d1} and C_{d2}. Capacitor C_{d1} also resonates with inductor L_d improving both gain and narrow-band behaviour. Output matching network is designed to match the 85 Ω input impedance of the active balun that follows the amplifier. Inductor L_d is 9.1 nH, whereas L_g is 4.1 nH. Bondwire inductances are 1 nH, whereas capacitances C_m, C_{d1}, and C_{d2} are 274, 208 and 169 fF, respectively. Observe that the input matching network has been designed so that the source degeneration inductor is implemented by exploiting exclusively the bondwire inductance. This in turn helps to improve the amplifier gain while still ensuring a good linearity, and to drastically reduce die area since only two integrated inductors are necessary. The designed low noise amplifier is unconditionally stable and its performances are reported in Fig. 3. The proposed LNA has a 15 dB gain and a reverse isolation of 35.5 dB, good input

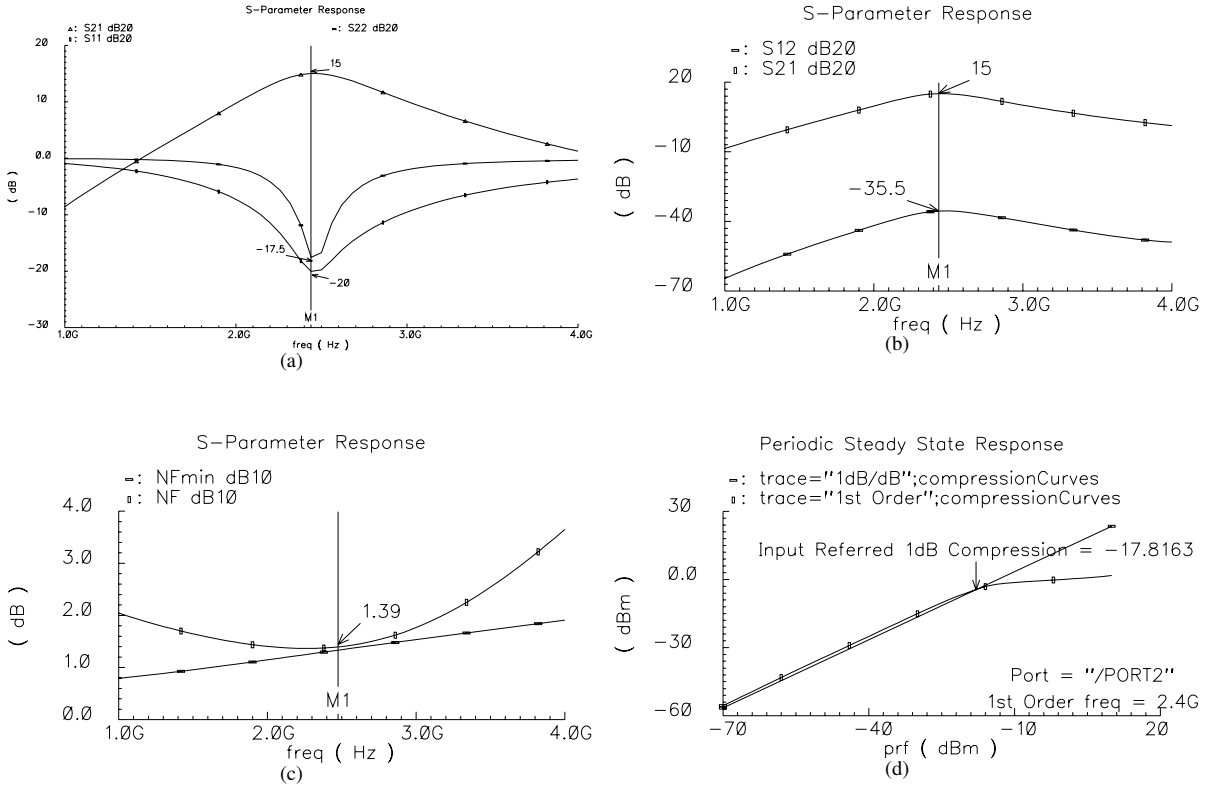


Fig. 3. Simulated Performances of the Low Noise Amplifier: (a) Gain (s_{21}), Input (s_{11}) and Output (s_{22}) Matching, (b) Reverse Isolation (s_{12}), (c) Noise Figure, and (d) Input Referred 1-dB Compression Point.

and output matching a noise figure of 1.39 dB and an input-referred 1-dB compression point of -17.81 dBm that makes it suitable for ZigBee applications.

B. Balun

There are several ways to implement an active balun [13]. A very straightforward method consists in using a CG-CS (common gate-common source) stage. Although, this is not the best way, its simplicity makes it very appealing for low-cost implementations such as ZigBee. Fig. 4 depicts the active CG-CS balun. Both transistors M1 and M2 are minimum length and 16 and 15 μm wide respectively; bias resistance R_s is 309.8 Ω and it is used to set the bias point of both the CG and CS stage so that the gain is approximately the same for both the amplifying stages. Load resistances R_{d1} and R_{d2} are both 222.4 Ω. Finally, the blocking capacitors C_B are 298 fF. An input-referred 1-dB compression point of at least -5 dBm is necessary to meet with ZigBee specification. Such linearity requirement must be met without increasing excessively power consumption and hence increasing circuit losses. The active balun has a -4.8 dBm input-referred 1-dB compression point, dissipates 3.5 mW with a bias current of 2.9 mA and a 1.2 V supply voltage and has a worst-case power loss of 2.8 dB, that is a better behaviour than a passive balun that has a minimal theoretical loss of 3 dB. The output buffers formed by transistors M3 and M4 and and resistances R_{o1} and R_{o2} are used for output matching and to drive the mixer input impedance. Both M1 and M2 are minimum length and

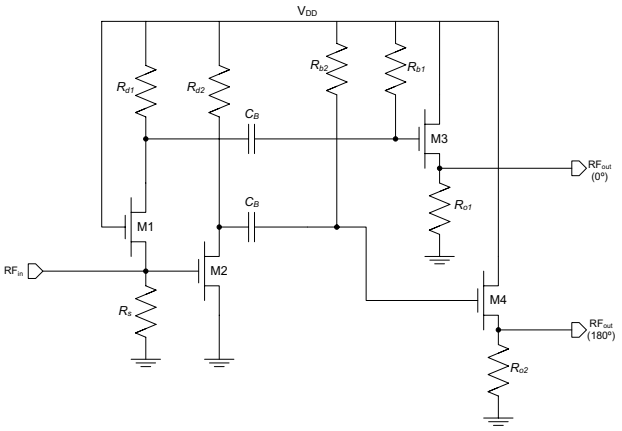


Fig. 4. The CG-CS Active Balun and the Output Buffers.

20 μm wide, whereas $R_{o1} = R_{o2} = 176$ Ω. Fig. 5 summarises balun performances. The gain and phase matching between the output signals is excellent as shown in Fig. 5 (a) and (b). The simulated gain difference is about 0.2 dB, whereas the phase difference is approximately 179.1 degrees in the band of interest, leading to a phase mismatch of 0.9 degrees.

C. Passive Switch Mixer

A mixer translates the incoming RF signal to low intermediate or zero frequency. Passive mixers are very attractive due to their very low power consumption and high linearity [14].

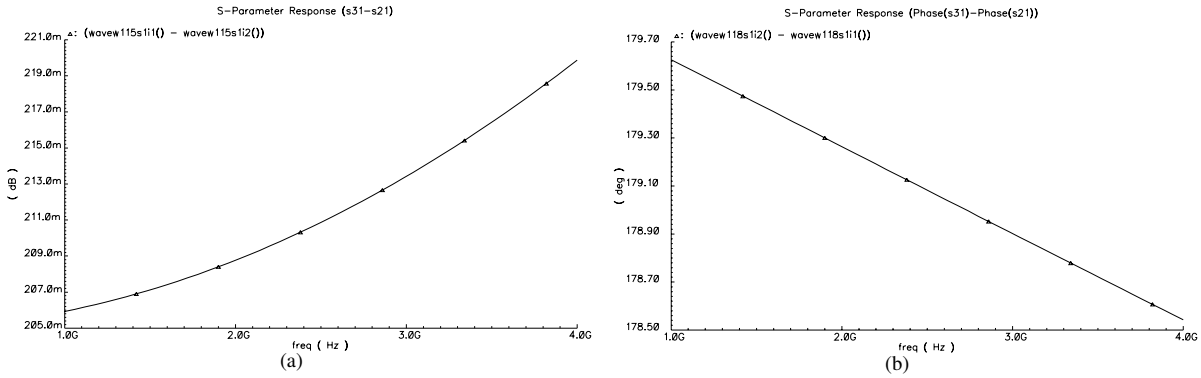


Fig. 5. Simulated Performances of the Active CG-CS Balun: (a) Gain Mismatch, and (b) Phase Mismatch.

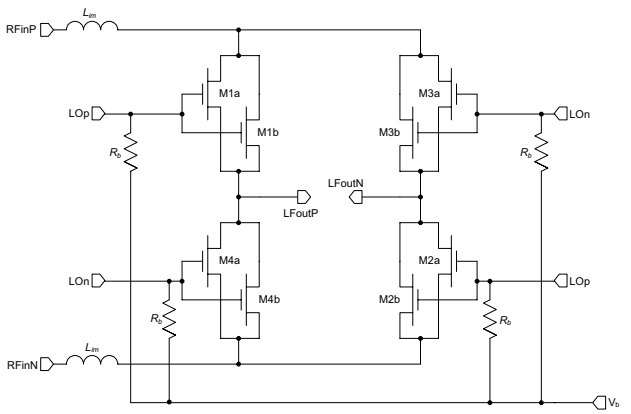


Fig. 6. The Passive Switch Mixer.

Fig. 6 depicts the proposed passive switch mixer. It consists of a input matching network formed by inductors L_{im}, a bias network formed by resistors R_b, and the switching core formed by transistors M1 to M4. Since both input and output impedances of the NMOS switch are capacitive, the series inductors L_{im} performs the cancellation of the imaginary part, thus improving input matching. The balanced RF signal is applied through inputs $RFinP$ and $RFinN$ to the sources of the NMOS switches, whereas the local oscillator (LO) signals are applied to the gates of the switching devices. All the transistors are minimum length and 90 μm wide, matching inductors are $L_{im} = 2.3$ nH, bias resistors are $R_b = 10$ KΩ, whereas bias voltage is $V_b = 0.3$ V. In a NMOS convectional switch, the transistor conducts when its gate-to-source voltage exceeds the threshold voltage V_T, thus the output signal could be decreased by V_T in the case of large RF inputs. The V_T drop problem leads to output signal compression and non-linearities when the RF input is large compared to the LO signal. In the proposed design, switching transistors gates are biased closed to threshold voltage to tackle the V_T drop problem and to improve mixer linearity. Fig. 7 summarises balun performances.

Voltage conversion gain is simulated for different values of the local oscillator (LO) power and assuming the mixer output is matched to the input of an high-impedance filter.

TABLE I
MIXER PORT TO PORT ISOLATION.

Port	Feedthrough Contribution
LO-RF	-72.40 dB
LO-IF	-77.80 dB
RF-LO	-113.84 dB
RF-IF	-72.40 dB

TABLE II
COMPARISON SUMMARY WITH PREVIOUSLY REPORTED IMPLEMENTATIONS.

Figure of Merit	This Work	[14]	[15]
LO Frequency	2.4 GHz	1.4 GHz	2.3 GHz
LO Voltage	420 mV	300 mV	280 mV
LO Power	$+2.5$ dBm	-0.4 dBm	-1 dBm
Noise Figure (SSB)	5.8 dB	10 dB	N/A
Conversion Gain	-0.96 dB	-3.6 dB	-2.9 dB
Input-Referred P1dB	-3.89 dB	-5 dBm	-1 dBm
LO-RF Isolation	72.40 dB	N/A	38 dB
Current Consumption	0 mA	N/A	< 0.1 mA
Die Area	0.19 mm^2	0.35 mm^2	0.21 mm^2
Technology	0.13 μm	0.35 μm	0.25 μm

Observe that that with a power of $+2.5$ dBm the mixer exhibits a voltage conversion gain of -0.966 dB, that drops down to -1.22 dB when the input oscillator power is -1 dBm. The noise figure is measured at 1 KHz to take into account the effect of flicker noise, since it is proportional to $\frac{1}{f}$. With an input oscillator power of -1 dB the simulated noise figure is about 6.8 dB. Mixer linearity is measured by the input-referred 1-dB compression point. The proposed mixer has a simulated 1-dB compression point of -3.89 dBm.

Table I summarizes the simulated port-to-port isolation. LO feedthrough to mixer input (RF) and output (IF) ports is considered as well as the feedthrough from input port to LO and IF ports. The LO-RF isolation is of paramount importance since reciprocal mixing at the RF port may produce a large DC-offset.

Table II compares the proposed implementation with other similar works. The proposed switch mixer has the best noise figure, conversion gain, port isolation and area overhead. The linearity is also excellent; however, the price to pay for these

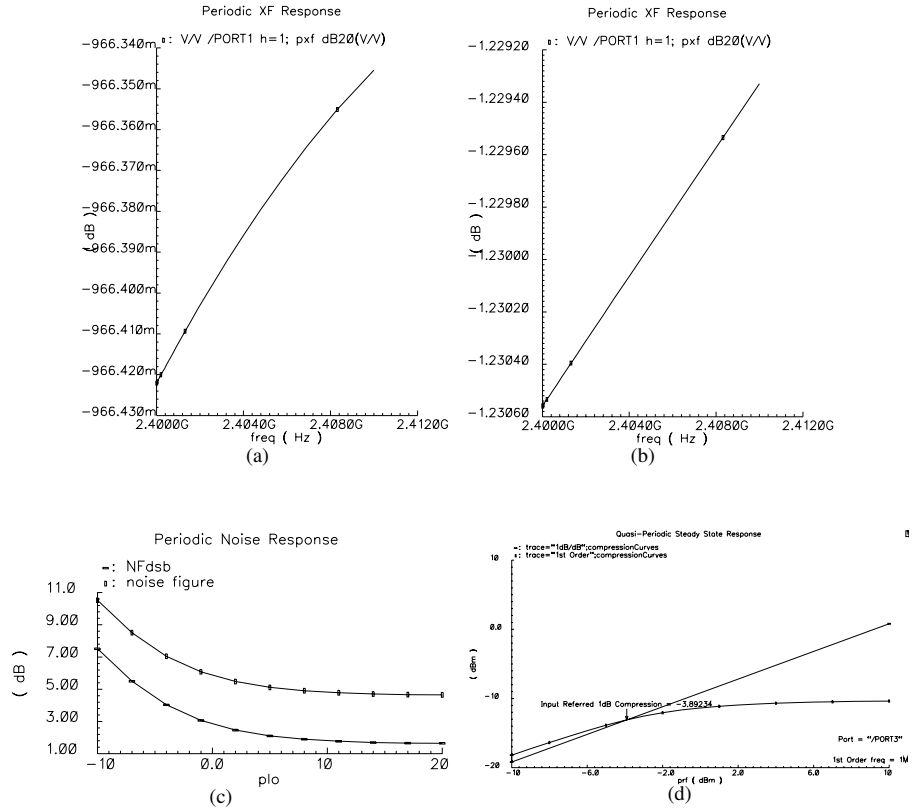


Fig. 7. Simulated Performances of the Passive Switch Mixer: (a) Voltage Conversion Gain with LO Power of $+2.5$ dBm, (b) Voltage Conversion Gain with LO Power of -1 dBm, (c) Noise Figure at 1 KHz, and (d) Input-referred 1-dB Compression Point.

performances is a high LO power requirement. Decreasing the LO power to -1 dB does not affect significantly the conversion gain that drops to -1.23 dB (as depicted in Fig. 7 (b)); the noise figure drop is also of little importance since it worsens by 1 dB. However, the impact on linearity is important since the input-referred 1-dB compression point is below -7 dBm with a LO power of 1 dB. Observe that these comparisons are qualitative and their main goal is only giving the reader a general view of the strength and weakness of the proposed design. In fact, the implementation described in this paper has only been laid out and simulated; nevertheless the comparisons are carried out with implemented designs with measured data.

D. Quadrature VCO

In modern RF applications such as zero or low-IF transceivers, the local oscillator must provide precise quadrature phases for either modulation or demodulation of the data streams in I and Q channels. This goal may be easily accomplished by using two cross-coupled VCOs as shown in Fig. 8. However, using a quadrature VCO might lead to a huge area penalty and to an excessive power consumption that is not desirable in mobile applications. To tackle area and power overheads, a negative G_m scheme is implemented with PMOS and NMOS cross-coupled pairs to allow the implementation of a floating LC tank. The UMC process does not provide the designer with tapped inductors, consequently, a floating tank is the best choice to save die area since only one inductor is necessary to implement the tank. Low power consumption is achieved by trading-off between bias current and oscillator output swing. The negative transconductance is implemented by the cross-coupled NMOS and PMOS transistors, oscillation frequency is tuned by a NMOS inversion-mode varactor. All transistors are minimum length; all transistors are minimum length and 20 μm wide. Bias transistors are used to draw from the supply a bias current of $I_b = 1.75$ mA. Supply voltage is 1.2 V, hence VCO power consumption is 2.1 mW. Cross-coupled transistors implement a negative resistance $R_i = -\frac{1}{g_m}$, where g_m is the transistor transconductance. The negative resistance value is designed to cancel the inductor parasitic resistance, namely, $R_i = -2R_s(1+Q^2)$. R_s being the parasitic series resistance and Q the quality factor of the inductor. In this way power is transmitted from the inductor to the capacitance of the LC tank and vice versa, and the circuit oscillates. In order to start the oscillation, transistor transconductance must be at least $g_m \geq \frac{R_s C_{tank}}{L_{tank}}$, where L_{tank} and C_{tank} are, respectively, the inductance and the capacitance of the LC tank of the oscillator. Bias, parasitics and inductor quality factor also affect the oscillator output swing ΔV, since $\Delta V = R_s I_b(1+Q^2)$ [12]. Bias current must be kept low to minimise power consumption, hence, due to the square dependence on Q, inductors quality has a great impact on the output swing. High quality inductors are necessary if a high output swing is a major design concern.

The LC tanks are formed by two inductors $L_d = 4$ nH,

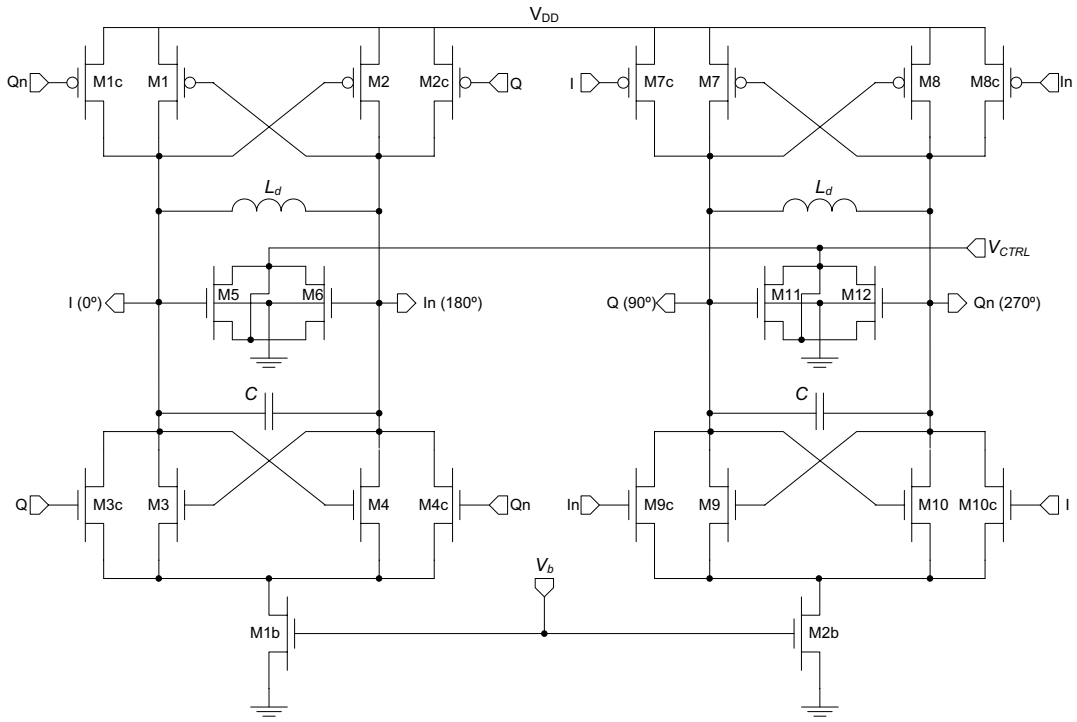


Fig. 8. Negative G_m Quadrature Voltage-Controlled Oscillator (Bias Network not Shown).

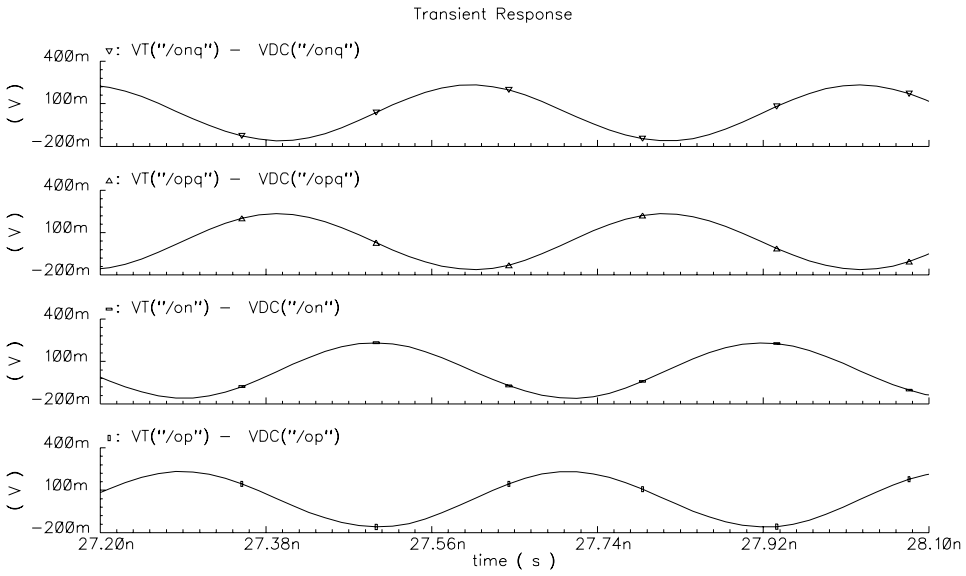
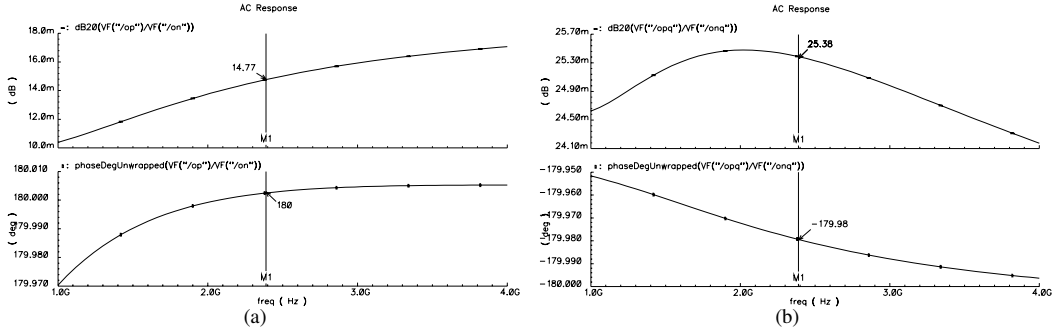


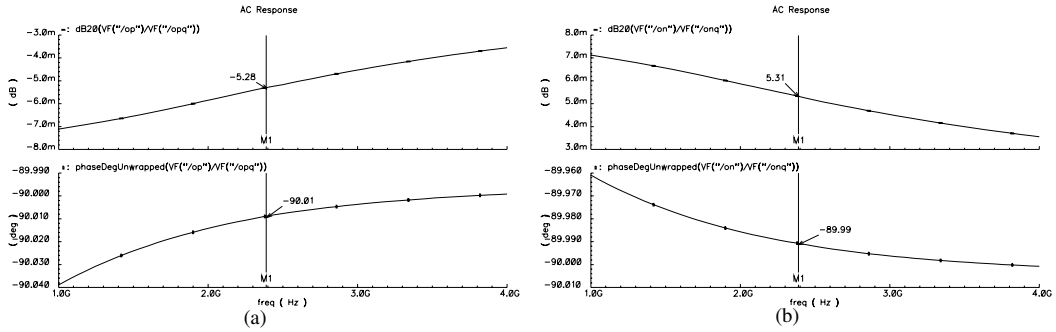
Fig. 9. Oscillator Output.

two capacitors $C = 766.8$ fF, and two MOS inversion-mode varactors formed by transistors M5-M6 and M11-M12 respectively. Transistors are minimum length and 90 μm wide and must be carefully laid out in order to minimise gate resistance. In the practice they are implemented by folding the channel width into 90 fingers of 1 μm length. An inversion-mode varactor is better than other implementations due to the smoothness of its gate capacitance versus v_{gs} characteristics. Fig. 9 shows the QVCO output waveforms. Observe that, once filtered the DC output level of approximately 0.7 V, the signal swing is about 0.4 V. Gain and phase mismatches of both balun and QVCO affect the downconverted signal since the level drift and delay introduced may lead to conversion errors when sampling at the theoretical instants. Hence, an estimation of the gain and phase errors introduced by the analog part of the transceiver is of paramount importance in order to set the size of the decision box of the digital demodulator. Fig. 10 shows the gain and phase mismatch of the in-phase and the quadrature-phase part of the QVCO. Observe from Fig. 10 that both gain and phase matching between the 0° and 180°



(a) (b)

Fig. 10. Gain and Phase Mismatches of: (a) In-phase Signal Generator of the QVCO (0° and 180° components), and (b) Quadrature-phase Signal Generator of the QVCO (90° and 270° components).



(a) (b)

Fig. 11. In-phase and Quadrature-phase Components Gain and Phase Mismatches: (a) 0° and 90° components, and (b) 180° and 270° components.

components and 90°, and 270° components respectively, is almost perfect. However, even more important is the gain and phase matching between the two VCOs that form the QVCO, i.e. the mismatch between 0° and 90° components, 180° and 270° components respectively. These evaluations are reported in Fig. 11. Also in this case the matching among the components is excellent. To improve matching, the QVCO has been designed with a coupling factor $k = 1$. This means that coupling transistors and cross-coupled transistors pairs have the same size. A coupling factor of 1 is detrimental for the phase noise [16], however it allows the best matching between in-phase and quadrature output waveforms and is the best design choice when design constraints on phase noise are not very strict, like in the case of ZigBee.

Fig. 12 shows the oscillation frequency as a function of the varactor control voltage V_{CTRL}. The designed VCO may oscillate between 2.391 (when $V_{CTRL} = 0$ V) and 2.531 GHz (when $V_{CTRL} = 0.7$ V). In ZigBee a high tuning range is not a major concern since the useful band goes from 2.4 to 2.48 GHz.

The ZigBee standard requires an oscillator phase noise at 1 MHz frequency offset from the carrier of at least -88 dBc/Hz [17]. The simulated phase noise is depicted in Fig. 12 and is -116.7 dBc/Hz at the required frequency offset. As a consequence, the proposed QVCO is suitable for ZigBee applications. Simulation results are summarized in Table III, whereas Table IV shows performance comparisons with other implementations. The figure of merit used in the comparisons

TABLE III
SUMMARY OF VCO PERFORMANCE.

Parameter	value
Frequency Tuning	2.391-2.531 GHz
Phase Noise @ 1 MHz	-116.7 dB
VCO gain	228 MHz/V
Current Consumption	1.75 mA
Supply Voltage	1.2 V
Die Area	0.19 mm^2
Technology	0.13 μm CMOS

is [18]:

$$FoM = PN(f_{off}) - 20\log_{10}\left(\frac{f_o}{f_{off}}\right) + 10\log_{10}\left(\frac{P_{DC}}{1\text{ mW}}\right)$$

where, f_o is the oscillation frequency, f_{off} the frequency offset, $PN(f_{off})$ the phase noise computed at the frequency offset, and P_{DC} is the DC power consumption.

The figure of merit takes into account three factors: noise figure of the oscillator, frequency of oscillation, and DC power consumption. The smaller is the figure of merit, the better the oscillator because this means that the oscillator is able to work at high frequencies with very low noise figure and power consumption. Observe that the proposed implementation has the best figure of merit and power consumption. This is of paramount importance in portable systems applications. The phase noise is not the best, however it is sufficient to comply with ZigBee specifications that require at least a -88 dBc/Hz phase noise at a frequency offset of 1 MHz from the carrier.

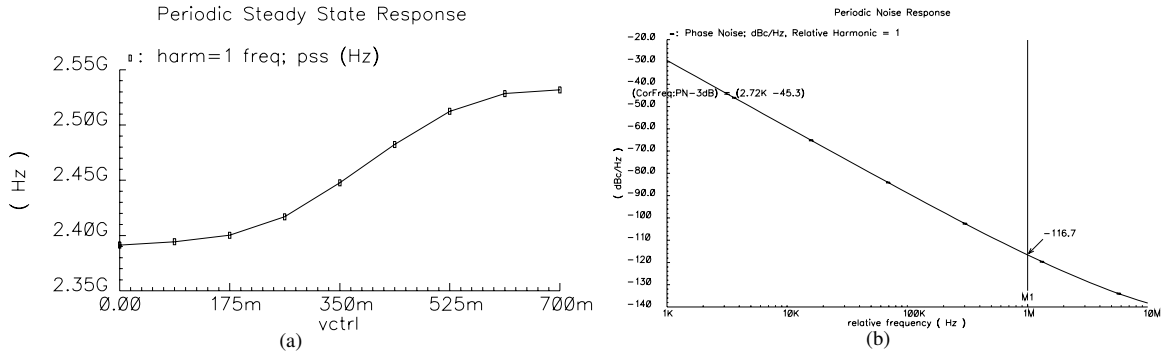


Fig. 12. Oscillation Frequency vs. Varactor Control Voltage.

TABLE IV
COMPARISONS SUMMARY WITH PREVIOUSLY REPORTED IMPLEMENTATIONS.

Implementation	Power Consumption	Phase noise (@ 1 MHz)	Operating frequency	Technology	FoM (dB)
[19]	5.40 mW	-120 dBc/Hz	1 GHz	0.18 μm	-172.67
[4]	2.70 mW	-107 dBc/Hz	5.15 GHz	0.18 μm	-176.91
[15]	5.56 mW	-114.6 dBc/Hz	2.4 GHz	0.25 μm	-174.75
This work	2.10 mW	-116.7 dBc/Hz	2.4 GHz	0.13 μm	-181.08

In this case as well, the same remark previously made for the mixer applies. Hence also the comparisons of Table IV are qualitative since the comparison is carried out between a laid-out and fabricated designs.

III. COMPARISONS

In this section receiver performance are evaluated. In the sequel the estimated performance are compared with those of similar implementations. The comparisons are carried out by considering several figures of merit, such as power consumption, noise figure, receiver sensitivity and input-referred 1-dB compression point.

Table V summarises the contributions to die area occupation and power consumption of each of the blocks that form the receiver. The receiver has an area of 0.70 mm^2 and an overall power consumption of 14.6 mW with a 1.2 V supply voltage. Table VI reports the cumulative values of the main figures of merit of the receiver, obtained by a cascaded computation. The high gain and low noise of the LNA, leads to an extremely low cumulative noise figure of only 2.27 dB. On the other hand, the cumulative input-referred 1-dB compression point is -19.8 dBm, matching the ZigBee linearity requirements. The receiver sensitivity is -97 dBm and it has been computed assuming a QPSK coherent demodulation scheme and a BER of 5.7×10^{-5}, as required by the IEEE 802.15.4 standard. The implementation described in this work has been compared with several recent implementations and the results are summarised in Table VII. Observe that these comparisons are qualitative and their main goal is only giving the reader a general view of the strength and weakness of the proposed design. In fact, the implementation described in this paper has only been laid out and simulated; nevertheless the comparisons are carried out with implemented designs with measured data. The front-end described in [9], [8] are ZigBee compliant and work in the 900 and in the 2400 MHz band respectively. They are full implementations that include, on-chip receiver, transmitter, frequency synthesis subsystem, variable-gain amplifiers and filters. However, the performance comparison will be carried-out only with the receiver subsystem. On the other hand, the implementation described in [10] is an ultra low-power receiver for wireless sensor networks not complying with ZigBee standard and operating in the 2400 MHz band. The receiver described in [10] has a very low-power consumption; however, this has been achieved by sacrificing linearity and noise figure. The receiver proposed in this work has excellent sensitivity, noise performance and linearity, as well as a better power consumption that those reported in [9] and [8]. Nevertheless, the measures reported in [9], [8] include also the PLL power consumption.

IV. CONCLUSION

A novel ZigBee-compliant receiver operating in the 2400 MHz ISM band has been presented. The circuit has been laid out and simulated using a 0.13 μm 1P8M process. The receiver is composed by a single-end LNA, an active balun, a quadrature passive switch mixer, buffers, and a quadrature VCO, and operates with a 1.2 V supply voltage. The circuit has a small die area of approximately 0.7 mm^2. This has been achieved by reducing to eight the number of inductors and exploiting bondwire inductances to reduce on-chip inductors size. The design exhibits excellent performances, as demonstrated by the comparisons summarised in Table VII. Simulations predict a 2.27 dB noise figure, a -97 dBm sensitivity, a -19.8 dBm input-referred 1-dB compression point, and a 14.6 mW power consumption.

TABLE V
SUMMARY OF THE RECEIVER AREA AND POWER CONSUMPTION.

Component	Area [mm^2]	Power [mW]
LNA	0.12	2.0
Balun	0.01	3.5
Quadrature Mixer	0.38	0.0
Quadrature VCO	0.19	2.1
Buffers	-	7.0
Total	0.70	14.6

TABLE VI
SUMMARY OF THE RECEIVER CUMULATIVE FIGURES OF MERIT.

Figure of Merit	LNA	Balun	Mixer	**Total**
NF	1.34	7.7	5.8	2.27
Gain[a]	17.3	0.36	−0.96	16.7
P-1dB	−17.8	−4.8	−3.98	−19.8

[a] Voltage gain.

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TABLE VII
COMPARISON SUMMARY WITH PREVIOUSLY REPORTED IMPLEMENTATIONS.

	This Work	[9]	[8]	[10]	
				w/o curr. reuse	curr. reuse
Supply [V]	1.2	1.8	1.8	1.0	1.0
Tech. [μm]	0.13	0.18	0.18	0.18	0.18
Frequency [GHz]	2.4	0.9	2.4	2.4	2.4
Power [mW]	14.6	25.2	26.46	0.50	0.50
Noise Fig. [dB]	2.27	9.5	5.7	19	10.1
Sensitivity [dBm]	-97	-98	-101	-90	-90
IIP3 [dBm]	-10	-10	-16	-23	-31
LO PN [dBc/Hz] (@ 1MHz)	-116.7	-108	N/A	-115.8^a	-115.8^a

[a] Supply voltage 0.7 V.