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Feed-Forward Control in Resonant DC Link Inverter

Apinan Aurasopon, and Worawat Sa-ngiavibool

***Abstract*—**This paper proposes a feed-forward control in resonant dc link inverter. The feed-forward control configuration is based on synchronous sigma-delta modulation. The simulation results showing the proposed technique can reject non-ideal dc bus improving the total harmonic distortion.

***Keywords*—**Feed-forward control, Resonant dc link inverter, Synchronous sigma-delta modulation.

I. Introduction

IN resonant link converter techniques, the dc bus voltage is used to resonate an LC network, the oscillation of this network gives rise to instants of zero voltage. Therefore, the output power switched are connected to the network such that switching occurs at such zero crossing, then switching losses are significantly reduced [1].

However, the resonant dc link system operates well under condition of an ideal dc bus (ripple-free) obtained by means of a passive dc link filter. To achieve a very low ripple, however, requires large filters. This increases the cost, size, and weight and reduces the overall efficiency of the conversion process. Furthermore, in a practical converter system, it is difficult to realize an ideal dc bus for a number of practical constraints. Most of the dc bus converter systems use a front-end diode bridge for AC–DC rectification. The ripple in the dc bus is undesirable, as it causes low-order harmonics appearing in the inverter output. These harmonics are difficult to filter out and cause deterioration in the quality of the output voltage. The feed-back control may be used to reject these harmonics. However, in case of the dc bus voltage v_{dc} is perturbed. The overshot voltage will be appeared at inverter output before the control process produces control signal. This problem can be solved by feed-forward and One-Cycle control techniques [2] [3]. However, the clock signal used in processing of these techniques is not synchronized with the width of pulse width modulation (PWM) signal. This paper therefore proposes a feed forward control using synchronous sigma-delta modulation (SSDM) configuration. The features of the proposed pattern generator are highlighted. The parameters affecting the performance of rejection capability are discussed. The simulation and experimental results show the total harmonic distortion of the proposed control technique reduced.

Apinan Aurasopon and Worawat Sa-ngiavibool Faculty of Engineering, Mahasarakham University, Kantharawichai district, Mahasarakham 44150, Thailand (phone: +6645-754321, fax: +6645-754316; e-mail: aurasopon@yahoo.com).

II. Resonant DC Link Circuit

The three phase resonant dc link inverter system shows in Fig. 1. The switch Ms is used to produce the initial inductor current as shown in Fig. 1 (a). The result is the periodic sinusoidal dc link voltage, $v_d(t)$. In Fig. 1 (b), the power switches M1-6 are modified to include the action of Ms. So it is possible that the power switches of inverter circuit can operate at high switching frequency without switching losses if they are turned on and turned off at zero crossing of $v_d(t)$. Fig. 1 (c) shows the line-to-line voltage v_{ab} and its fundamental component.

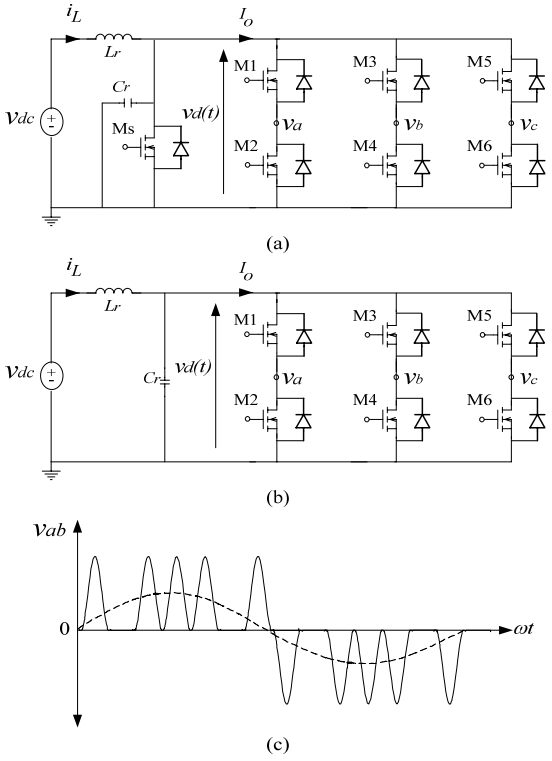

Fig. 1 Circuit schematics of three-phase resonant dc link inverter. (a) Seven switches and (b) Six switches (c) Low frequency ac waveforms

III. Resonant DC Link Inverter Equivalent Circuit

A. Ideal DC Bus Voltage

Fig. 2 (a) shows the equivalent resonant dc link circuit. The switch Ms is turned on by the short pulse to provide initial condition of inverter operation. When Ms is opened, the dc bus oscillates and returns to zero generating, $v_d(t)$, where upon Ms is turned again. Then, this process can be repeated. The resonant link voltage, $v_d(t)$, is given by [1]:

$$v_d(t) = Z(i_{L(0)} - I_0)\sin(\omega t) + v_{dc} + (v_{d(0)} - v_{dc})\cos(\omega t) \quad (1)$$

where

$i_{L(0)}$ initial resonant inductor current;

$v_{d(0)}$ initial resonant capacitor voltage;

I_0 load current;

ω angular frequency = $2\pi f_c$;

Z resonant impedance = $\sqrt{L_r / C_r}$.

Equation (1) shows that $v_d(t)$ is a function of dc bus voltage $v_{dc}(t)$ and output current. However, the dc link voltage peak depends strongly on $v_{dc}(t)$, which is about $2V_{dc}$ as shown in Fig. 2 (b). Therefore, the dc link voltage average $\tilde{v}_d$ can be found

$$\tilde{v}_d = \frac{4V_{dc}}{\pi(1 + t_{on} / t_{off})} \quad (2)$$

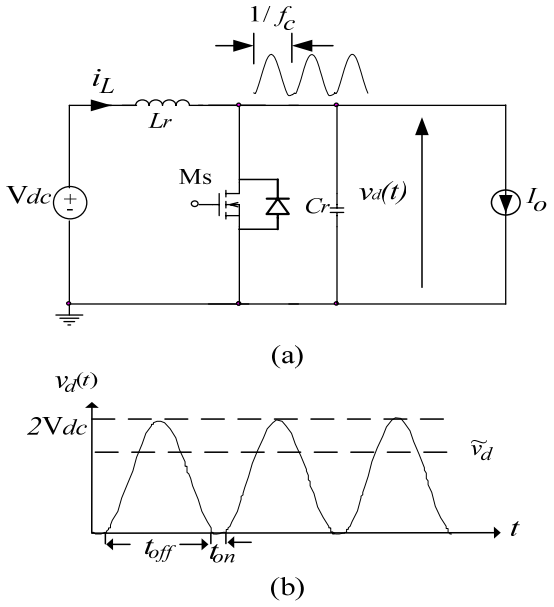

Fig. 2 (a) Resonant dc link inverter equivalent circuit (b) DC link voltage

B. Non-Ideal DC bus Voltage

From previous subsection, the dc bus voltage is assumed as a constant voltage. However, in practical it is difficult to realize the constant dc voltage source. Equation (2) shows the dc link voltage average depending on the dc bus voltage, $v_{dc}(t)$, which uses to determine the fundamental voltage output amplitude. When $v_{dc}(t)$ is swigged causing the variation of $\tilde{v}_d$ in each switching period as shown in Fig. 3. The result is to appear the low order harmonics causing power losses in output voltage.

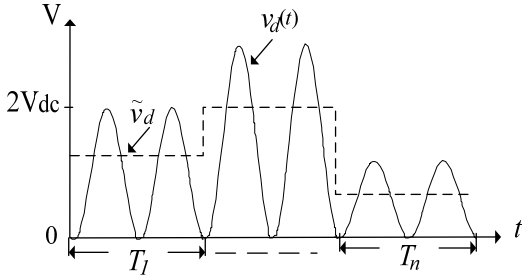

Fig. 3 DC link voltage in case of non-ideal dc bus

IV. Feed-Forward Control SSDM

Fig. 4 shows the feed forward control sigma delta modulation (FFC-SSDM) in three-phase inverter. The non ideal dc bus is sent to be the control information and reduced by gain A. This voltage is controlled by the D-Flip-Flop output, Q and $\overline{Q}$. The result is to generate the forward voltage, $v_s(t)$. Therefore, the error signal, *e*, is the difference between the input voltage v_i and the forward voltage, $v_s(t)$. The $v_s(t)$ is fed to an integrator to produce the integrated error signal E. The E then is fed to a quantizer, the output of which depends on the polarity of E. For E positive an output of $+V_e$ is produced, whereas for negative values of E an output $-V_e$ is produced. The quantizer output is strobe by sample and hold) at a frequency f_c (the link frequency) to give the output waveforms Q and $\overline{Q}$. Fig. 5 (a) shows generating the switching waveforms of M1 and M2. At the resonant frequency, the both switches have to be turned on to produce initial condition of inductor current. The logic gates of M1 and M2 show in Fig. 5 (b). Fig. 6 shows the key waveforms of FFC-SSDM. Assuming the input signal is dc voltage. At interval period A, the dc bus voltage, $v_{dc}(t)$, is V_{dc}. Therefore, the forward voltage equals to $\pm V_s$ and produces the constant slopes of integrated error signal E(t). The modulation cycle can be determined by [5].

$$v_i = \frac{1}{T_{sn}} \int_0^{T_{sn}} v_s(t)dt \quad (3)$$

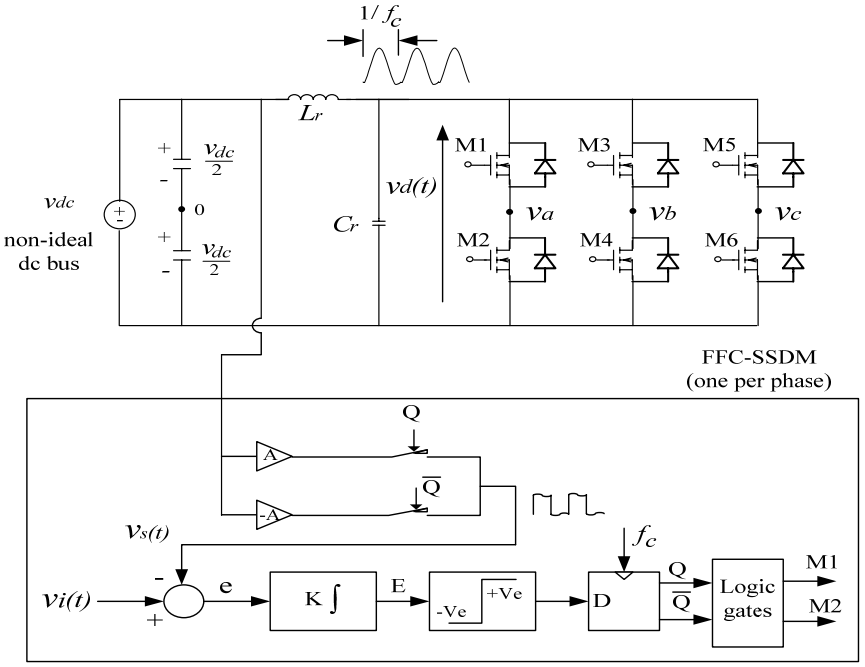

Fig. 4 Block diagram of Feed-forward control sigma-delta modulation

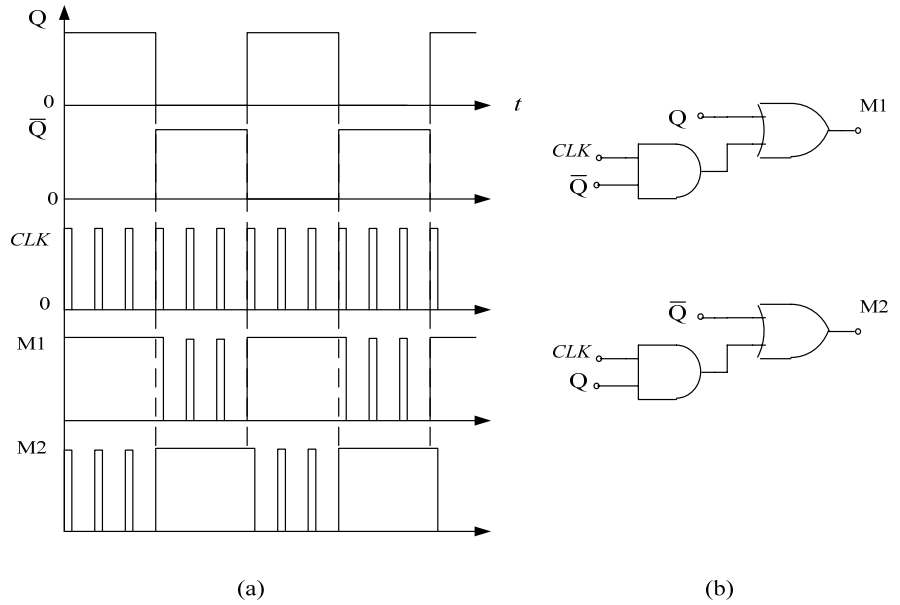

Fig. 5 (a) Switching waveforms (b) Logic gates control M1 and M2

$$T_{sn} = \frac{2T_c}{(1-m(t))} \quad (4)$$

where

$m(t)$ is the amplitude modulation index

$$, \frac{v_i}{v_s(t)} \sin \omega t \ \ (M \sin \omega t);$$

$v_s(t)$ is step down voltage of $v_{dc}(t)$;

T_{sn} is the modulation cycle;

T_c is the modulation clock cycle.

In SSDM process, the pattern modulation repeats every L (number of limit cycles) modulation cycles. The T_{sn} could be different from modulation cycle to the next, although, the v_i and $v_s(t)$ are constant. This is simply because of discretized nature of output. However, this steady state error process will be not considered in this paper. Considering (4), the modulation cycle T_{sn} is proportional to $v_{dc}(t)$. When the $v_{dc}(t)$ increases T_{sn} is reduced as shown at interval period B in Fig. 6. In other words, when the $v_{dc}(t)$ reduces, the T_{sn} increases,

respectively. The T_{sn} is still corresponded with pulse number of resonant dc link voltage.

$$p_n = \frac{T_{sn}}{T_c} - 1 \tag{5}$$

where p_n is the pulse number of positive resonant dc link voltage.

The phase voltage average of inverter can be found by integrating v_a

$$\tilde{v}_a = 0.5\tilde{v}_d \frac{(p_n - 1)}{(p_n + 1)} \tag{6}$$

As shown in Fig. 6, p_n is varied as proportional to T_{sn} and $v_{dc}(t)$. Therefore, the phase voltage average is equal to v_i in each modulation cycle. The result is to reject the non-ideal dc bus voltage. This should also be true in case of sinusoidal input voltage. However, there are some parameters that affect the ripple rejection capability, which will be discussed and simulated in the next topic.

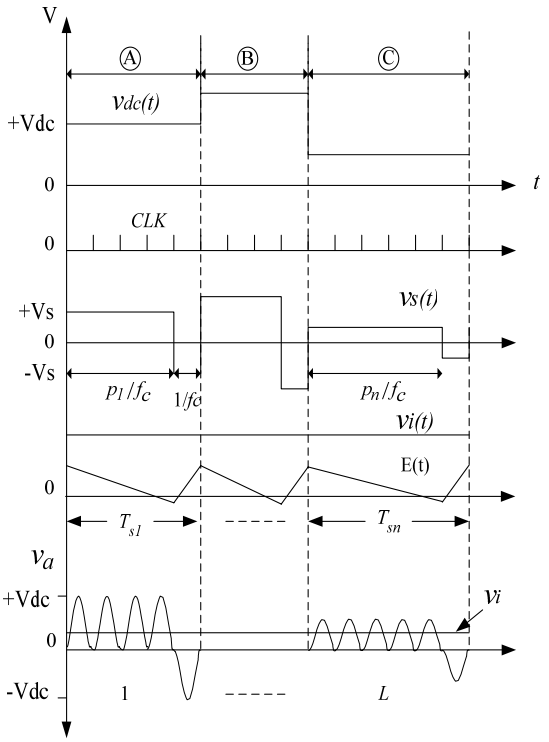

Fig. 6 Key waveforms of FFC-SSDM for dc input signal

V. Simulation Results

To verify the control theory, this session shows the PSpice simulation results. The system parameters of resonant dc link system are set as following: f_c = 40 kHz, V_{dc} = 100 V and output load, R = 10 Ω and L = 10mH, therefore, feed forward gain A = 0.05, L_r = 5 μH , C_r = 3.1 μF and t_{on} = 3 μs , t_{off} = 22 μs . The simulation results in Figs. 7 and 8 use half-bridge resonant dc link configuration (M1 and M2) showing the parameter effects to FFC-SSDM performance. Fig. 7 shows the relationship between dc bus voltage and positive pulse number average, $\tilde{p}_n$ where $\tilde{p}_n = (p_1 + p_2 ... + p_n)/L$ while input signal is dc voltage. It shows the $\tilde{p}_n$ varying as proportion with dc bus voltage. Fig. 8 shows the variation of dc link voltage average $\tilde{v}_d$ that affects phase voltage average $\tilde{v}_a$. These results use equation (6) for plotting. It shows the constant of phase voltage average $\tilde{v}_a$ to the variation of dc link voltage average $\tilde{v}_d$.

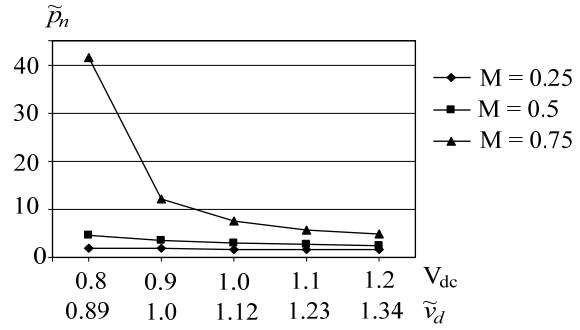

Fig. 7 Positive pulse number average versus variation of dc bus voltage

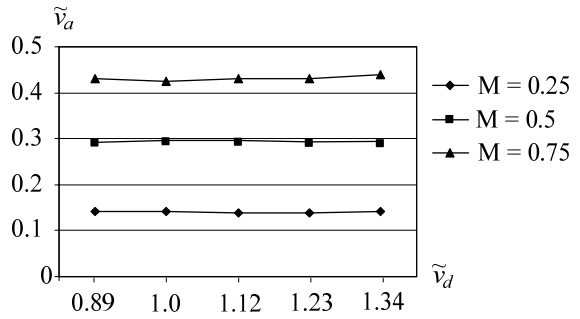

Fig. 8 Output voltage average versus variation of resonant dc link voltage average

The results in Figs. 9 to 12 use three-phase resonant dc link configuration in Fig. 4. The resolution of Fast Fourier Transform (FFT) for measuring harmonic spectrum is set at 5 Hz (sampling time 100 ms). The total low order harmonic distortion in output voltage used to measure rejection ability is defined as:

$$THD_{lv} = \frac{\sqrt{V_{f_r - f_i}^2 - V_{f_r + f_i}^2}}{k_r V_{dc}} \tag{7}$$

To show the performance of control technique, the ripple voltage is added with dc bus voltage where the dc bus ripple factor k_r is set at 0.1 and ripple frequency f_r is 200 Hz. Figs. 9 and 10 show the results of various control techniques. The line-to-line voltage is swing to follow the dc bus voltage as shown in Figs. 9-10 (a) and its harmonic spectrum shows in Figs. 9-10 (b). Figs. 9-10 (c) is the output current. In the open loop control (OLC), the result is causing high total low order harmonics distortion THD_{lv}, 12.2% and total current harmonic

distortion (THD_i), 4.9%. These harmonic distortions can be solved by FFC-SSDM as shown in Fig. 10. It indicates the performance of FFC-SSDM. The THD_{lv}, is only at 0.58% and THD_i is at 3.1%.

Figs. 11 and 12 show the effects of amplitude modulation index, M, and ripple frequency, f_r, to ripple rejection capability. In Fig. 11, when M increases causing high THD_{lv}. This is because its $\tilde{p}_n$ is strongly nonlinear with variation of dc bus voltage as shown in Fig. 7. Fig. 12 shows the effect of ripple frequency, f_r. The result shows high ripple frequency causing the ripple rejection capability reduced. However, in the most practical applications, the dc bus voltage that is generated by means of a diode rectifier has only low ripple frequency.

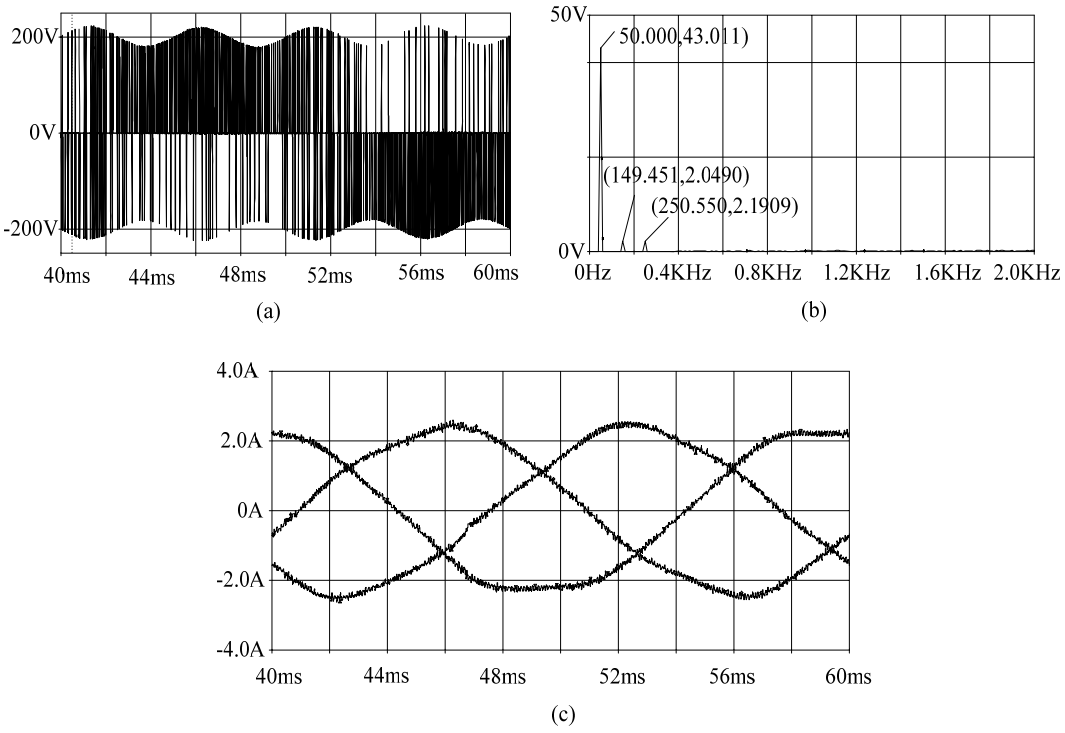

Fig. 9 Simulation results of open loop control resonant dc link inverter. (a) Line-to-line voltage v_{ab} and its harmonic spectrum (b). (c) Load currents: M = 0.5

These simulation results show that FFC-SSDM can effectively reject the variation of dc bus voltage and improve the total harmonic distortion.

VI. Conclusion

This paper proposed the feed-forward control in resonant dc link inverter. The control technique is simple and can effectively reject the non-ideal dc bus voltage. The parameters affecting the performance of the control technique were discussed. The simulation results confirmed its ability of low order harmonics rejection.

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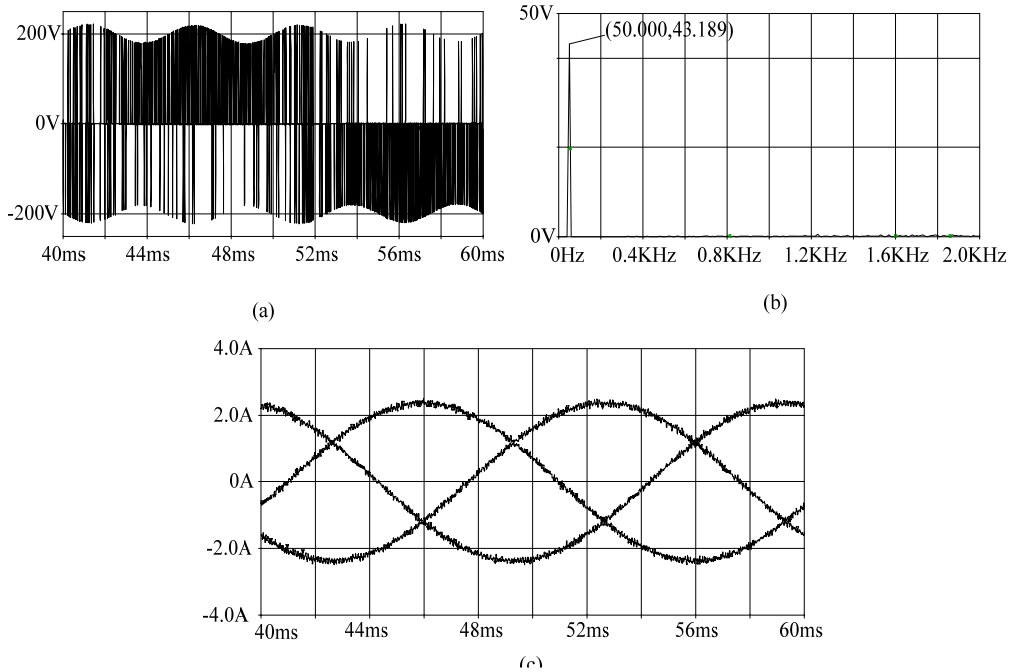

Fig. 10 Simulation results of FFC-SSDM resonant dc link inverter. (a) Line-to-line voltage v_{ab} and its harmonic spectrum (b). (c) Load currents: M = 0.5

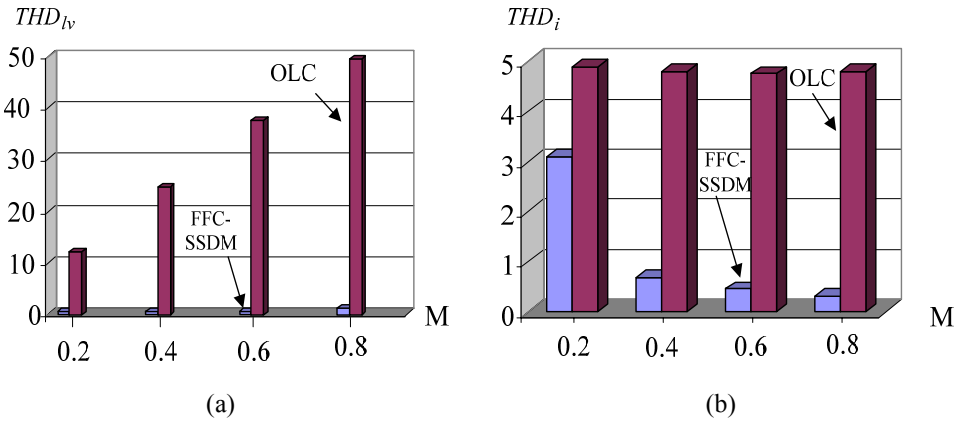

Fig. 11 (a) Total low order harmonic distortion of line-to-line voltage. (b) Total harmonic distortion of output current: f_r = 200 Hz, k_r = 0.1

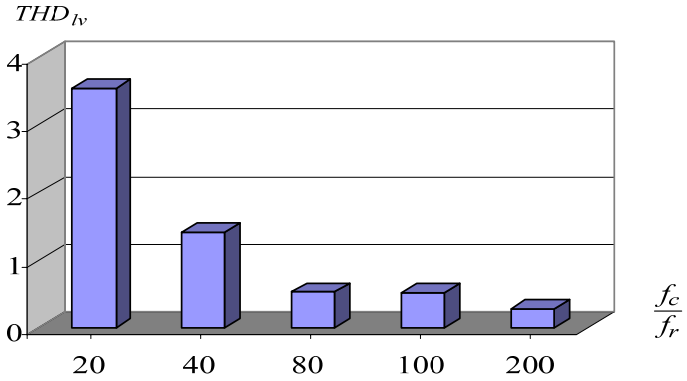

Fig. 12 Total low order harmonic distortion of line-to-line voltage of FFC-SSDM versus ripple frequency: k_r = 0.1