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Modeling of a Second Order Non-Ideal Sigma-Delta Modulator

Abdelghani Dendouga*, Nour-Eddine Bouguechal, Souhil Kouda and Samir Barra

***Abstract*—**A behavioral model of a second order switched-capacitor Sigma-Delta modulator is presented. The purpose of this work is the presentation of a behavioral model of a second order switched capacitor ΣΔ modulator considering (Error due to Clock Jitter, Thermal noise Amplifier Noise, Amplifier Slew-Rate, Non linearity of amplifiers, Gain error, Charge Injection, Clock Feedthrough, and Nonlinear on-resistance). A comparison between the use of MOS switches and the use transmission gate switches use is analyzed.

***Keywords*—**Charge injection; clock feedthrough; Sigma Delta modulators; Sigma Delta non-idealities; switched capacitor.

I. Introduction

SIGMA Delta (ΣΔ) modulators have achieved the most attraction topologies for digitizing with high-resolution analog signals characterized by their noise shaping behavior and there low sensitivity to circuit imperfections [1].

Oversampling data converters are able to achieve over 20 Effective Number Of Bits (ENOB) resolution at reasonably high conversion speeds by relying on a trade-off. They use sampling rates much higher than the Nyquist rate, typically higher by a factor between 8 and 512, and generate each output utilizing all preceding input values [2][3]. The most popular approach is based on a sampled-data solution with Switch Capacitor (SC) implementation. For this reason, we will focus on the case of SC modulators in this paper.

Given the diversity of architectures implementing converter can not exist a generic model for all ADCs each architecture implementation of converter requires its own model. In this paper we analyzed the performances of a second order sigma-delta modulator including non-idealities compared to its ideal model. To do this, we must define the parameters for estimating this feature can characterize an ADC, and the tolerances on these parameters.

In this work we will define in the first part the parameters (errors) that can affect on the performances of the Sigma-Delta modulator. In the second part, we will present a non-ideal Sigma-Delta modulator model and showing the different effects providing by each circuit imperfection, and the difference between the use of the NMOS switch and the CMOS switch (transmission gate).

Abdelghani Dendouga is with the Advanced Electronics Laboratory of BATNA University, 05 Avenue Chahid Boukhlouf, 05000 BATNA, ALGERIE (fax: +213-33-81-54-54; e-mail: dendouga_gh@hotmail.com).

II. Clock Jitter

The sampling operation assumes a perfect clock, whose period is well defined and stable over time. The intrinsic noise devices that will produce the clock oscillator (fixed or variable oscillator, phase locked loop...) however introduce some uncertainty t_j (jitter) on the exact moment of sampling.

Jitter is mainly caused by thermal noise, phase noise and spurious components in every clock-generation circuitry. In a SC circuit, jitter is generally defined as short-term, non-cumulative variation of the significant instant of a digital signal from its ideal position in time [7]. Sampling clock jitter results in non-uniform sampling and increases the total error power in the quantizer output.

The magnitude of this error is a function of both the statistical properties of the jitter and the modulator input signal.

This effect can be simulated with SIMULINK® by using the model shown in Fig. 2, which implements Eqn. (1). Here, we assumed that the sampling uncertainty δ is a Gaussian random process Fig. 1 with standard deviation $\Delta\tau$ [14][8].

$$x(t+\delta)-x(t)\approx 2\pi f_{in}\delta A\cos(2\pi f_{in}t)=\delta\frac{d}{dt}x(t) \quad (1)$$

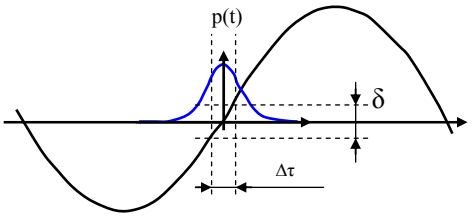

Fig. 1. Effect of clock jitter in the sampling.

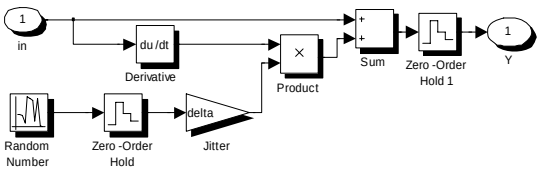

Fig. 2. SIMULINK® Model of a random sampling jitter.

III. Noise on Integrator

The two primary sources of noise in a switched-capacitor circuit are the resistance of the switches in the on state and the amplifier [8]. To determine the density of noise introduced by the integrator, we must choose a topology of the integrator. Either, the switched capacitor integrator in Fig. 3 with

feedback. In the following, we will study the influence of noise generated by the integrator on the Sigma-Delta modulator.

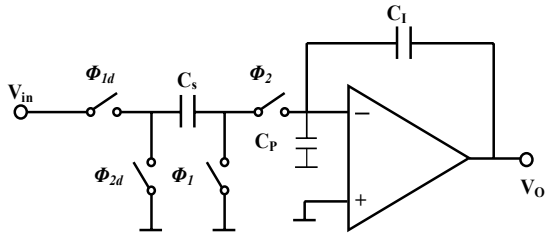

Fig. 3. Simple integration with feedback.

A. Thermal noise

According to Nyquist theorem the spectral density of noise at the terminals of a dipole passive depends only on the temperature and the real part of impedance of the dipole. In a switched capacitor integrator switches operate in ohmic region, the noise power at their terminals is equal to:

$$E_{sff}^2 = \gamma(f)\Delta f = 4KTR\Delta f \tag{2}$$

The noise due to switch on phases I and P is given bay the eqns (3) and (4):

Phase I

$$V_{thP}^2 = \frac{KT}{C_s} + \left(\frac{C_r}{C_s}\right)^2 \frac{KT}{C_r} \tag{3}$$

Phase P

$$V_{thI}^2 = \frac{KT}{C_s} + \frac{KT}{C_r} \tag{4}$$

K is the Boltzman constant ($K = 1.38\ 10^{-23}\ jK^{-1}$) and T the absolute temperature in Kelvin.

The equations (3) and (4) show that if we wishes to reduce the thermal noise power, then we must increase the value of the sampling capacity C_s.

B. Amplifier Noise

The sources of noise present in an amplifier are generally two reasons for the thermal noise and noise in $1/f$. For a MOS transistor in saturation, the voltage generator noise equivalent to the two sources is given by:

$$S_{En} \approx 2\frac{2}{3}KT\frac{1}{g_m} + \frac{k_f}{C_{ox}WL}\frac{1}{f} \tag{5}$$

The first term of this Eqn. (5) represents the equivalent thermal noise of a MOS transistor and the second represents the noise equivalent to $1/f$.

IV. Integrator Imperfections

A. Gain error

The DC gain of the ideal integrator is infinite. In practice, the gain of the operational amplifier open loop A_0 is finite. This is reflected by the fact that a fraction of the previous sample out of the integrator is added to the sample input [4].

The model of a real integrator with an integrator delay is real considering the saturation op-amp, the gain over the finite bandwidth and slew-rate. The Z transfer function of a perfect integrator is given by:

$$H(z) = \frac{z^{-1}}{1 - z^{-1}} \tag{6}$$

The transfer function of the real integrator becomes:

$$H(z) = \beta\frac{z^{-1}}{1 - \alpha z^{-1}} \tag{7}$$

where α and β are the integrator's gain and leakage, respectively [6].

$$\alpha = \frac{A_0 - 1}{A_0} \tag{8}$$

B. Distortion and settling time of the integrator

The distortion limits the power effectively used by the system and its bandwidth. There are various reasons why a signal distorts. Regarding the harmonic distortion, it is mainly due to two factors of nonlinearity and slew-rate of the amplifiers.

- *Non linearity of amplifiers*

Theoretically its transfer function is:

$$V_s = AV_e \tag{9}$$

A is the amplification factor. However simulation we obtain curve in Fig. 4, whose transfer function is approximated given by (10)[5].

$$A \cong A_0\left(1 + \alpha_1|V_o| + \alpha_2|V_o|^2 + \alpha_3|V_o|^3 + \ldots\right) \tag{10}$$

$(\alpha_1, \alpha_2, \alpha_3 \ldots)$ are the amplification factors parasites. Thus, for a pure sinusoidal signal of frequency f in the input of the amplifier, we find the output of the amplifier not only the output signal of departure, amplified, same frequency of V_e but also other parasitic signals with higher frequency and proportional to the frequency f_r, in this case we say that there is harmonic distortion, because this spectrum of frequencies $2f, 3f, ets\ldots$. The THD (total harmonic distortion) is the ratio of the sum of squared amplitudes of these signals on the amplitude of the fundamental.

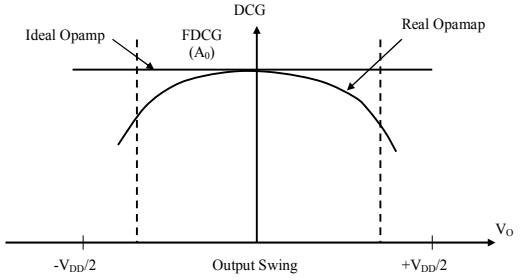

Fig. 4. DC gain of an amplifier as a function of output voltage [9].

- *Amplifier slew-rate*

For a given constant amplitude, slew-rate characterizes the limit of the amplifier frequency (maximal speed).

When a signal is changing more slowly than the maximal speed, the amplifier follows and reproduces faithfully the signal. But when the signal frequency increases (for constant amplitude), The amplifier distorts the output signal. In this case, in addition to the original signal, there are additional frequencies (harmonics). The augmentation of the input signal frequency, cause difficult to the amplifier to restore the signal faithfully.

For the amplifier responds linearly, it generally we define a maximum frequency above which the amplifier distorts the output signal. For a sinusoidal signal of amplitude A pulsation ω, this frequency is defined by:

$$GBW = 2\pi Af \le SR \Rightarrow f = \frac{SR}{2\pi A} \tag{11}$$

For a converter it is:

$$f = \frac{1}{2\pi A 2^n \tau} \tag{12}$$

T is the settling time, $\tau = 1/2\pi GBW$ and n the resolution of the converter.

In the case of a switched-capacitor integrator (the main constituent of a Sigma-Delta modulator) the maximum speed cause an error "settling error" on the output voltage of the integrator.

Indeed, the finite width of the band and "slew-rate" of the amplifier are related and may occur in the switched-capacitor circuit transient response non-ideal (non-linear: called especial mode of operation "slew-rate" producing each clock tick an incomplete charge transfer at the end of the integration period. The effect of the finite bandwidth and the slew-rate are related to each other and may be interpreted as a non-linear gain [16].

V. Switch Non-Idealities

Switches are one of the major elements in SC circuits. The ideal role of them is to have zero or infinite resistance when they are ON or OFF. However, as switches in CMOS technology are realized by using nMOS and pMOS transistor, they manifest some non-idealities such as nonlinear on-resistance, clock- feedthrough, and charge injection [12].

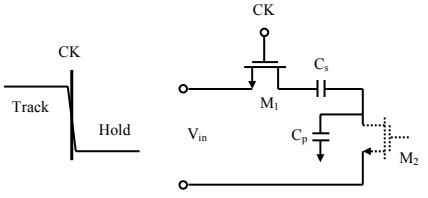

Fig. 5. Simplest sample-and-hold circuit in MOS technology.

A. Charge Injection

When a MOS switch is on, it operates in the triode region and its drain-to-source voltage, V_{DS}, is approximately zero. During the time when the transistor is on, it holds mobile charges in its channel. Once the transistor is turned off, these mobile charges must flow out from the channel region and into the drain and the source junctions as depicted in Fig. 6 [10][11].

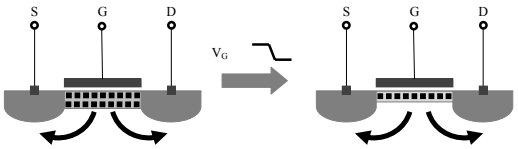

Fig. 6. Channel charge when MOS transistor is in triode region.

For the S/H circuit in Fig. 6, if the MOS switch, M_1, is implemented using an nMOS transistor, the amount of channel charge Q_{ch}, this transistor can hold while it is on is given by Eqn. (13):

$$Q_{ch} = -WLC_{ox}\left(V_{DD} - V_{tn} - V_{in}\right) \tag{13}$$

where W and L are the channel width and channel length of the MOS transistor, C_{ox} is the gate oxide capacitance, and V_{th} is the threshold voltage of the nMOS transistor.

When the MOS switch is turned off, some portion of the channel charge is released to the hold capacitor C_s, while the rest of the charge is transferred back to the input, V_{in}. The fraction k, of the channel charge that is injected into C_s is given by Eqn. (14):

$$\Delta Q_{ch} = kQ_{ch} = -kWLC_{ox}\left(V_{DD} - V_{tn} - V_{in}\right) \tag{14}$$

As a result, the voltage change at V_{out} due to this charge injection is given by Eqn. (15):

$$\Delta V_{out} = \frac{\Delta Q_{ch}}{C_s} = \frac{-kWLC_{ox}\left(V_{DD} - V_{tn} - V_{in}\right)}{C_s} \tag{15}$$

Notice that ΔV_{out} is linearly related to V_{in} and V_{tn}. However, V_{th} is nonlinearly related to V_{in} [10][15]. Therefore, charge injection introduces nonlinear signal-dependent error into the S/H circuit.

B. Clock Feedthrough

Clock feedthrough is due to the gate-to-source overlap capacitance of the MOS switch. For the S/H circuit of Fig. 5,

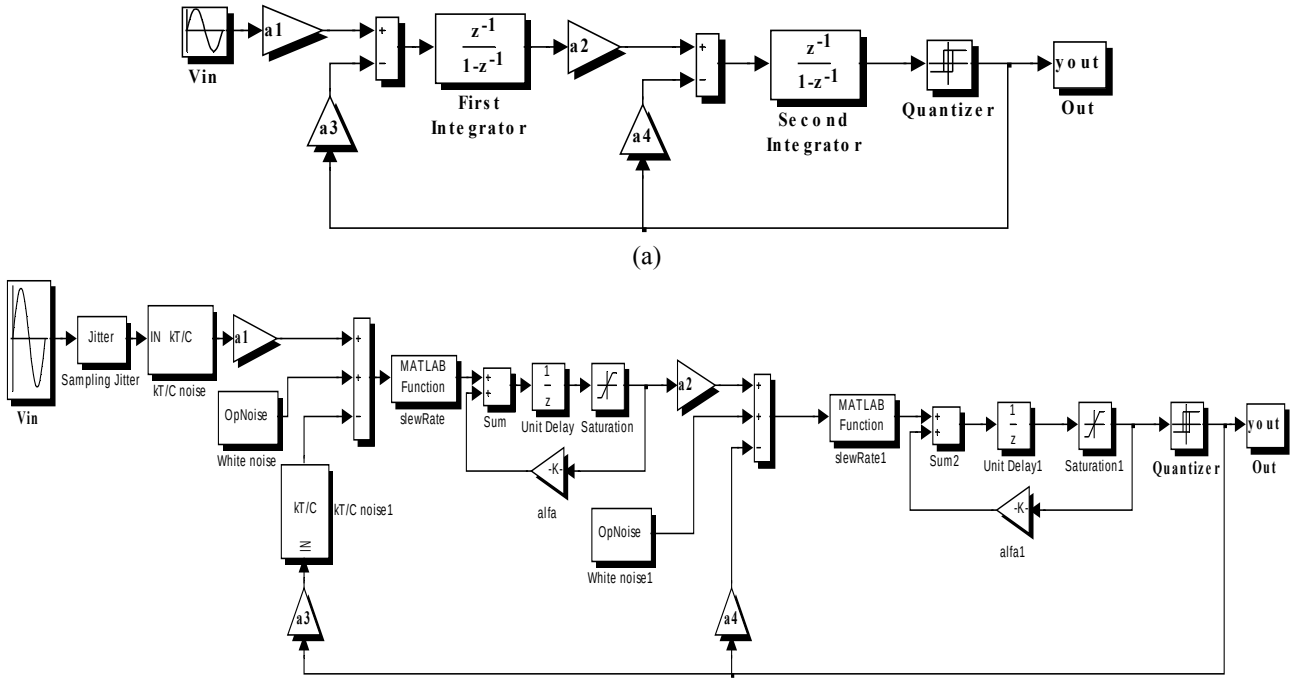

Fig. 7. (a) Ideal second-order single-loop single-bit ΣΔ modulator. (b) Its non-ideal model.

the voltage change at V_{out} due to the clock feedthrough is given by Eqn. (16) [10]:

$$\Delta V_{out} = \frac{-C_p\left(V_{DD} - V_{SS}\right)}{C_p + C_p} \tag{16}$$

where C_p is the parasitic capacitance.

The error introduced by clock feedthrough is usually very small compared with charge injection. Also, notice that clock feedthrough is signal-independent which means it can be treated as signal offsets that can be removed by most systems. Thus, clock feedthrough error is typically less important than charge injection.

Charge injection and clock feedthrough are due to the intrinsic limitations of MOS transistor switches. These two errors limit the maximum usable resolution of any particular S/H circuit, and in turn, limit the performance of the whole system [10][15].

C. Nonlinear ON-resistance

Is a signal-dependent variation of the on-resistance of the switch introduces harmonic distortion into the circuit. There are many ways to degrade this nonlinearity, such as decreasing the sample and hold (S/H) time constant, using transmission gates, clock-boosting and bootstrapping (in low-voltage applications), etc. [12][13].

VI. Simulation Results

In order to validate the behavioral model of our modulator and compare the effects of non-idealities with the ideal modulator Fig. 7, the fundamental blocks for the behavioral simulation of SC ΣΔMs are SC integrators, noise sources such as sampling jitter, and thermal noise, and basic circuits non-idealities such as finite DC Gain, Slew-Rate, Charge Injection …etc. The second-order low-pass modulator shown in Fig. 7. with the parameters listed in TABLE I was used. Were Fig. 7.a shows a model of an ideal modulator and Fig. 7.b the real one.

TABLE I
NOISE DUE TO THE SWITCH

Parameter	Value
Oversampling Ratio (OSR)	256
Clock Frequency (MHz)	12.28
Input Sinusoidal frequency (kHz)	7.3
Samples number	65536
a1, a3	0.2
a2	0.5
a4	0.25
a	1

It is important to note that when an analog signal is sampled, the variation of the sampling period was not a direct effect on circuit performance. Therefore, the clock jitter is only introduced by the sampling signal and thus the effect of this error on a Sigma-Delta converter is independent of the structure or the order of the modulator. We can see that, when the jitter error increases, the total noise power at the output of the quantizer increases. For the same value of uncertainty, frequency of input signal introduces a high power noise more

important. Thus a compromise must be made between a high error and high frequency. Fig. 8 shows the SNR of the modulator for different values of clock jitter.

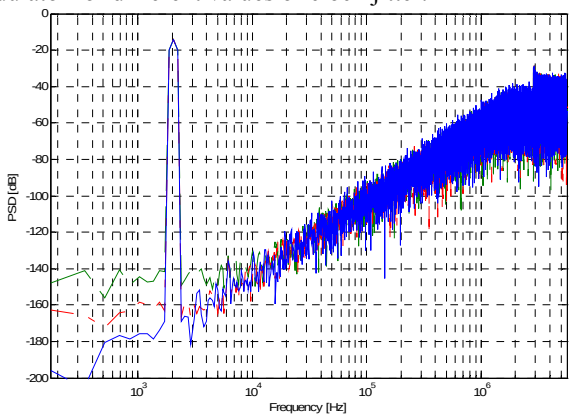

Fig. 8. The PSDs of the modulator output with deferent Clock Jitter.

To reduce the non-linearity introduced by the switch the bootstrapping technique is often used. In this case a dedicated circuit drives the gates of the MOS transistors with a voltage dependent on the input signal (e.g. $V_{DD}+V_{in}$ in the ideal case) in order to maintain the V_{GS} constant. Actually the gate voltage cannot be exactly $V_{DD}+V_{in}$, but is typically $V_{DD}+BSV_{in}$, with BS ranging from 0 (no bootstrapping) to 1 (ideal bootstrapping). In this case, the on-resistance of a complementary CMOS switch becomes [14]:

$$R_{ON}=G_{SN}+G_{SP}=K_N^{'}\frac{W}{L}(V_{DD}-V_{thN}-V_{in}+BSV_{in})+K_P^{'}\frac{W}{L}(-V_{SS}+V_{thP}+V_{in}-BSV_{in}) \quad (17)$$

which is almost independent of the input signal.

where V_{in} Vin is the input voltage, V_{thN} (positive) and V_{thP} (negative) are the threshold voltages of the N-MOS and P-MOS transistors, K'N and K'P are the gain factors of the N-MOS and P-MOS transistors and V_{DD} and V_{SS} are the positive and negative supply voltages used for driving the gates of the N-MOS and P-MOS transistors, respectively.

Fig. 9 shows the PSD of a sigma delta modulator using NMOS switches, and the use of a transmission gate switches. Were Table III sumerize the specifications of the modulator shown in fig. 7 with the parameters listed in Table II.

TABLE II Parameters of the ΣΔM shown in fig. 7 with parameters listed in TABLE I.

TABLE II
PARAMETERS OF THE ΣΔM SHOWN IN FIG. 7 WITH PARAMETERS LISTED IN TABLE I.

Parameter	Value
Sampling Capacitor (pF)	5
Thermal Noise (μV_{rms})	10
Clock Jitter (ns)	1

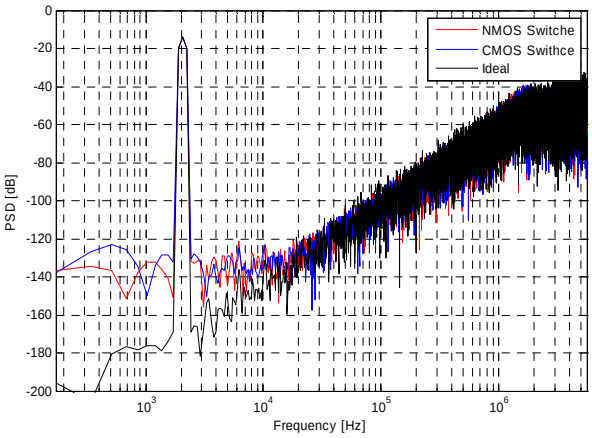

Fig. 9. The PSDs of the modulator output with deferent values of bootstrap.

TABLE III shows the deference between the use of a NMOS switches and the use of a transmission gate switches

TABLE III
SNR AND ENOB FOR THE USE OF NMOS SWITCH AND TRANSMISSION GATE SWITCH.

	NMOS switch	Transmission gate switch
SNR	96.06	96.37
ENOB	15.66	15.71

We can see that the use of transmission gate switches have not a consederable effect on the behavior of the sigma delta modulator, but they have an effect on the power dissipation and many other parameters.

VII. Conclusion

In this paper, a presentation of a behavioral model of the SC ΣΔ modulator including the non-idealities of the modulator (operational amplifier thermal noise, the finite DC gain of the integrator, slew-rate, DC gain nonlinearities, switches Charge Injection, Clock Feedthrough, Nonlinear ON-resistance are presented.

A comparison was made between the use of an NMOS switch and the use of a CMOS (transmission gate) switch.

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