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Resistive RAM Based on Hfo_x and its Temperature Instability Study

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***Abstract*—**High performance Resistive Random Access Memory (RRAM) based on HfO_x has been prepared and its temperature instability has been investigated in this work. With increasing temperature, it is found that: leakage current at high resistance state increases, which can be explained by the higher density of traps inside dielectrics (related to trap-assistant tunneling), leading to a smaller On/Off ratio; set and reset voltages decrease, which may be attributed to the higher oxygen ion mobility, in addition to the reduced potential barrier to create / recover oxygen ions (or oxygen vacancies); temperature impact on the RRAM retention degradation is more serious than electrical bias.

***Keywords*—**RRAM, resistive switching, temperature instability.

I. Introduction

THE conventional memory scaling of flash memory is expected to approach the technical and physical limitations (e.g. lithography, few-electron storage, coupling ratio, and cross-talk) in the near future. Recently, Resistive Random Access Memory (RRAM) has been extensively researched as one of the most promising candidates in the next generation nonvolatile memory or maybe universal memory applications [1] largely due to its characteristics of low power consumption, high speed switching, low voltage operation, high integration density and CMOS compatibility. Various transitional metal oxide (TMO) has been explored as RRAM material candidates for their simple compositions and reported outstanding performance, e.g. NiOx [2], TiOx [3], CuOx [4]. Among them, HfOx has shown exceptional electrical performance [5]. In this work, temperature dependent resistive switching and retention behavior have been investigated on HfOx (TiN/HfOx/Pt) based devices. All the observations can be correlated with the oxygen vacancies (Vo) inside binary oxide (HfOx in this work) dielectrics, which further reinforce the role of Vo assisted conduction filament formation and rupture in the RRAM switching behavior.

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II. Experiment

Hafnium oxide based RRAM devices are fabricated by high temperature oxidation of Hf thin films. First, Hf film is prepared by DC sputtering of Hf target on $Pt/Ti/SiO_2/Si$ substrates, follows by 450°C oxygen furnace annealing for 10 minutes. After that, TiN top electrode is deposited by reactive sputtering and then devices are patterned with lithography and dry etched with final devices area ranging from 5625 to 99225 μm^2. The morphologies of the MIM capacitor are examined by high-resolution transmission electron microscopy (HRTEM), chemical composition of the blank HfO_x film is analyzed by X-ray photoelectron spectroscope (XPS). And the electrical measurement is performed using a Keithley 4200-SCS semiconductor parameter analyzer.

III. Results and Discussion

The chemical composition of the prepared resistive switching layer after oxidation is analyzed by XPS. Hf 4*f* scan shows two peaks at binding energy of 17.1eV and 18.6eV indicating that Hf thin film has been fully oxidized even with short oxidation time (results not shown here). High resolution transmission electron microscope (HRTEM) is used to check the morphology of the prepared samples. Fig. 1a shows the cross-section image of the $TiN/HfO_x/Pt$ memory cell. It reveals the thickness of HfO_x is approximately 8nm, and an interfacial layer (IL) of TiO_xN_y (~ 1 to 2nm) is identified between HfO_x and top electrode (TiN). This may be due to the strong attraction of oxygen ions towards Ti rich region. This interfacial layer formation is further confirmed with EDX spectrum profile as shown in Fig. 1b. The oxygen profile tends to be attracted to the TiN side, indicating that the HfO_x layer in the device possibly becomes oxygen deficient due to the formation of TiO_xN_y. It is believed that this IL layer may serve as oxygen reservoir during the resistive switching.

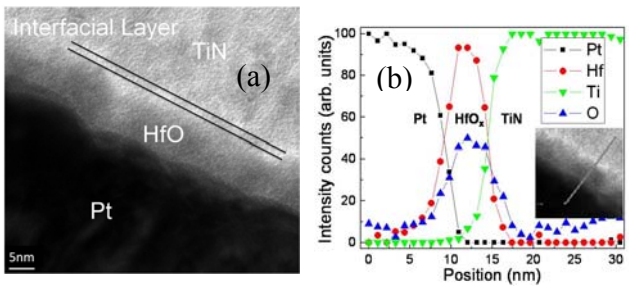

Fig. 1 Physical characterization of HfO_x based MIM capacitor (a) Cross-sectional TEM image of the $TiN/HfO_x/Pt$ memory. (b) EDX study of elemental spatial profile. Inset shows the direction of profile.

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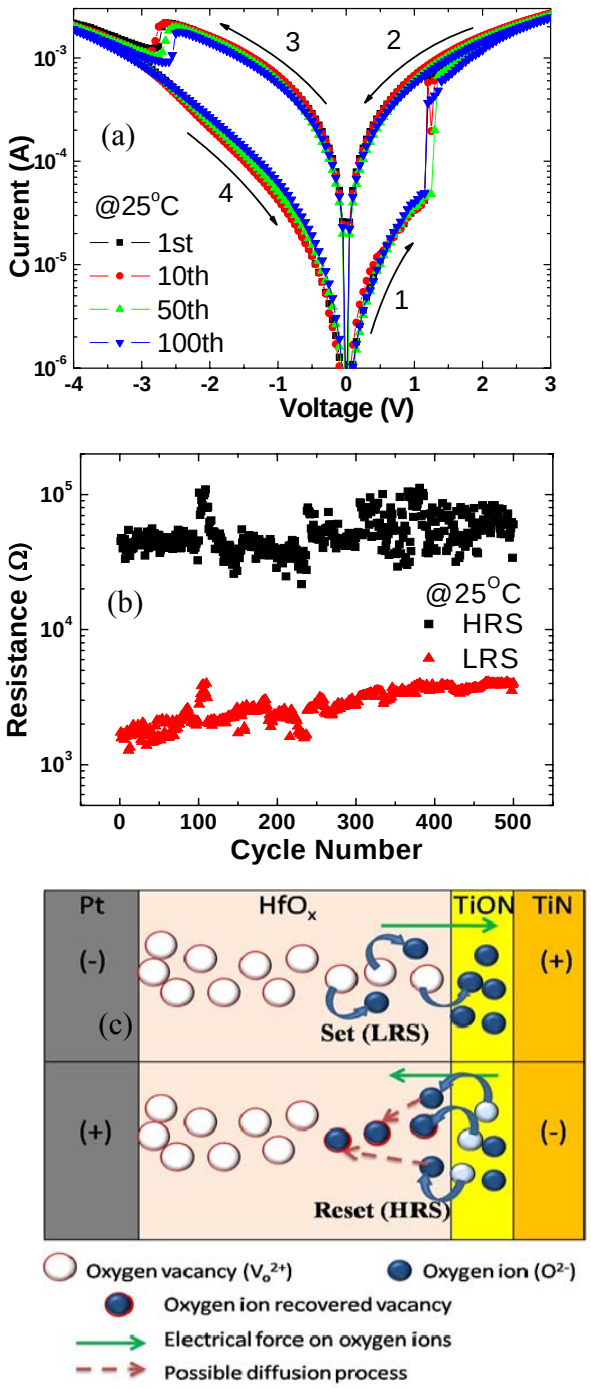

Fig. 2 Resistive switching behaviors at room temperature. (a) The switching characteristics of 100 repetitive DC sweeping current-voltage curves (b) Switching endurance of 500 cycles in DC sweeping mode (c) The schematics of set and reset processes.

Polarity dependent bipolar resistive switching phenomenon is observed in the fabricated RRAM cells. Fig. 2a shows the current-voltage (I-V) characteristics of 100 repetitive DC sweeps after forming at room temperature. The current increases suddenly at the set voltage (V_{set}) of ~ +1.4V during positive sweep, which turns it on from high resistance state (HRS) to low resistance state (LRS). The LRS keeps till with a negative voltage sweep to the reset voltage (V_{reset}) of ~ –2.5V, and HRS will resume. Fig.2b demonstrates good endurance of the fabricated HfO_x RRAM devices up to 500 cycles. The resistive switching phenomenon can be well explained by formation and rupture of oxygen vacancies related conduction filaments, as schematically depicted in Fig.2c [6].

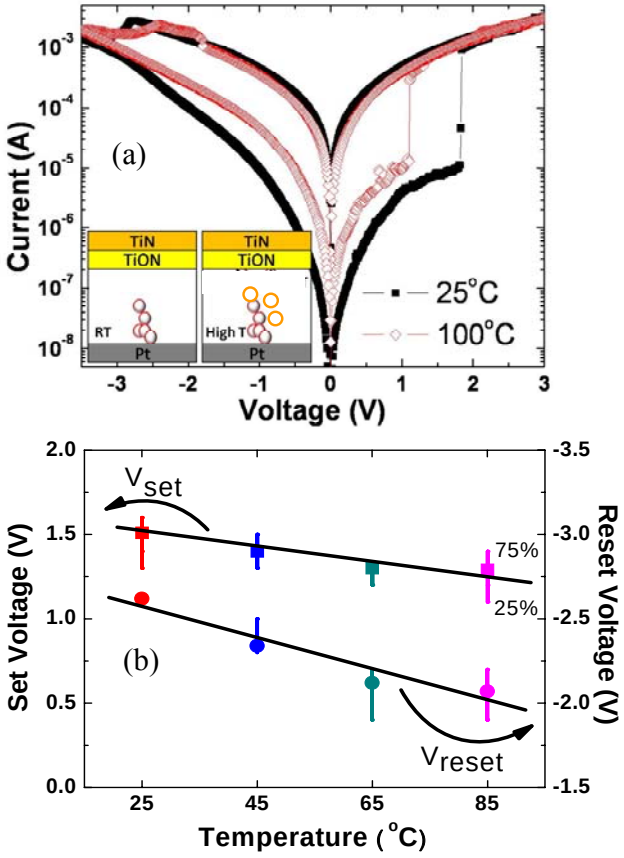

Fig.3 (a) Comparison of DC resistive switching at both 25°C and 100°C. (Inset shows schematic of high temperature HRS leakage current (TAT) increasing). (b) Set (V_{set}) and reset (V_{reset}) voltages decrease with increasing temperature

To better understand the resistive switching behavior in the TiN/HfO_x/Pt device. Resistive switching at room temperature and high temperature (100°C) is compared in Fig. 3a. It is clearly observed the HRS current increases under both polarities with temperature, which can be explained by the schematics as inset of this figure. When device is reset to HRS, the conduction filament is believed to be broken near metal interface, cutting off the current. According to crystal defect theory [7], the probability (p) of oxygen ions to overcome the potential barrier and create vacancies can be expressed as

$$p \approx \nu \exp(-E / k_B T) \quad (1)$$

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where E is the potential barrier height, T is temperature. Thus with the increase of temperature, the probability of defects formation increases. The increased V_o–related traps inside the dielectrics would thus increase the trap-assist tunneling (TAT) leakage. Consequently, a smaller On/Off ratio would also be observed. Further to the above, in Fig.3b, V_{set} / V_{reset} decrease with increasing temperature, which is correlated with the increased oxygen ion mobility [8], in addition to effectively lowered potential barrier according to Eq. (1). at high temperature.

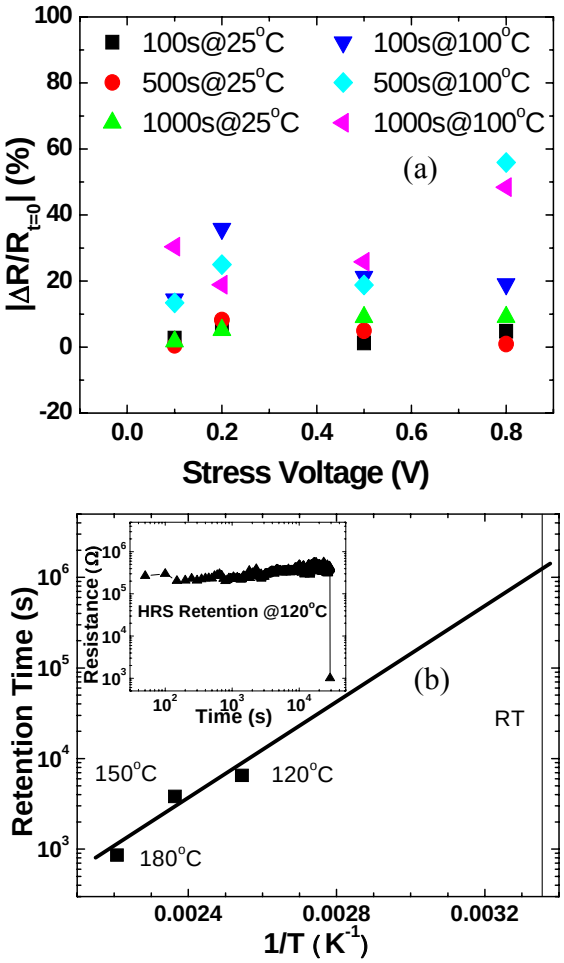

Fig. 4 (a) Resistance variation ($|\Delta R/R_{t=0}|$) of HRS at different stress conditions and temperatures (b) Measured HRS retention time as a function of temperature, inset shows the HRS retention at 120°C, and retention time is defined at the point where resistance suddenly drops.

Electrical stress of 0.1V to 0.8V at both room temperature and high temperature on the reliability of RRAM devices is studied in Fig. 4a. The HRS resistance variation after stress of different period ($|\Delta R/R_{t=0}|$, where $R_{t=0}$ stands for the resistance prior to stressing) is used to evaluate the degradation of RRAM retention. It can be found that the variation at room temperature is much smaller compared to high temperature case for all the stressing conditions. The resistance variation at high temperature is less than 60% and is almost independent of stressing condition. This variation will not degrade the reliability (retention) of RRAM. The possible reason is due to the small stressing voltage (which must be smaller than V_{set}) and short stressing time. And in Fig. 4b, the room temperature HRS retention is projected from Arrhenius plot with high temperature measurements. Each data point is the logarithm average of ten measurement results and the inset of Fig. 4b shows the definition of the retention time.

IV. Conclusion

In conclusion, HfO_x based RRAM shows good resistive switching behavior and its temperature instability is investigated in details in this work. The temperature dependent properties pose a challenge to the commercialization of binary oxide based RRAM devices, and material-oriented solutions might be the way to address these problems.

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