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Phase Jitter Transfer in High Speed Data Links

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***Abstract*—**Phase locked loops in 10 Gb/s and faster data links are low phase noise devices. Characterization of their phase jitter transfer functions is difficult because the intrinsic noise of the PLLs is comparable to the phase noise of the reference clock signal. The problem is solved by using a linear model to account for the intrinsic noise. This study also introduces a novel technique for measuring the transfer function. It involves the use of the reference clock as a source of wideband excitation, in contrast to the commonly used sinusoidal excitations at discrete frequencies. The data reported here include the intrinsic noise of a PLL for 10 Gb/s links and the jitter transfer function of a PLL for 12.8 Gb/s links. The measured transfer function suggests that the PLL responded like a second order linear system to a low noise reference clock.

***Keywords*—**Intrinsic phase noise, jitter in data link, PLL jitter transfer function, high speed clocking in electronic circuit

I. Introduction

HIGH speed, data links running at 16 Gb/s in parallel can provide terabyte memory bandwidth for high performance computing [1]. After accounting for the appropriate bit error rate for the data link, the random jitters of the link components need to be less than one picosecond in order for the link to achieve sufficiently large data opening for sampling [2, 3, 4].

Figure 1 is a generic model of jitter propagation typical of data links in high performance systems. The phase locked loops (PLLs) in the transmitting (Tx) and receiving (Rx) devices, and the reference clock chip are primary sources of the random jitters in the received data stream. Since these PLLs are designed to operate with a low jitter reference timing signal, the output signal can be dominated by the PLLs' intrinsic noise, namely, N_{TX} and N_{RX}.

Reported in this paper is a novel approach for characterizing low jitter PLLs for data links faster than 10 Gb/s. The approach is based on a linear system model to account for the intrinsic noise. The model allows an algebraic separation of the intrinsic noise and the amplified reference clock noise, thus in a form convenient for the processing of phase noise data to determine the phase jitter transfer function and intrinsic noise of a PLL.

II. Clock Jitter Reduction

The phase jitter transfer functions of the Tx PLL and Rx PLL in a data link determine the degree of phase jitter reduction in the reference clock signal. Figure 1 is a generic model representing the essential elements in the propagation of clock jitters. Even though the transmitting and receiving devices are in compliant with the link specification, they are often from different manufacturers designed using different techniques. Therefore, their bandwidths are within the frequency range in the specification of the links but different from one another.

The generic model has a built-in reduction mechanism for the reference clock noise. The reference timing signal carries jitters from the clock source along the data and reference clock (RefClk) paths. The Tx PLL and Rx PLL are low pass filters with different bandwidths, reducing the high frequency jitter components in the clock signal to different extents. Thus the remaining low frequency jitters from the two paths are not the same. They are cancelled partly in the receiving device after the Rx PLL. The residual clock noise remains in the received data. Also appearing in the data is the intrinsic noise of both PLLs. References 5 and 6 have already described the characterization of the band pass filtering effect in a 5 Gb/s and a 16 Gb/s data links.

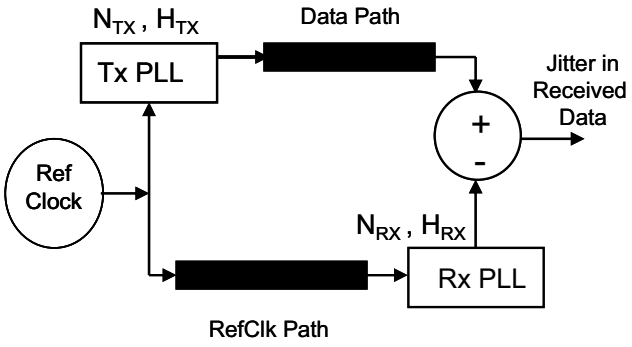

Fig. 1 Generic model of jitter propagation commonly found in high speed data link architecture.

III. Intrinsic Phase Noise

The intrinsic phase noise of a PLL must be accounted for in order to characterize its phase jitter transfer function accurately. The data in Figure 2 are the phase noise profiles output by a PLL for three different RefClk noise levels. When a nominal RefClk is used, the PLL output exhibits its characteristic peaking behavior. As the noise of the RefClk decreases, the output becomes dominated by the intrinsic phase noise of the PLL. When the jitter of RefClk is below a certain level, the effect of peaking is masked out completely.

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Therefore, the intrinsic phase noise can be measured when the RefClk has very low phase noise. Figure 3 shows the intrinsic phase noise associated with the random jitter of a 5 GHz PLL. The data exhibits a 10 dB/decade slope on the left and -20 on the right. The deterministic jitter components are separated and not shown.

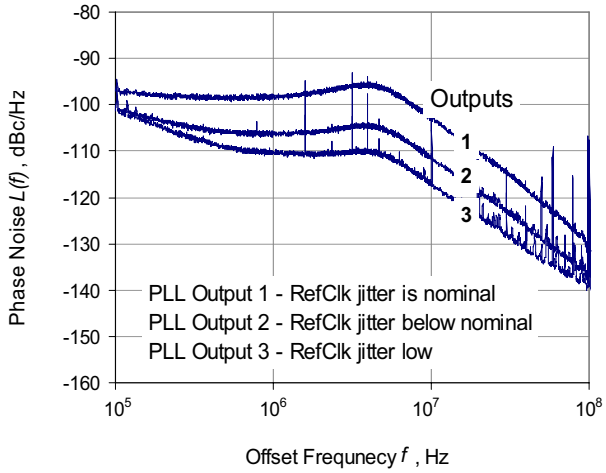

Fig. 2 Peaking becomes dominated by the intrinsic phase noise of the PLL as RefClk jitter decreases.

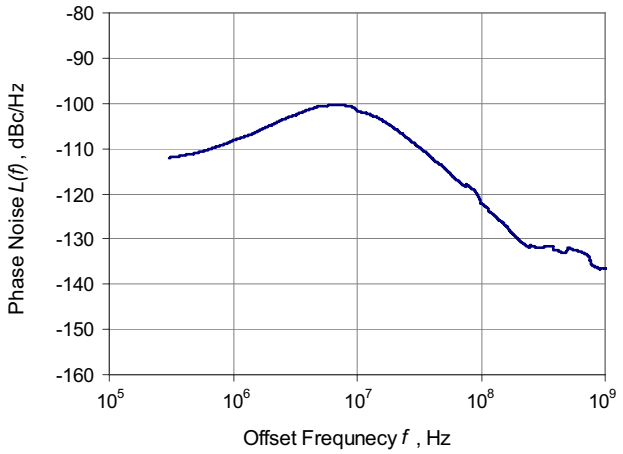

Fig. 3 Intrinsic random phase noise of a 5 GHz PLL (deterministic jitter components are removed).

IV. A Linear Model with Intrinsic Noise

In this study a linear model which accounts for the intrinsic noise of a PLL is used to analyze the phase jitter transfer function of the PLL.

The phase noise of PLL output Y at the offset frequency *f* is represented by

$$Y(f) = X(f)\,H(f) + N(f) \quad (1)$$

where X is the phase noise of the input clock (RefClk), and N is the intrinsic phase noise of the PLL. Equation (1) is in the spectral power density domain and its unit is dBc/Hz.

Figure 4 shows two phase noise profiles of the 6.4 GHz outputs of a PLL in a test chip for a 12.8 Gb/s data link. The frequency of the RefClk is 400 MHz. When the jitter of the RefClk is low, the intrinsic noise of the PLL is significantly larger than the amplified input phase noise, i.e. Y ~ N. For a RefClk with nominal jitter, the frequency multiplication also amplifies the input phase noise by the same ratio, 24 dB. The resulting phase noise is high enough to mask out the intrinsic noise of the PLL, i.e. Y ~ XH. These measurements show that Equation (1) is an adequate approximation of the jitter transfer for PLLs that requires low phase noise reference clock in high speed data links.

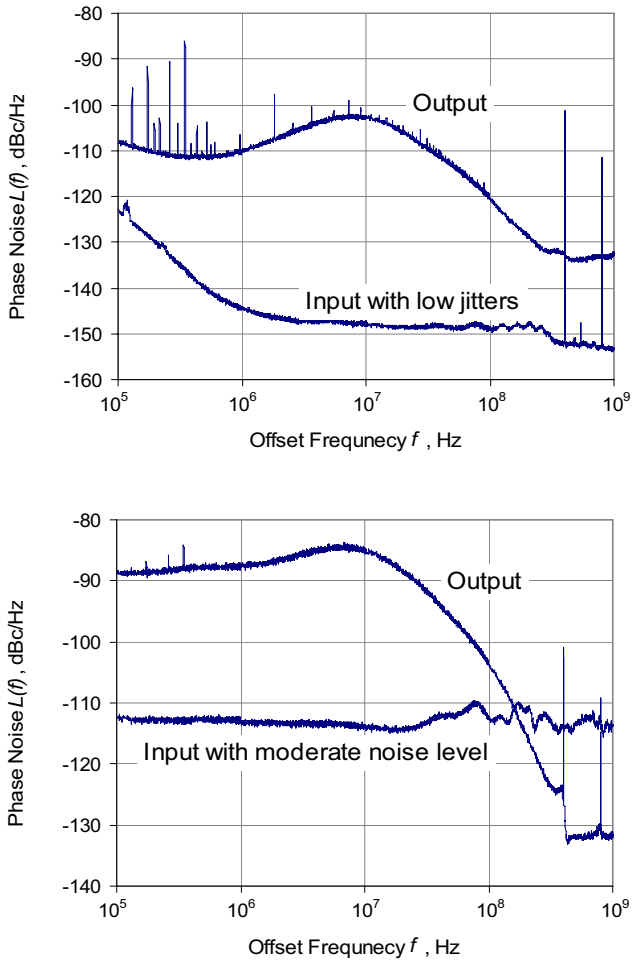

Fig. 4 Variations in output phase noise with low and moderate levels of input jitters.

V. Jitter Transfer Function

Given two inputs of the same frequency but different in jitter levels, namely X_1 and X_2, the corresponding outputs can be written as

$$Y_1(f) = X_1(f)\,H(f) + N(f) \quad (2)$$

$$Y_2(f) = X_2(f)\,H(f) + N(f) \quad (3)$$

The jitter transfer function can be determined by

$$H(f) = \frac{Y_2(f) - Y_1(f)}{X_2(f) - X_1(f)} \quad (4)$$

where X_1 and X_2 cannot be too small for Y ~ N to be true.

VI. Transfer Function Characterization

Figures 5 and 6 show the phase noise profiles of two 400 MHz inputs and the corresponding PLL outputs at 6.4 GHz. The data points were collected using an instrument for measuring phase noise. Each profile has a few thousands data points over the indicated range of offset frequency. Based on the definition of phase noise, the data are valid up to the offset frequency equal to one half of the carrier frequency. Since the input carrier, RefClk, is 400 MHz, the jitter transfer function determined from the data is valid up to 200 MHz.

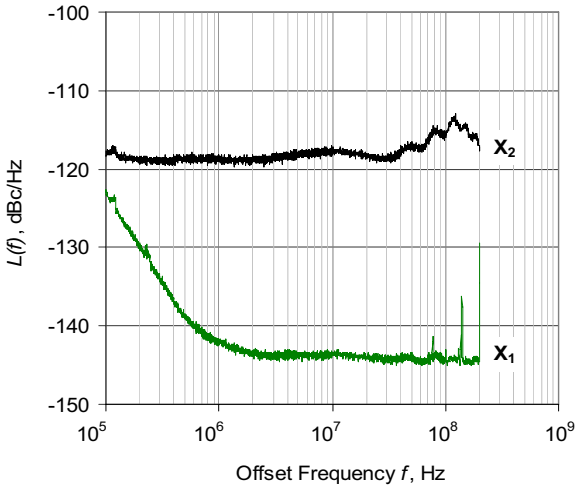

Fig. 5 Two phase noise profiles for different levels of input clock jitter.

The jitter transfer function determined using Equation (4) is shown in Fig. 7. The -3dB point of the PLL is at 40 MHz. The decay of the transfer function matches the rate of a second order linear model, i.e. -20 dB per decade.

VII. Comparison with Sinusoidal Excitation

Equation (4) can also be used to determine the transfer function when the RefClk is modulated by a sinusoidal signal. This commonly used technique can characterize the PLL at one discrete frequency at a time.

Contrarily the present approach requires only four measurements to determine the jitter transfer function over a range of frequency by introducing excitations simultaneously at different frequencies. Each phase noise measurement captures a profile of the jitter components. Two RefClks of different phase noise levels are used. The profile of the excitations includes the difference in the phase noise at each frequency. Accordingly the response of the PLL is the difference in the two corresponding output noise profiles. Based on Equation (4), four phase noise measurements can

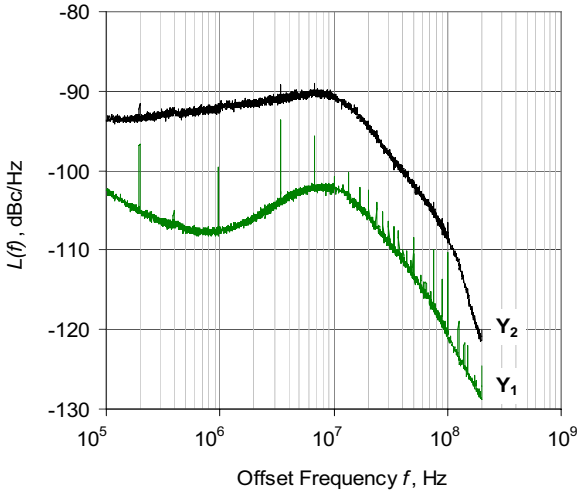

Fig. 6 PLL outputs at 6.4 GHz for the two levels of jitters carried by the input clock.

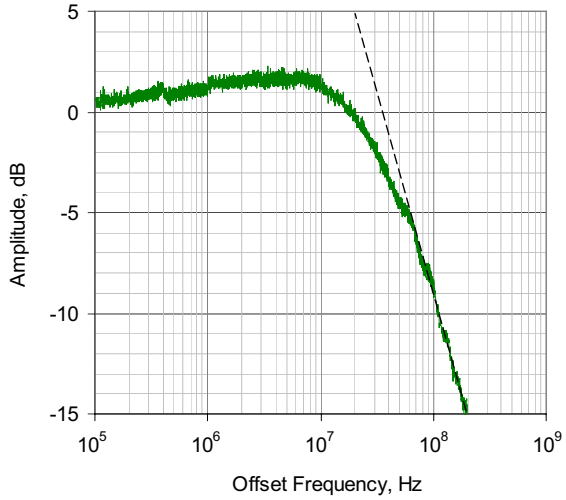

Fig. 7 Jitter transfer function of a 6.4 GHz PLL. Dotted line indicates the 20 dB/decade decay rate typical of a second order linear model.

collect sufficient data to determine the jitter transfer function over a selected offset frequency range.

A reference clock, instead of a sinusoidal, signal is normally the input of a PLL and its jitter is wideband. The output of the PLL contains the responses to the simultaneous modulation by all the jitter components in the RefClk signal. The jitter transfer characteristic determined by a sinusoidal modulation cannot capture the simultaneous phase modulations at the adjacent frequencies. Therefore clock sources with nominal jitter levels can introduce the more realistic wideband excitation encountered by a PLL.

VIII. Conclusion

This study has shown that a linear model with an intrinsic noise term is adequate for describing the phase jitter transfer characteristic of low noise PLLs for high speed data links. Measurement of the intrinsic noise of a PLL requires a very low noise RefClk source. The paper has also introduced a novel approach for determining the phase jitter transfer function of a PLL. It uses a clock with jitter near the nominal operating conditions as a source for wideband excitation. The results show that the PLLs in this study have the characteristics of a second order linear system.

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