World Academy of Science, Engineering and Technology
International Journal of Electronics and Communication Engineering
Vol:1, No:9, 2007

Design Optimization Methodology of CMOS Active Mixers for Multi-Standard Receivers

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***Abstract*—**A design flow of multi-standard down-conversion CMOS mixers for three modern standards: Global System Mobile, Digital Enhanced Cordless Telephone and Universal Mobile Telecommunication Systems is presented. Three active mixer's structures are studied. The first is based on the Gilbert cell which gives a tolerable noise figure and linearity with a low conversion gain. The second and third structures use the current bleeding and charge injection techniques in order to increase the conversion gain. An improvement of about 2 dB of the conversion gain is achieved without a considerable degradation of the other characteristics. The models used for noise figure, conversion gain and IIP3 used are studied. This study describes the nature of trade-offs inherent in such structures and gives insights that help in identifying which structure is better for given conditions.

***Keywords*—**Active mixer, Radio-frequency transceiver, Multi-standard front end, Gilbert cell, current bleeding, charge injection.

I. Introduction

THE explosive growth in the wireless communications market, over the past ten years, has led to consumer demand for low-cost, optical infrastructures, high data rate communications and low-power transceivers , [1], [2]. To explain such a growth, GaAs, that used to be the substrate of choice for RF functions, has been challenged by Bipolar and BiCMOS processes. But none of these processes has the cost of CMOS structure. That's why CMOS RF circuits have naturally become the target of many RF designers. For set makers it is very useful to have cost effective front-end solutions that can be applied in communication systems for different standards at a time [3].

The down conversion mixer is one of the most important building blocks for RF transceivers in wireless communications. Modern wireless communication standards such as Global System Mobile (GSM), Digital Enhanced Cordless Telephone (DECT) and Universal Mobile Telecommunication System (UMTS) demand high performance RF front ends. These are very often constrained by the achievable conversion gain, noise figure and linearity of the low noise amplifier and down-conversion mixers.

This paper presents a design flow of CMOS mixers suitable for single-chip 0.35µm AMS CMOS multi-standard receivers. This design flow consist of using models of noise figure, conversion gain and linearity of the conventional doubly-balanced mixer to enhance its performances using circuit techniques like current-bleeding and charge injection.

These mixers are used to down-convert the RF signal after the low-noise amplifier (LNA) to the desired intermediate frequency (IF). The required specifications for the standards of concern; the GSM, DECT and UMTS are: a noise figure NF < 10dB, a third-order interception point IIP3> 0 dBm, a power conversion gain CG >12 dBm and a maximum power consumption of 30 mW for the operational frequencies: 960 MHz (GSM), 1.9 GHz (DECT) and 2.1 GHz (UMTS).

II. The Doubly-Balanced Mixer (1ST STR)

Fig. 1 shows a CMOS doubly-balanced mixer based on the Gilbert cell [3]. It consists of an RF amplification stage with an LO switching quad stacked. For such mixers, the input is required to match 50 Ohms for all the standard frequencies (960, 1.9 GHz, 2.1 GHz). This can be done either selectively at each frequency [5] or over a band covering all frequencies. The latter approach is used here because it requires less complex matching networks [6]. Then, the following methodology can be followed to have an optimized circuit:

1) First, we start by ensuring the saturation regime of all Gilbert cell transistors.
2) Then, we develop models for performance characteristics like noise figure, conversion gain and linearity (IIP3) in order to estimate optimum transistors sizing and biasing.
3) Finally, based on the models developed, key parameters (e.g. bias current, transistors sizes, and load resistance) can be identified and optimized for a good performance. Since, input transistor sizing affects matching condition, the matching network should be readjusted.

A. Ensuring the saturation mode of Gilbert cell transistors

The main objective of this step is to determine parameters allowing the saturated mode of the transistors. This can be theoretically done by imposing a constant drain current (bias current) using an ideal bias current source, as shown in Fig. 1 (denominated here as 1st STR). Accordingly and under an appropriate supply voltage, the gate-source voltages of $M_{1\text{-}6}$ will be automatically adjusted to satisfy the saturation condition.

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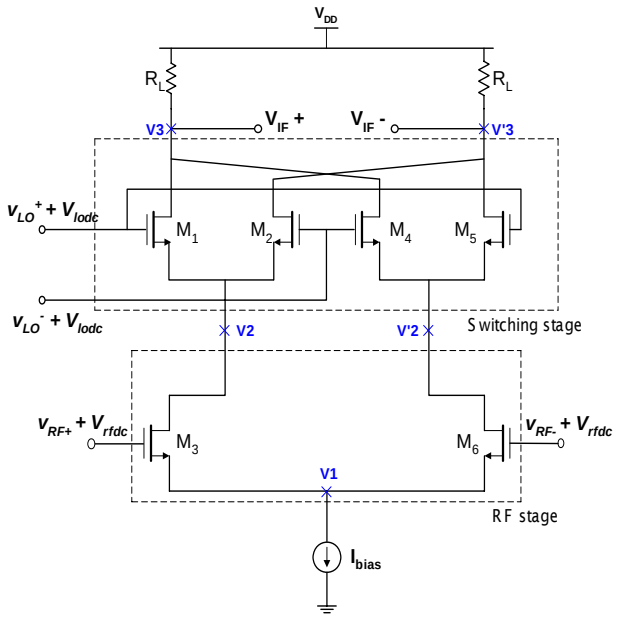

Fig. 1 simplified doubly-balanced mixer based on the Gilbert cell (1st STR)

Practically, the bias current is that of a MOS current mirror.

Looking at Fig. 1, for a given bias current the bias voltage V1 is determined by the DC voltage V_{rfdc} and the aspect ratio (W/L) of the RF port transistors M_3 and M_6 as

$$V1=V_{rfdc}-V_{GS3} \quad (1)$$

Similarly, the bias voltage V2 is defined by the DC voltage V_{lodc} and the aspect ratio of the switching port transistors M_1, M_2, M_4 and M_5 by

$$V2=V_{lodc}-V_{GS1} \quad (2)$$

Also the bias voltage V3 is determined by the resistor load R_L, the supply voltage V_{DD} and the bias current, assuming matched pairs, as

$$V3= V_{DD} - (I_{bias}/2)*R_L \quad (3)$$

It follows that the drain-source voltages of all FETs are determined by V1, V2 and V3. As a consequence, for a given supply voltage V_{DD} and bias current I_{bias}, the saturation mode of the mixer FETs is obtained by adjusting V_{rfdc}, V_{lodc}, R_L and the aspect ratios of transistors M_{1-6}.

B. Noise figure model

Any communication system is affected by external and internal noises which limit its performance. To design and predict communication system performances, it is imperative to control effectively all noise sources. A theoretical analysis undertaken by Terrovitis and Meyer [7] gives an approximate model for the noise figure of CMOS Gilbert cell-based mixers. The time-varying power spectral density of noise generated in the RF stage (M3 and M6) is:

$$S^0_{nRF} = \alpha.4kT.(Rs + 2.rg_3 + \frac{2\gamma}{g_{m3}}).g^2_{m3}, \quad (4)$$

where T is the absolute temperature, coefficient α is equal to 1 for a square LO wave, Rs is the input source resistance which drives the mixer RF port, g_{m3} is the instantaneous small-signal transconductance of M_3 and M_6, rg_3 is their polysilicon gate resistance, and coefficient γ is equal to 2/3 for long channel transistors and need to be replaced with a larger value for submicron MOSFETs [8].

The time-average output noise power spectral density generated in the switching pair is given by

$$S^0_{nSWITCH}(f) = 4kT.\gamma\left(\frac{1}{T_{LO}}\int_0^{T_{LO}} G(t).dt\right) = 4kT.\gamma.\overline{G}, \quad (5)$$

where $\overline{G}$ is the time average of $G(t) = 2\frac{g_{m1}.g_{m2}}{g_{m1}+g_{m2}}$., the small-signal transconductance of the differential pair.

The time-average power spectral density of noise from the LO port is defined as

$$S^0_{nLO}(f) = 4kT(4r_{g1})\overline{G^2}. \quad (6)$$

Having calculated the noise contribution from the various sources to the output, the mixer noise figure can be estimated. Consider that the load introduces output noise which can be represented by an equivalent noise resistance R_L. The time-average power spectral density of the mixer total output noise is

$$S^0_{nMIXER}(f) = S^0_{nRF}(f) + S^0_{nSWITCH}(f) + S^0_{nLO}(f) + 4KT\left(\frac{1}{R_L}\right). \quad (7)$$

The time-average power spectral density of the mixer input noise is

$$S^0_{IN}(f) = 4kT.R_S.(c.g_{m3})^2, \quad (8)$$

where "***c***" represents the conversion gain of the switching pair alone. So, the single sideband (SSB) noise figure of a Gilbert cell type mixer is:

$$NF_{(SSB)} = 10.LOG\left[\frac{S^0_{nMIXER}(f)}{S^0_{IN}(f)}\right] = 10.LOG\left[\frac{\alpha}{c^2} + \frac{2(\gamma_3 + rg_3.g_{m3})\alpha.g_{m3} + \gamma_1\overline{G} + (4r_{g1})\overline{G^2} + \left(\frac{1}{R_L}\right)}{R_S.c^2(g_{m3})^2}\right]. \quad (9)$$

The model described in (9) can be used to optimize the size of the Gilbert cell transistors. The parameters r_{g1}, r_{g3}, g_{m3}, $\overline{G}$ *and* $\overline{G^2}$ depend on the aspect ratio (W/L) of the transistors as well as the bias current I_{bias}. Here, the length L is fixed at the minimal value of 0.35µm in order to allow maximum operating frequencies.

To identify key parameters determining the noise performance of the circuit, two steps are needed:

1) In the first step, we assume that all the transistors of the RF and LO ports have the same width W. Then, we draw the noise figure as a function of the parameters W and I_{bias}. We obtain the curve shown in Fig. 2, where we perceive that to reduce the noise figure, we must increase I_{bias} and W. Then, according to the required specifications (e.g. maximum tolerable power consumption and supply voltage), the highest value of bias current can be defined. For example, for a minimal noise figure, the maximum current is $I_{bias}=P_{max}/V_{DD}$=10mA (P_{max} and V_{DD} taken equal to 30mW and 3V, respectively).

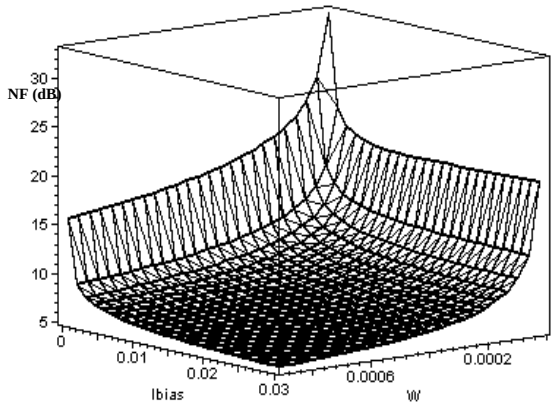

Fig. 2 noise figure variation as a function of the channel width W and bias current I_{bias}

2) In the second step, we study the dependence of noise figure on widths of the switching stage (W1) and RF stage (W3). We obtain the curve shown in Fig. 3 when I_{bias} =10mA. The noise figure decreases when W1 and W3 increase. This is much more pronounced for W3 than W1. Indeed, when W3 varies from 50 µm to 900 µm the noise figure falls steeply from 14 dB to 6.5 dB, whereas a variation of W1 from 10 µm to 500µm results in 0.7dB decrease only. Therefore, the noise figure can be reduced by increasing the total bias current of the circuit or/and by increasing the aspect ratio of the RF and the switching devices.

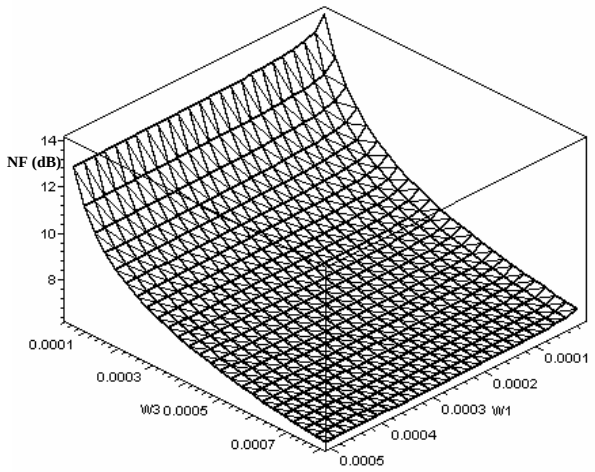

Fig. 3 noise figure's variation as a function of the transistor's channel width of the Gilbert cell (W1 & W3) for I_{bias}=10mA

C. Conversion gain model

The total conversion gain is the product of the RF-IF switching stage gain "A_{switch}" and the RF pair gain "A_{VRF}". [9] The conversion gain A_{switch} of the RF-IF switching stage can be approximated by

$$A_{switch} = \frac{2}{\pi}\left[g_{m1}.(r_{ds1} \,//\, R_L)\right], \tag{10}$$

where r_{ds1} and g_{m1} are the drain-source resistance and the transconductance of the LO transistors, respectively, and R_L is the load of the switching pair.

On the other hand, the switching transistors present loading impedance approximately equal to $1/g_{m1}$ to the RF pairs. Then, the voltage gain A_{VRF} of the RF pair is given by

$$A_{VRF} = -g_{m3}.\left(\frac{1}{g_{m1}}\right), \tag{11}$$

were g_{m3} is the transconductance of the RF pair transistors.

Therefore, the total mixer voltage gain (CG) can be approximated by

$$CG = A_{VRF} \times A_{switch} = -\frac{2}{\pi} g_{m3}.(r_{ds1} \,//\, R_L). \tag{12}$$

Fig. 4 shows the variation of the voltage gain as a function of W1 and W3. It's obvious that a higher conversion gain is obtained for a combination of wide RF transistors (M_3, M_6) and narrow LO transistors (M1, M2, M4 and M5).

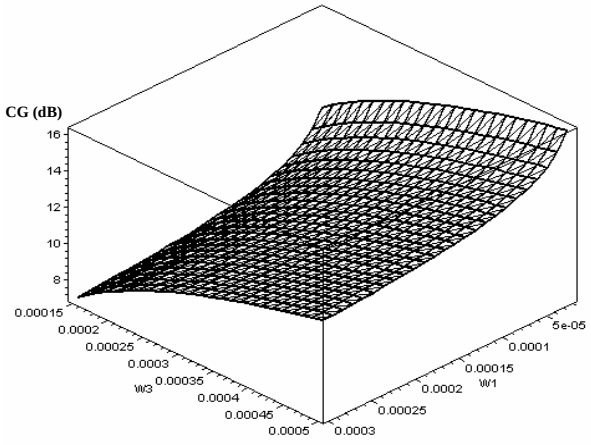

Fig. 4 gain variation as a function of to the transistor channel width of the RF and LO ports

D. Third- order interception point model

As described in [10] and [11], the *IIP3* of a Gilbert cell mixer can be approximated by

$$IIP3 = 4\sqrt{\frac{2}{3}}\left(V_{gsRF} - V_t\right) \quad (13)$$

A higher *IIP3* is then obtained for a high overdrive voltage (V_{gsRF}–V_t) of RF devices.

E. Optimization and simulation results

The optimisation methodology is based on the developed models for noise, gain and linearity. For a fixed bias current, a high conversion gain and low noise figure would require high values of g_{m3}, that is wider RF transistors, as evidenced in (9) and (12). However, this would reduce their overdrive voltage and hence degrade the mixer *IIP3* (see (13)). Also, wide RF pairs degrade the high-frequency response of the RF stage. Alternatively, both gain and linearity improve if the bias current increases. This would, however, result in higher power consumption.

On the other hand, the switching pair transistors should be made narrow in order to achieve higher gains without a considerable degradation of noise figure. Therefore, we need to optimize all the above trade-offs inherent in such systems.

After cycles of DC and RF optimization, the following values were obtained:

- Bias current = 6mA under 3 V supply voltage
- For the RF stag e: W3= 800 µm
- For the switching stage : W1= 400 µm
- R_L= 400 Ω.

Fig. 5 shows the simulated power conversion gain and *IIP3* over a band covering the three standard frequencies for an intermediate frequency f_{IF} = 45 MHz. A 3 V supply voltage and 6 mA biasing current I_{bias} were applied (i.e. power=18 mW).

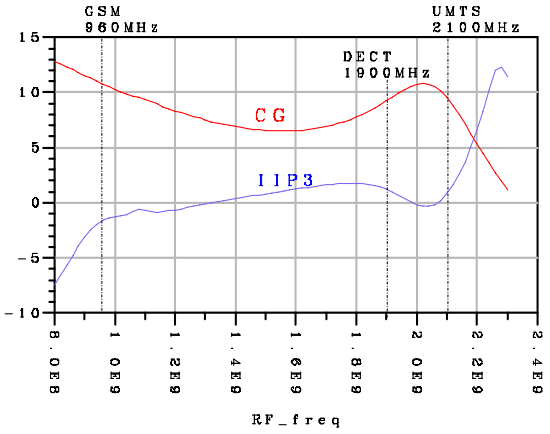

Fig.5 simulated conversion gain and IIP3 of the doubly-balanced mixer

Table I summarizes the simulated results obtained for the three standard frequencies.

TABLE I
SIMULATION RESULTS OF THE DOUBLY-BALANCED MIXER

Standard	GSM	DECT	UMTS
Frequency Operation (MHz)	960	1900	2100
CG (dBm)	10.7	9.2	9.5
CP1 (dBm)	-12.5	-8	-10.5
NF (dB)	9.3	9.4	9.9
IIP3 (dBm)	-1.6	1.2	0.8
Power consumption	18 mW (3V, 6mA)		
Process	0.35 µm CMOS		

It shows that the Gilbert-cell doubly-balanced mixer structure gives acceptable levels of noise and linearity but a conversion gain lower than that the minimum value required by the standards specifications (i.e. 12 dBm).

In the following section, techniques allowing an improvement of the conversion gain without affecting the linearity will be studied.

III. Doubly -Balanced Mixer With Current-Bleeding Technique (2ND STR)

This structure is an enhancement of the preceding one. The target is to improve the conversion gain without a significant degradation of linearity.

A. Structure alternative

The disadvantage of the preceding structure is its low conversion gain. Its conversion gain in (12) can be approximated by

$$CG = -\frac{2}{\pi} g_{mRF} R_L, \quad (14)$$

were g_{mRF} is the RF port transconductance (g_{mRF}= g_{m3}).

Since the RF devices operate in the saturation region, (14) and (13) can be replaced, respectively, by

$$CG \approx \frac{2}{\pi} R_L \sqrt{K_n I_{bias}} \quad (15)$$

$$IIP3 \approx 4\sqrt{\frac{2}{3}\frac{I_{bias}}{K_n}} \quad (16)$$

where $K_n = \mu_n C_{ox} \frac{W}{L}$.

The *IIP3* and the conversion gain are then proportional to the square root of the bias current. It follows that the mixer linearity and gain can simultaneously improve by simply increasing the bias current. Practically, this hypothesis is not exact. The increase of the bias current will automatically increase the voltage-drop across R_L, which affects the bias conditions of the switching transistors. Therefore, for a fixed

V_{DD}, R_L must decrease to preserve these bias conditions. According to (15), this will decrease the conversion gain. Furthermore, the increase of the bias current results in higher power consumption. One may therefore deduce that to improve both gain and linearity, we should increase the RF stage bias current (I_{bias}) without varying the bias current of the switching pair. This can be achieved using the charge injection or current-bleeding techniques [11], [12].

The bleeding technique can be explained more clearly using a single-balanced mixer. Fig. 6 shows a single-balanced mixer in which a bleeding current source (I_{BLD}) is added. Without this current source, the total bias current is $I_{bias} = I_{D1} + I_{D2}$. With the bleeding current source and without changing I_{D1} or I_{D2}, I_{bias} increases to $I_{bias} = I_{D1} + I_{D2} + I_{BLD}$.

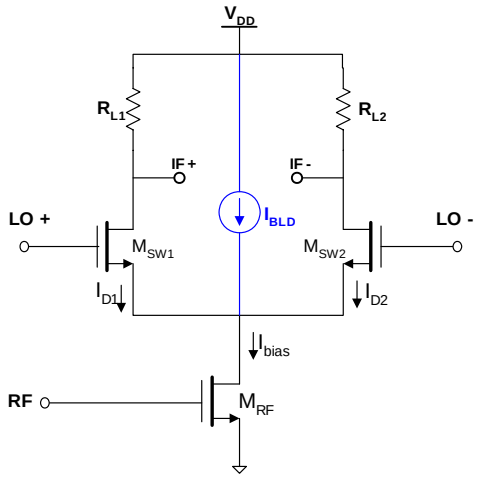

Fig.6 single-balanced mixer with current bleeding source

Therefore, it will be possible to improve linearity and conversion gain at the same time (see (15) and (16)). However, the total power consumption of the circuit would increase.

Alternatively, it is possible to keep constant the total bias current and thus the power consumption. In this case, by adding the bleeding source, I_{D1} and I_{D2} should decrease. Then, the load resistor R_L must increase to not destroy the bias conditions of the switching pair. It follows that the conversion gain will be improved as shown in (15) without improving the *IIP3*.

Fig. 7 shows an implementation of the circuit in Fig. 6 with current-reuse bleeding technique. The p-channel transistor M_{Bld} has a common gate with the RF NMOS transistor. Therefore, M_{Bld} has double function: it plays the role of a current bleeding source as well as be part of the RF stage drive amplifier. The M_{Bld} increases the conversion gain by increasing the total transconductance of the RF stage (M_{RF} + M_{Bld}) from "g_{mRF}" to "g_{mRF} +g_{mBld}", where g_{mBld} is the transconductance of the transistor M_{Bld}. The conversion gain expression is now given as

$$CG = \frac{2}{\pi}(g_{mRF} + g_{mBld})R_L. \qquad (17)$$

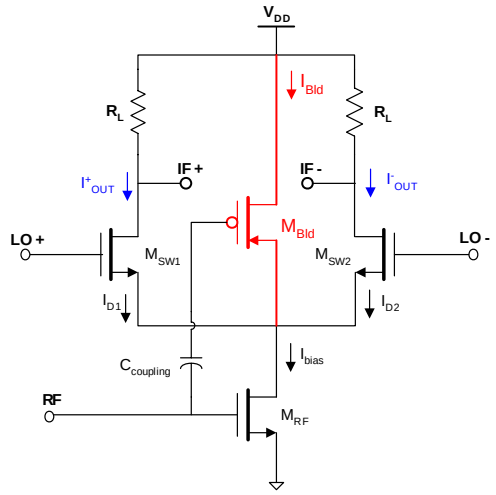

Fig.7 single-balanced mixer with current-reuse bleeding technique

Based on our results, this technique has allowed the improvement of the conversion gain without considerable noise degradation. Nevertheless, the linearity degrades compared to the Gilbert cell. This can be explained by the fact that PMOS transistors introduce some distortion to the circuit [13].

On the other hand, if a wideband input matching is needed, the use of M_{Bld} as a part of the drive amplifier would degrade this matching and hence the circuit performance. For a wide frequency variation, parasitic capacitances of this device can corrupt the input matching and hence deteriorate linearity and gain.

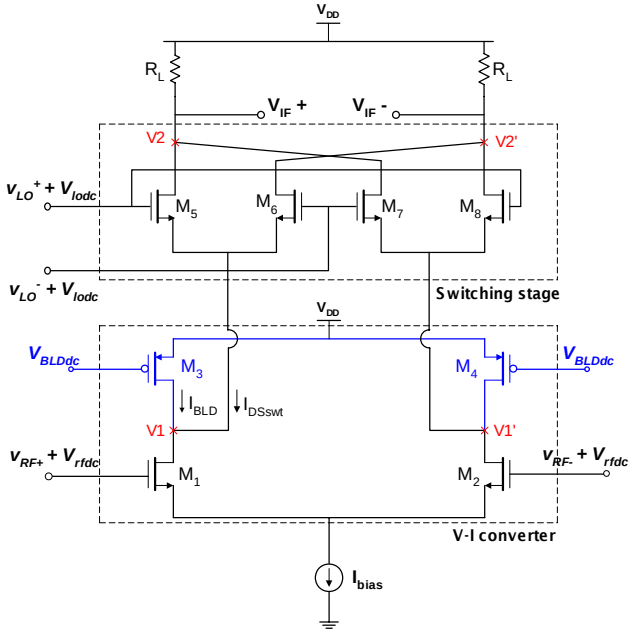

Fig.8 doubly-balanced mixer with current-bleeding technique (2^{nd} STR)

Therefore, this technique is preferred for narrow band applications only (one standard) and not for wideband systems like multi-standard and ultra wideband (UWB) receivers. Otherwise, the PMOS and RF NMOS devices must be independently biased to not affect the wideband input matching.

Fig. 8 shows the basic core of the proposed double-balanced Gilbert-type mixer with bleeding technique (denominated here as 2nd STR). The p-channel transistors M3 and M4 are used only as bleeding current sources.

B. Structure operation and simulation results

In view of the above discussion, there are two approaches to improve performances using this technique. These are summarized below.

1) Increasing the RF pair bias current alone (*1st Apr.*)

We conserve the load R_L and bias current of the switching devices $M_{5\text{-}8}$. Here, this current was set to I_{DSswt} =3 mA. The bleeding sources increase the total bias current without any effect on the switching pairs. If each bleeding source delivers 1 mA, the total bias current will increase from 6 to 8 mA.

Fig. 9 shows the simulated power conversion gain and *IIP3* for an intermediate frequency f_{IF}= 45 MHz over a band covering the GSM, DECT and UMTS standard frequencies, when a 3V supply voltage and 8 mA biasing current I_{bias} are applied. The simulated values for the three standard frequencies are presented in Table II. We note that the conversion gain was boosted by about 2 dB for the three standards. Also, the *IIP3* has also increased for the DECT and UMTS standards. These results confirm the previous theoretical analysis.

With this approach, there were no significant effects on the noise figure compared to the first structure (1st STR). On the Other hand, the power consumption has increased. It is not worthy that adding 1 mA as bleeding-current doubles the total bias current due to the differential topology of the circuit.

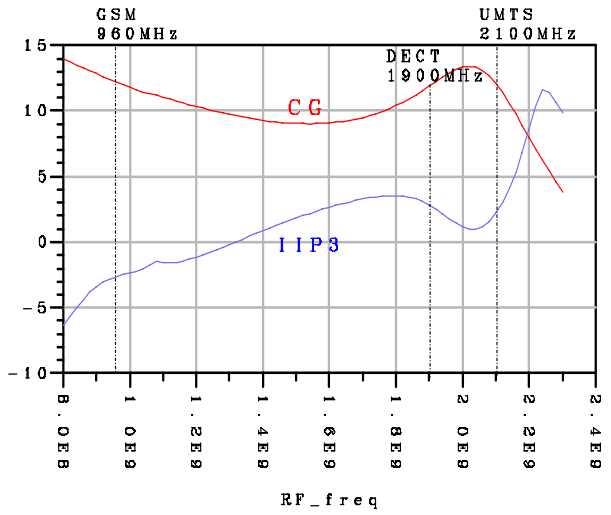

Fig.9 simulated conversion gain and IIP3 of the doubly-balanced mixer with current-bleeding technique (2nd STR)

TABLE II
SIMULATION RESULTS OF THE DOUBLY-BALANCED MIXER WITH CURRENT BLEEDING, 1ST APPROACH

Standard	GSM	DECT	UMTS
Frequency Operation (MHz)	960	1900	2100
CG (dBm)	12.2	11.9	12.1
CP1 (dBm)	-12.5	-9	-10
NF (dB)	9.5	8.9	9.8
IIP3 (dBm)	-2.8	2.8	2.2
Power consumption	24 mW (3V, 8mA)		
Process	0.35 µm CMOS		

A same strategy would lead to less increase in the power consumption when a single balanced topology is used.

2) Increasing the load resistance while maintaining the bias current (*2nd Apr.*)

The bias current is conserved at 6 mA. The aspect ratio and the biasing voltage of the bleeding devices M_3 and M_4 (Fig. 8) are adjusted to make a bleeding current I_{BLD}=1 mA.

In this case, lower DC currents flow through the switching transistors (I_{DSswt} =I_{bias}/2 -I_{BLD} =3-1= 2 mA), which results in a low voltage drop across R_L and a higher bias voltage V2 and V2'. As discussed previously, to maintain these voltages and thus the bias conditions of the switching stage, the resistive load R_L should increase (here from 400 Ω to 550 Ω). This would enable higher gains (see (15)). There should be no effect inflicted on the circuit linearity because I_{bias} is kept constant (see (16)). Simulated values for a 3V-supply voltage, a bias current I_{bias} of 6 mA, a resistive load R_L=550Ω and f_{IF}=45 MHz for the three standards are shown in Table III. The results are as expected except that the noise figure has slightly increased because of the reduction in the bias current of the LO pairs.

TABLE III
SIMULATION RESULTS OF THE DOUBLY-BALANCED MIXER WITH CURRENT BLEEDING, 2ND APPROACH

Standard	GSM	DECT	UMTS
Frequency Operation (MHz)	960	1900	2100
CG (dBm)	11.7	11.8	12
CP1 (dBm)	-12	-9.5	-10.5
NF (dB)	10.1	9.3	10.1
IIP3 (dBm)	-2.3	0.8	-0.3
Power consumption	18 mW (3V, 6mA)		
Process	0.35 µm CMOS		

Summarizing then, the advantage of the 2nd approach is to improve the conversion gain while conserving the same power consumption. Also, it does not improve the circuit linearity as was allowed by the first approach.

C. Minimal supply voltage determination

Another technological parameter that is paramount is the minimal supply voltage required. For the operation of mixer in Fig. 8, this voltage is given by the overdrive voltages of the transistors M1-4. We denote V_{ovd1} and V_{ovd2} as the overdrive voltages of (M1, M2) and (M3, M4) transistors, respectively. These voltages are given, respectively, by $V_{ovd1}=V_{rfdc}-V_t$ and $V_{ovd2}=V_{dd}-V_{BLDdc}-V_t$. Assuming that V_{rfdc} = V_{BLDdc}, one can write

$$V_{DD}=V_{ovd1}+V_{ovd2}+2V_t \tag{18}$$

Knowing the minimal values of V_{ovd1}, V_{ovd2} and V_t, the minimal supply voltage ensuring a good circuit operation can be calculated. This study will be useful when low supply voltage and/or low power consumption is required.

IV. Doubly -Balanced Mixer With Charge Injection Method (3RD STR)

The disadvantage of the second structure is that the minimum supply voltage, needed for a good operation, is limited by the PMOS transistors added for bleeding purposes (M_3 and M_4 in Fig. 8). To overcome this, a new structure using resistive loads instead of PMOS transistors is shown in Fig. 10 (denominated here as 3rd STR).

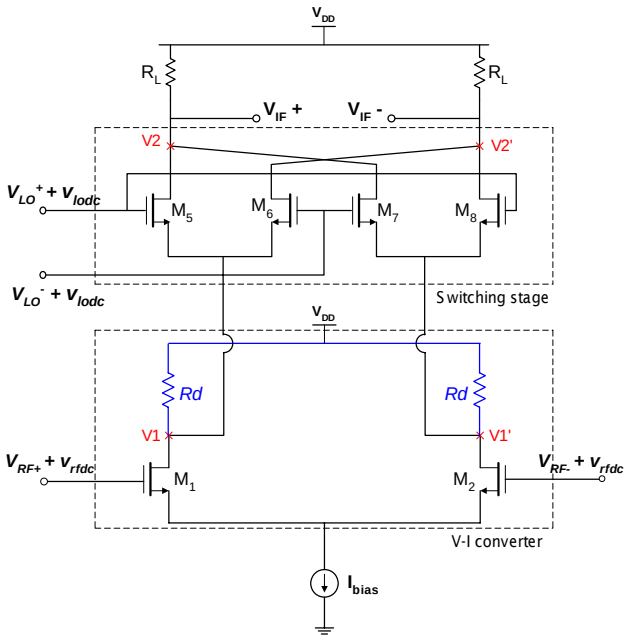

Fig.10 doubly-balanced mixer with charge injection method (3rd STR)

A. Structure operation

The conversion gain of the new structure can be approximated by

$$CG=\frac{2}{\pi}\left(\frac{g_{mRF}R_L}{1+\frac{1}{Rd\,(g_{ms}+g_{msb})}}\right), \tag{19}$$

where g_{mRF} is the transconductance of M1 and M2, g_{ms} and g_{msb} are, respectively, the transconductance and the substrate transconductance of the switching transistors (M5, M6, M7, M8).

To increase the conversion gain, *Rd* should increase. However, this would produce a high drop voltage across *Rd*, which in turn would reduce V1 and hence eventually driving M1 and M2 out of their saturation regime. The noise figure of this structure can be approximated by

$$NF=10\,LOG\left[2+\frac{4\gamma_n}{g_m R_s}+\frac{4}{g_m^{\,2}R_s.R_d}+\frac{2\gamma_n g_{ms}}{\mathrm{Rs}\,g_m^{\,2}R_d^{\,2}(g_{ms}+g_{mbs})^2}+\frac{\pi^2\left(1+\frac{1}{Rd(g_{ms}+g_{mbs})}\right)^2}{2\mathrm{R\,Rs}.g_m^{\,2}}\right]. \tag{20}$$

The thermal noise of *Rd* contributes to the total noise. Here, the noise of the switching transistors affects the total noise figure more critically than in the two preceding approaches (fourth term in (20)). To decrease the noise figure, we need to increase *Rd*. This will also make it possible to increase the conversion gain.

B. Simulation results

For a fair comparison between this structure and the previous ones, we should conserve the same bias conditions for the switching devices.

The first and second approaches applied for the second structure are also adopted here for the third structure. The value of *Rd* is set to 2 kΩ in order to allow a bleeding current I_{BLD}=1mA (as in the second structure). This value is determined by

$$Rd=\frac{V_{DD}-V1}{I_{BLD}} \tag{21}$$

1) Increasing the RF pair bias current alone (*1st Apr.*)

The bleeding current is used to increase the total bias current of the circuit from 6 to 8 mA. The resistive load is conserved at R_L=400 Ω.

2) Increasing the load resistance while maintaining the bias current (*2nd Apr.*)

For the same reasons mentioned previously in the second structure, the total bleeding current is kept equal to 6 mA and the load was set to R_L=550 Ω,. We noted an improvement in the conversion gain as expected without a significant degradation of the total noise figure.

TABLE IV
COMPARISON OF RESULTS OF ALL STRUCTURES

	UMTS (2100 MHz)					DECT (1900 MHz)					GSM (960 MHz)				
	1st STR	**2nd STR**		**3rd STR**		**1st STR**	**2nd STR**		**3rd STR**		**1st STR**	**2nd STR**		**3rd STR**	
		1st Apr.	*2nd Apr.*	*1st Apr.*	*2nd Apr.*		*1st Apr.*	*2nd Apr.*	*1st Apr.*	*2nd Apr.*		*1st Apr.*	*2nd Apr.*	*1st Apr.*	*2nd Apr.*
CG (dBm)	9.5	12.1	12	12.1	12	9.2	11.9	11.8	11.9	11.8	10.7	12.2	11.7	12	11.5
CP1 (dBm)	-10.5	-10	-10.5	-10.5	-11	-8	-9	-9.5	-9	-10	-12.5	-12.5	-12	-13	-12
NF (dB)	9.9	9.8	10.1	9.7	10	9.4	8.9	9.3	8.8	9.1	9.3	9.5	10.1	9.5	10.1
IIP3(dBm)	0.8	2.2	-0.3	2.1	-0.3	1.2	2.8	0.8	2.5	0.9	-1.6	-2.8	-2.3	-2.5	-2.1
Power dissip. (mW)	18	24	18	24	18	18	24	18	24	18	18	24	18	24	18
Technique	Gilbert Cell	Current-bleeding		Charge injection		Gilbert Cell	Current-bleeding		Charge injection		Gilbert Cell	Current-bleeding		Charge injection	

V. DISCUSSION

Table IV summarizes the performance parameters of the three structures studied above. The Gilbert-cell structure provides a low conversion gain and a moderate linearity. The current-bleeding and charge injection techniques used in the second and third structures, respectively, allow a conversion gain improvement of ~2dB for the same power consumption of 18 mW (1st *Apr.*). There is no significant effect on the total noise figure. With these techniques, it is also possible to improve the circuit linearity by increasing the total bias current, which naturally cause an increase in consumed power from 18 to 24 mW (2nd *Apr.*).

Under the same RF and LO biasing conditions, the performances achieved by the second and third structures are very similar. When lower power consumption is needed, the use of p-channel transistors as bleeding sources in the first structure put constraints on the minimal supply voltage needed. This drawback can be surmounted using a charge injection method as presented in the third structure. In this case, the high value of *Rd* needed would require a larger silicon area. Also, this degrades the frequency response of the switching stage.

The above study has contributed to gain more insights on the design of multi-standard mixers. It helps figure out what structure to use and how to optimize it.

VI. CONCLUSION

A design methodology of down-conversion mixers suitable for multi-standard UMTS, DECT and GSM receivers was presented. The models for noise figure, conversion gain and IIP3 used in this methodology were discussed. Techniques such as current bleeding and charge injection were studied and compared with the standard Gilbert cell. These two techniques boost the conversion gain by about 2 dB with no significant degradation of over characteristics. The study compares the nature of trade-offs inherent in these techniques and identifies what technique would be better under given conditions.

REFERENCES

[1] A. Verma, K. O. Kenneth and J. Lin,"A Low-Power Up-Conversion CMOS Mixer for 22–29-GHz Ultra-Wideband Applications", *IEEE Transactions on Microwave Theory and Techniques*, vol. 54, no. 8, pages: 3295- 3300, August 2006

[2] L. Liu and Z. Wang; "Analysis and design of a low-voltage RF CMOS mixer**",** *IEEE Transactions on Circuits and Systems —II: Express Briefs*, vol. 53, Issue 3, Page(s):212 - 216, March 2006

[3] V. Vidojkovic, J. Van der Tang, A. Leeuwenburgh and A. v. Roermund "A DECT/Bluetooth multi-standard front-end with adaptive image rejection in 0.18 /spl mu/m CMOS", *Circuits and Systems, 2004. ISCAS '04. Proceedings of the 2004 International Symposium I (ISCAS.2004)*, vol. I, pp. 573-576, 2004.

[4] B. Gilbert "The Micromixer: a highly linear variant of the Gilbert mixer using a bisymmetric class-ab input stage", *IEEE Journal of Solid-State Circuits*, Vol. 32, No. 9, pp.1412-1423, 1997.

[5] A.Q.Safarian, A.Yazdi and P.Heydari; **'**Design and analysis of an ultrawide-band distributed CMOS mixer' *Very Large Scale Integration (VLSI) Systems*, IEEE Transactions on, Volume 13, Issue 5, Page(s):618 – 629, May 2005.

[6] A. Ismail and A. Abidi 'A 3 to 10 GHz LNA using a wideband LC-ladder matching network' in *IEEE ISSCC Dig. Tech.*. Papers, pp. 384-385, 2004.

[7] M. Terrovitis and R. G. Meyer "Noise in Current-Commutating CMOS Mixers", *IEEE Journal of Solid-State Circuits*, vol. 34, 1999.

[8] V. Geffroy, "RF mixers using standard digital CMOS 0.35µm process" *IMS2001/RFIC 2001 Technical Sessions,* 2001.

[9] S.Douss and M.Loulou, 'Design of enhanced performances CMOS RF mixers suitable for multi-standards receiver'*1 International IEEE Conference on Design & Test of Integrated Systems in Nanoscale Technology*, IEEE DTIS'06, September 2006.

[10] B. Razavi "Design of Analog CMOS Integrated Circuits", *McGraw-Hill,* 2001.

[11] L. A. MacEachern and T. Manku, ,'A charge-injection method for Gilbert cell biasing'. *IEEE Canadian Conf. Electrical and Computer Engineering*, pp. 365-368, 1998.

[12] S.G. Lee and J.-K. Choi "Current-reuse bleeding mixer", *Electronics Letters, Vol.36, Issue 8*, pp. 696 – 697, 2000.

[13] V. Vidojkovic, J. Van der Tang, A. Leeuwenburgh and A. v. Roermund, "mixer topology selection for a 1.8 - 2.5 GHz multi-standard front-end in 0,18 µm CMOS", *International Symposium on Circuits and Systems (ISCAS.2003)*, vol. II, pp. 300-303, 2003.

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