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A Behavior Model of Discrete Sampling and Hold Amplifier based on AC Response

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***Abstract*—**A kind of behavior model for discrete sampling and hold amplifier with charge transmission is analyzed. The transfer function and behavior features are based on the main AC responses of operation amplifier. The result used in pipelined and sigma-delta ADC shows the exact of model of sampling and hold amplifier, and the non-ideal factors are taken into account.

***Keywords*—**SHA, response, behavior, transfer function.

I. Introduction

SAMPLE and hold amplifier (SHA) is an important part of analog circuit. According to Nyquist criterion, it can hold the information of the signal accurately. In fact, as there are some non-ideal factors of amplifier, the effect of sample and hold amplifier could be deteriorated.

This paper presents a new behavior design theory of sample and hold amplifier based on MATLAB. Contrary to the traditional model, the model analyzes SHA from aspect of AC characters of amplifier such as gain, bandwidth, and phase margin instead of some inconspicuous factors such as resistance, capacitance, and conductance. So the model shown in this paper is more intuitionistic, and can be analyzed easily.

The paper has 5 parts. Following the introduction, the amplifier from system view is analyzed, and a proper model of amplifier will be given. In section III, according to the behavior of SHA, a proper model of SHA based on amplifier will be given. Section IV presents some testing result to justify the model. Section V is on conclusion.

II. Behavior Module of SHA

Now, in most analog design of ADC, SHA is the first part and its performance is very important for the accuracy of ADC. Along with the circuit design, behavior module should be researched further. It provides the behavior validation of the theory and analysis for the circuit design.

The discrete time switched-capacitor of sampling and hold amplifier can be equal to a continual time SHA with a discrete time input source in operation period [1], the equal model is shown in Fig. 1.

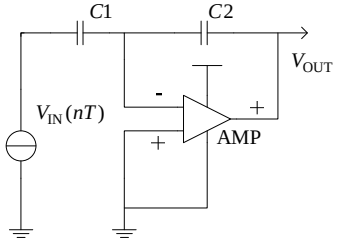

Fig. 1 Equivalent module of SC circuit

In this module, operational amplifier as an important part affects the whole circuit seriously. Traditionally, the amplifier is analyzed from transistor level, use the resistance, capacitance and conductance of transistors to analyze the amplifier and get the response. This method is accurate but not intuitionist. That is because it is not easy to get such characters and the AC characters should be considered with gain, bandwidth and phase margin in system level. So this part aims at a connection between AC characters and response directly.

A. Amplifier Model of Single Pole

To better understand this method, the process of single pole amplifier modeling is shown. In Fig. 2, there is a common-source amplifier with the load C_L. Using the system view, this amplifier can be seen as a transfer net.

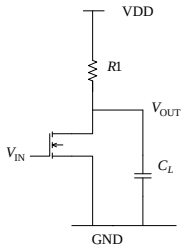

Fig. 2 The common source amplifier

In this net, there is only one pole, the pole can be calculate by formula $1/(2\pi \cdot R_0 \cdot C_L)$, R_0 is output resistance of amplifier [2]. This pole cause 20dBc/dec rolling down and 90 degree phase shifting in bode diagram. So we can connect the pole and AC characters such as gain, bandwidth, and phase margin.

According to the relation between phase margin and pole,

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$$Pm=180^0-\arctan(GBW/W_1) \quad (1)$$

So,

$$W_1=GBW/\tan(180^0-Pm) \quad (2)$$

Or, according to the relation between gain and pole,

$$W_1=GBW/(10\wedge\frac{(A_0-3)}{20}) \quad (3)$$

Pm is phase margin, W_1 is main pole, GBW is unity gain bandwidth, A_0 is dc gain. Solve those formula, we can obtain the pole. So the transfer function is,

$$H(s)=\frac{A_0}{(1+\frac{s}{W_1})} \quad (4)$$

B. Amplifier Model of Two Poles

The amplifier usually has two main poles, and the amplifier with more than two main poles seldom used because of stability. The most common amplifier with two poles is the cascode amplifier which shown in Fig. 3.

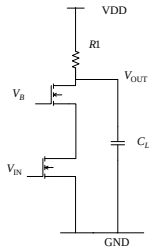

Fig. 3 The cascode amplifier

The modeling process of two poles amplifier is same as single pole amplifier, but the position of the pole should be analyzed carefully.

When the second pole beyond the GBW, within the GBW there is 20dBc/dec rolling down in bode diagram. So it contains two poles by relation below:

$$Pm=180^0-\arctan(GBW/W_1)-\arctan(GBW/W_2) \quad (5)$$

$$W_1=GBW/(10\wedge\frac{(A_0-3)}{20}) \quad (6)$$

And if the second pole is within GBW, there is 20dBc/dec rolling down and 40dBc/dec rolling down followed within the GBW. So we can obtain the two poles by formula below:

$$Pm = 180^\circ - \arctan(GBW / W_1) - \arctan(GBW / W_2) \quad (7)$$

$$A_{W2}=40\cdot\log_{10}(GBW/W_2) \quad (8)$$

$$W_1=W_2/(10\wedge\frac{(A_0-A_{W2})}{20}) \quad (9)$$

So we can calculate the transfer function of two poles amplifier.

$$H(s)=\frac{A_0\cdot W_1\cdot W_2}{S^2+(W_1+W_2)\cdot S+W_1\cdot W_2} \quad (10)$$

In the Fig. 4 and Fig. 5, the simulations of model and Spectre are shown. The amplifier has same AC characters: gain 61.31dB, phase margin 76.4 degree, bandwidth 469.2 MHz.

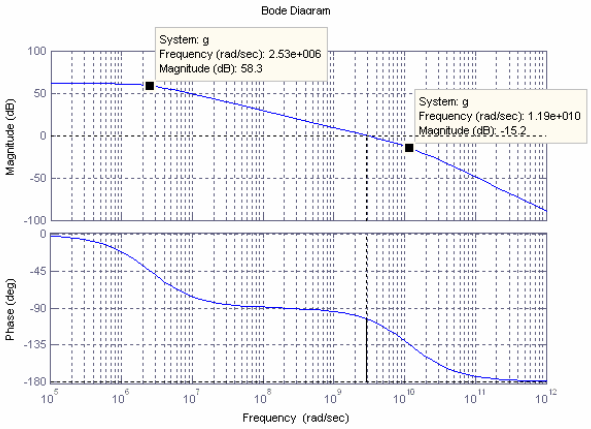

Fig. 4 Bode diagram in Matlab

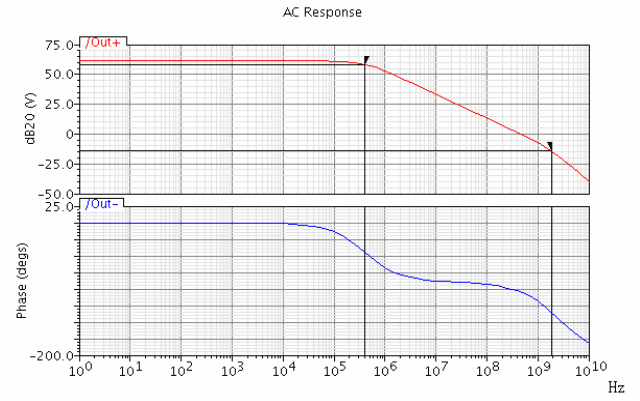

Fig. 5 Bode diagram in Spectre

In the result of Matlab, the pole is shown with unit rad/sec, convert it to Hz, W_1 and W_2 are 403KHz and 1.89GHz: the result in Spectre shown the two poles are 408KHz and 1.87GHz. The result of two poles justifies the method of amplifier modeling is accuracy.

III. Sampling and Hold Amplifier

Based on the amplifier with two poles, the relationship between input and output is shown in this section. And the operational conditions are analyzed in detail.

In ideal condition, the input of system is a step signal, so the output will be a same step signal because of the unite loop gain. But in reality, there are some non-ideal factors such as amplifier performance, the output need some time to achieve the final voltage, this time is called setup time. The setup time can divide to two parts period of small signal which is determined by GBW and period of large signal which is determined by the speed of capacitor charging. Link to the C.T.Chuang model [3], when the amplitude of signal is smaller than critical voltage(V_P), output current has a linearity relation with input voltage(period of small signal); when the amplitude of signal is larger than critical

voltage, output current is constant, the constant output current is maximum current charge for load capacitor. The critical voltage is V_P, it can be calculated by formula I_{sat}/g_{m1}. Fig. 6 is a math model for transient analysis during the process of output signal setting up.

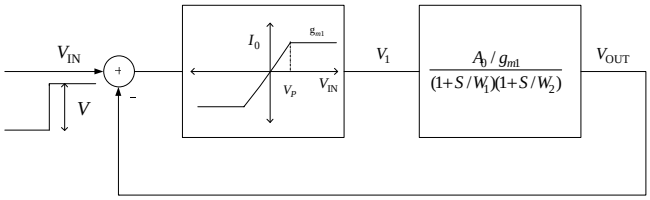

Fig. 6 Mathematical model of SHA

According to the relation of I_{sat}, SR, GBW and g_m. Such as,

$$I_{\text{sat}}=\text{SR}\cdot C_L \tag{11}$$

$$2\pi\cdot\text{GBW}=\frac{g_m}{C_L} \tag{12}$$

So, we can convert the critical voltage V_P to a new form,

$$V_P=\frac{I_{\text{sat}}}{g_{m1}}=\frac{\text{SR}}{2\pi\cdot\text{GBW}} \tag{13}$$

Now, all the variables which are need for the SHA are linked to the amplifier AC characters. Those are poles, transfer function, V_P.

A. Analysis for Large Signal

When the signal is larger than V_P, so the amplifier is working in the time of setting up large signal [4]-[5]. The SHA can be seen as a current source instead of two poles system, and the time can be determined by the speed of load capacitor charging as in (14).

$$V_{out}=\text{SR}\cdot t \tag{14}$$

B. Analysis for Small Signal

When the amplitude of input signal is smaller than V_P, the amplifier is working in small signal setting up. So the response of SHA can be determined by transfer function. According to the equal model of SHA, so the transfer function of SHA is:

$$H_S(s)=\frac{C1}{C2}\cdot\frac{b\cdot A(s)}{1+A(s)} \tag{15}$$

b is feed-back factor, and $b=C2/(C1+C2)$; $A(s)$ is open loop transfer function of amplifier, which is,

$$A(s)=\frac{A_0\cdot W_1\cdot W_2}{S^2+(W_1+W_2)\cdot S+W_1\cdot W_2} \tag{16}$$

So the transfer function of SHA can be denoted as,

$$H_S(s)=\frac{C1}{C2}\cdot\frac{A_0\cdot b\cdot W_1 W_2}{s^2+(W_1+W_2)\cdot s+(1+A_0\cdot b)\cdot W_1\cdot W_2} \tag{17}$$

The SHA has two poles, according to the poles of amplifier, the poles of SHA can be calculated by,

$$S_{1,2}=\frac{1}{2}\cdot[-(W_1+W_2)\pm\sqrt{(W_1+W_2)^2-4(1+A_0\cdot b)\cdot W_1\cdot W_2}\,] \tag{18}$$

In order to analyze conveniently, define $W_n=\sqrt{(1+A_0)\cdot W_1\cdot W_2}$, and $dam=(W_1+W_2)/(2\cdot W_n)$. W_n is nature oscillation frequency, and dam is coefficient of damp. So the poles of SHA can be denoted as,

$$S_{1,2}=-dam\cdot W_n\pm W_n\sqrt{dam^2-1} \tag{19}$$

The response can be determined by those two poles, with different coefficients, the output can be calculated in different ways below.

① $dam<1$

$$V_S(t)=\frac{(1-b)}{b}\cdot\frac{A_0\cdot b}{1+A_0\cdot b}\cdot V\cdot\{1-\frac{V_P/V}{\sqrt{1-dam^2}}e^{-dam\cdot W_n(t-T_1)}\}\cdot\sin\phi \tag{20}$$

② $dam=1$

$$V_S(t)=\frac{(1-b)}{b}\cdot\frac{A_0 b}{1+A_0 b}V\cdot\{1-\frac{V_P}{V}[e^{-dam W_n(t-T_1)}+W_n(t-T_s)e^{-W_n(t-T_1)}]\} \tag{21}$$

③ $dam>1$

$$V_S(t)=\frac{(1-b)}{b}\cdot\frac{A_0\cdot b}{1+A_0\cdot b}V\cdot\{1-\frac{V_P}{V}\cdot[\frac{(dam+\sqrt{dam^2-1})^{\alpha}}{2\sqrt{dam^2-1}}]\} \tag{22}$$

T_1 is the time of large signal period, $\phi=W_n\sqrt{1-dam^2}\cdot(t-T_1)+\arctan(\sqrt{1-dam^2}/dam)$, V is amplitude of input signal, $\alpha=(-W_n)\cdot(t-T_1)\cdot(dam-\sqrt{dam^2-1})$. Now, the different response with different input signal in time-domain is analyzed clearly.

C. Full Process of Output Setting Up

According to the analysis before, we can divide the process of output setting up to two parts, larger signal period and small signal period. The flow plan can be seen in Fig. 7 below.

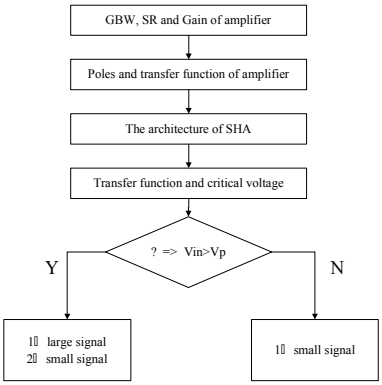

Fig. 7 Modeling flow plan

If the amplitude of signal is V_{in}, critical voltage is V_P, the period of clock is T_S, so the full process can be calculated as following:

(1) If $V_{in} > V_p$, the SHA will work in large signal period first, the time of large signal period is $T_1 = V_p / \mathrm{SR}$.

① If $T_1 > T_S/2$, SHA will not enter the small signal period, so the final output is $V_{out} = \mathrm{SR} \cdot T_s / 2$.

② If $T_1 < T_S/2$, SHA will work in large signal first, when the output larger than V_P, SHA will work in small signal period, the time of small signal period will be $T_E = T_S/2 - T_1$, so the final output is $V_{out} = V_P + V_S(t)\big|_{t=T_E}$.

(2) If $V_{IN} < V_P$, SHA will work in small signal directly, so the output will be $V_{out} = V_S(t)\big|_{t=T_S/2}$.

IV. Simulation

This section will show some measurement, all the results are based on Matlab. As shown in Fig. 8, all the variables are link to those appeared before.

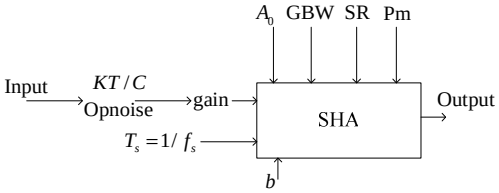

Fig. 8 The math model of SHA in Matlab

A_0 is open loop dc gain, GBW is unite gain bandwidth, SR is slew rate, Pm is phase margin, those variables are link to the performance of amplifier; b is feed-back factor, which is determined by the architecture of SHA; T_S is period of system clock, KT/C is noise of switch-capacitor circuit, OpNoise is white noise of amplifier, Gain is real close loop gain consider finite gain of amplifier and mismatch of capacitor [6]. Through sweeping those variables, different response can be obtained, so we can analyze the character of SHA model. In Table I, there are several cases, the blanks are sweeping variable, and the results are also shown after the table.

TABLE I
Simulation Condition

	Vin (v)	A_0 (dB)	GBW (MHz)	SR (Mv/s)	Pm	f_S (MHz)	f_{IN} (MHz)	C_L (pF)
1	1		200	200		50		
2	1				65°	50		
3		100	200	200	65°	50	10	1
4	1		200	200	65°			
5	1		200	200	65°	50		

A. Step Responses of Different Phase Margin

All the variables in SHA are shown as Table I(1). The step response is shown in Fig. 9, and it can be seen clearly that there are two parts, one is large signal period, and another is small signal period.

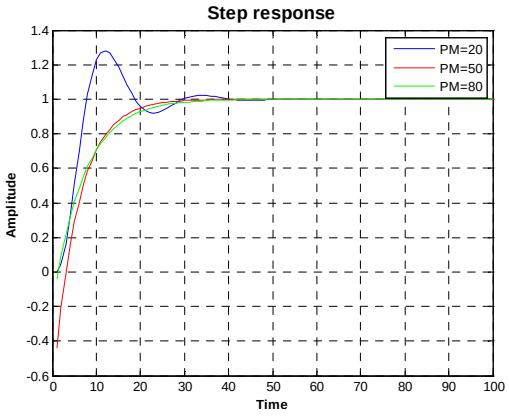

Fig. 9 Step responses of different phase margin

B. Step Responses of Different GBW and SR

All the variables in SHA are shown in Table I(2), the step response is shown in Fig. 10. If GBW and SR increase, the error which is difference between ideal output and real output will decrease in the condition that other variables are constant.

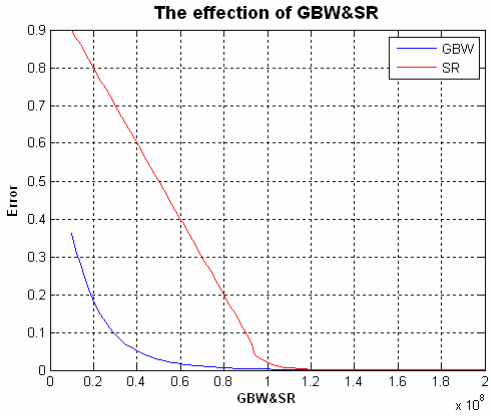

Fig. 10 The relation between GBW, SR and error

C. Step Responses of Different Amplitude of Input Signal

After the analysis of AC characters of amplifier, we can choose proper AC characters which are shown in Table I(3), and make the simulation about different amplitude of input signal. From Fig. 11, the larger amplitude of input signal is the larger error is in the condition that other variables are constant.

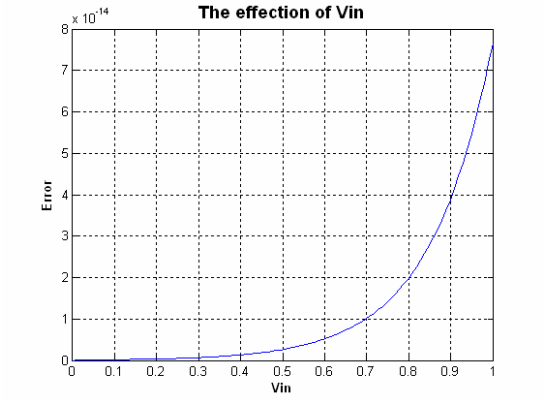

Fig. 11 The relation between amplitude of input and error

D. Step Responses of Different Period of Clock

The clock is a control signal of SHA, which has serious effect to the performance of SHA. For the given variables such as in Table I(4), if the period of clock decreases, the performance of SHA such as SNR, SFDR will decrease shown in Fig. 12.

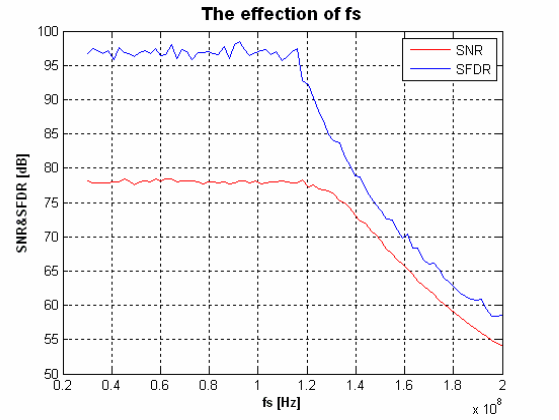

Fig. 12 The relation between frequency of clock, SNR and SFDR

E. The Power Spectral Density

Consider all the analysis before, we choose a group of variables which are shown in Table I(5). The power spectral density is shown in Fig. 13.

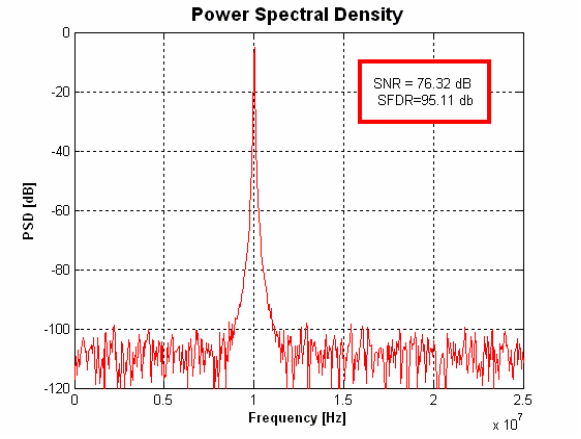

Fig. 13 The power spectral density

V. Conclusion

This paper show a new model of SHA which is based on the AC characters of amplifier. Through the AC characters of amplifier, the transfer functions of amplifier and SHA are deduced, and realize the new model of SHA. Contrary to the traditional model, the new model focuses on the relation between performance of SHA and AC characters of amplifier, and some non-ideal factors such as noise, mismatch also is considered. So the new model will be more suits for the behavior modeling and analysis of large analog circuit such as pipelined ADC and sigma-delta modulator.

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