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Low Leakage MUX/XOR Functions Using Symmetric and Asymmetric FinFETs

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Abstract**—**In this paper, FinFET devices are analyzed with emphasis on sub-threshold leakage current control. This is achieved through proper biasing of the back gate, and through the use of asymmetric work functions for the four terminal FinFET devices. We are also examining different configurations of multiplexers and XOR gates using transistors of symmetric and asymmetric work functions. Based on extensive characterization data for MUX circuits, our proposed configuration using symmetric devices lead to leakage current and delay improvements of 65% and 47% respectively compared to results in the literature. For XOR gates, a 90% improvement in the average leakage current is achieved by using asymmetric devices. All simulations are based on a 25nm FinFET technology using the University of Florida UFDG model.

Keywords**—**FinFET, logic functions, asymmetric work-function devices, back gate biasing, sub-threshold leakage current.

I. Introduction

THE demand for smaller and faster electronic equipment has forced the integrated circuit fabrication technology to a sharp reduction in the minimum feature size of the transistors from the micro to the nanometer regime. Accordingly, other device parameters such as threshold voltage, supply voltage, and gate oxide thickness must also be scaled down to maintain device scalability rules [1]. These reductions have affected the static power dissipation of the circuits. This situation becomes a concern in sub-22nm bulk CMOS technology because of very poor channel electrostatic potential which leads to degraded short-channel behavior and high leakage current [1], [2]. FinFET transistors overcome these problems with a stronger control of the channel potential by using two gates wrapped around the fin [2]. Until now, a limited study has been performed on arithmetic functions based on only symmetric FinFET devices [3], [7], and [8]. The goal of this paper is to develop circuit topologies and configurations that lead to high performance low leakage arithmetic components using symmetric FinFETs. Also, we have developed a new approach by utilizing back gate biasing for asymmetric devices without using any extra power supplies for arithmetic functions to achieve ultra low leakage current, yet maintaining high performance. Device and circuit characterizations were performed in a SPICE simulation environment using the

University of Florida double gate device models (UFDG) [4], with typical 25nm FinFET device parameters, which are listed in the next section.

The rest of the paper is organized as follows. A brief review of four terminal FinFET devices and mechanisms to control leakage current are presented in Section II. In Section III, we examine different circuit topologies of multiplexer function utilizing symmetric and asymmetric FinFET devices. Symmetric and asymmetric topologies of XOR gate are discussed in section IV. Section V concludes the paper.

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II. Four Terminal Devices and Leakage Current Control

Four terminal FinFETs were extensively studied and analyzed in [3] and [5]. These devices could be more beneficial than three terminal FinFETs since the threshold voltage can be adjusted by biasing the back gate terminal which tends to reduce sub-threshold leakage current and improve the slope factor. In addition, four terminal FinFETs can merge two parallel transistors into one transistor, by tying independent signals to both the front and back gates, which is beneficial in reducing area and power dissipation in digital circuits [5]. For the device shown in Fig. 1, the effective channel length (L) and width (W_{min}) are equal to L_{FIN} and h_{FIN} respectively. The device parameters used in this paper are listed in Table I.

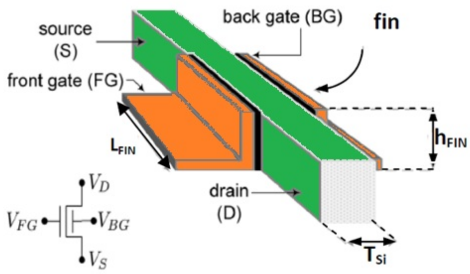

Fig 1 Four terminal FinFET device [5]

To demonstrate the effect of back gate biasing on I_{ON} and I_{OFF}, we simulated both NFinFET and PFinFET devices for a channel width of 25nm, and for a fixed value of V_{DS} of 1.2V. The back gate biasing voltages were altered from -0.4 to 0.4V and 0.8 to 1.6 V for the N and PFinFETs respectively. The results for both devices are shown in Tables II and III. The first important point to note from the simulation results is that the average driving capability of the NFinFET is 6 times better than the dual P device. On the other hand, the average leakage current for the P device is significantly less than that of the N device for the same range of back gate biasing voltages. Hence, back gate biasing technique is more effective in controlling the leakage current in NFinFET devices than in PFinFET.

In addition, Table II indicates that I_{OFF} drops by a factor of 300 when V_{BG} varies from 0 to -0.4V. This drop is much higher as V_{BG} is altered from 0.4V to -0.4V. However, due to high leakage, positive values of V_{BG} are not practical. For PFinFET devices, Table III indicates that I_{OFF} improves by a factor of 4 when V_{BG} varies from 1.2V to 1.6V. The drop is higher as V_{BG} is varied from 0.8V to 1.6V. However, due to high leakage, gate voltages less than V_{DD}=1.2V are not practical.

TABLE I
DEVICE PARAMETERS FOR FINFET

PARAMETER	VALUE
LENGTH OF THE CHANNEL (L)	25 NM
THICKNESS OF FRONT/BACK GATE OXIDE (T_{OXFG}/T_{OXBG})	1 NM
THICKNESS OF THE FIN (T_{SI})	14 NM
HEIGHT OF THE FIN (H_{FIN})	25 NM
WORK FUNCTION (N/P) (Φ_N/Φ_P)	4.6 EV
POWER SUPPLY (V_{DD})	1.2 V
CHANNEL DOPING (N_{BODY})	1E15 CM^{-3}

As for the slope factor $= \frac{\partial V_{FG}}{\partial log I_d}$, the improvement is 21% as the back gate voltage of the NFinFET changes from 0V to -0.4V, while for the P devices the improvement is only 4% by varying the back gate voltage from 1.2 to 1.6V as shown in Figs. 4 and 5 respectively. Hence, it seems that the slope factor of P devices have less dependency on the back gate biasing.

TABLE II
DATA FOR FOUR-TERMINAL NFINFET

V_{BG}(V)	I_{ON}(A)	I_{OFF}(A)
-0.4	1.11E-05	1.09E-13
-0.2	1.34E-05	1.79E-12
0	1.57E-05	3.31E-11
0.2	1.82E-05	7.86E-10
0.4	2.08E-05	2.15E-08

TABLE III
DATA FOR FOUR-TERMINAL PFINFET

V_{BG}(V)	I_{ON}(A)	I_{OFF}(A)
0.8	5.08E-06	2.55E-16
1	3.74E-06	2.92E-17
1.2	2.60E-06	4.99E-18
1.4	1.62E-06	1.87E-18
1.6	8.80E-07	1.44E-18

A. Impact of Asymmetric Work Functions on Sub-Threshold Leakage Current

The work function difference between the gate and the channel of a FinFET transistor dictates the threshold voltage of the device. It is a function of the gate material and the doping concentrations [6]. For a double gate FinFET, the use of asymmetric work functions has been found to have an effective control on the leakage current [2]. Achieve this property is a non-trivial matter which requires a very well controlled and selective doping process; hence, increasing the complexity and the cost of fabrication. However, due to its effectiveness in controlling the leakage current, we decided to explore this avenue.

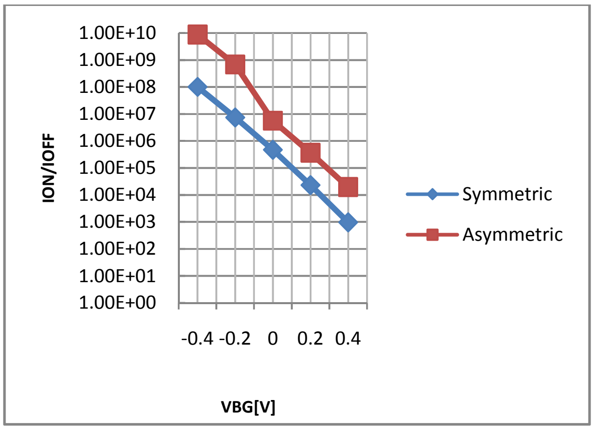

Fig. 2 Ratio I_{ON}/I_{OFF} for the four terminal NFinFET

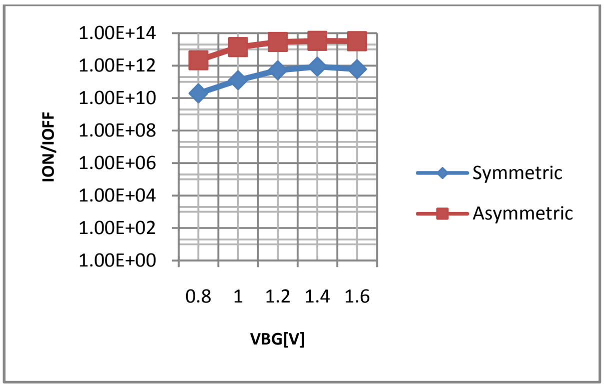

Fig. 3 Ratio I_{ON}/I_{OFF} for the four terminal PFinFET

We have characterized N (P) FinFET devices by increasing (decreasing) the work functions of the back gate in steps of 0.1eV. Figs. 2 and 3 show the ratio I_{ON}/I_{OFF} as a function of V_{BG} for symmetric and asymmetric N and PFinFETs respectively. The asymmetric devices have front gate work functions of 4.6eV and back gate work functions adjusted to 4.8eV and 4.4ev for the NFinFET and PFinFET respectively. Results show that the ratio I_{ON}/I_{OFF} for the NFinFET devices improves by a factor of 100 for a voltage of V_{BG} varying from -0.4V to -0.2V. On the other hand, for PFinFET devices, the ratio I_{ON}/I_{OFF} improves by a factor of 100 for a value of V_{BG} varying from 0.8V to 1.0V. In addition, for the slope factor S of the asymmetric N and P FinFET devices shown in Figs. 4 and 5 we can see an average improvement of 5% and 2% respectively compared to symmetric devices for the same change of back gate bias voltage.

The above results demonstrate the effectiveness of the use of asymmetric devices in achieving superior ratio of I_{ON}/I_{OFF} and sub-threshold slope factor metrics compared to symmetric devices.

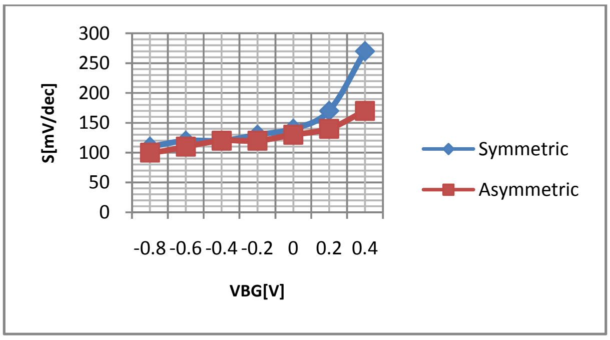

Fig. 4 Slope factor for symmetric and asymmetric four terminal NFinFET

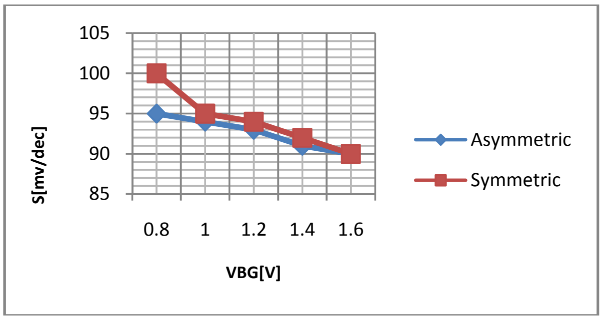

Fig. 5 Slope factor for symmetric and asymmetric four terminal PFinFET

III. Symmetric and Asymmetric FinFETs for Multiplexer Circuits

In this section, sub-threshold leakage current and transient characteristics of four terminal FinFET based multiplexer circuits in different topologies are considered. The multiplexer is one of the arithmetic components used to realize various arithmetic circuits such as adders and multipliers [1]. Hence, the optimization of this block is critical to obtain high performance low leakage computer arithmetic design. The transistors are initially sized with W_n=W_p= 25nm. The leakage current I_{OFF} is presented as an average for all input combinations by considering the leakage current of the buffers. The delay t_p is for the worst case scenario for a fan-out of four (FO4). One fan-out is represented by an inverter with transistors short gated, i.e. both the front and back gates are tied together. A voltage called V_{bbn} is defined as the back gate voltage of the transistors in the pull down networks.

It should be noted that the findings in the previous section dictated the following design strategies to design digital circuits:

1: Back gate biasing is more beneficial for pull down devices due to their leakage current dominance.

2: The back gates of pull up devices are short gated to their front gates to improve drivability, and due to their lower leakage current compared to pull down devices.

3: Applying asymmetric devices is an alternative design strategy to achieve significantly lower leakage current.

A. Transmission Gates MUX

A traditional method to implement the multiplexer based on bulk CMOS transistors is to use transmission gates (TGs) [1]. The main problem of this topology is the weak drivability, especially when cascading a number of these components. Buffers are usually added to the design to provide sufficient driving strength. On the other hand, with the addition of a buffer, the parasitic capacitance at the output is increased. However, FinFET transistors have a better driving current capability due to their double gate structures, especially when the back gate of the transistor is tied to the front gate. Hence, the need for an extra buffer at the output to improve drivability may not be necessary.

Based on the design strategies mentioned earlier in this section, the configuration in Fig. 6 is proposed to achieve the best trade-off between leakage current and delay. In this configuration, the NFinFET devices are back biased to V_{bbn}=-0.2V, with short gated PFinFETs. All devices have symmetric work functions. The other configuration is to replace the transistors with asymmetric counterparts with work functions of the back gates set to 4.8eV and 4.4eV for N and P devices respectively with V_{bbn}=0V. Simulations were conducted for the proposed configuration of the transmission gates multiplexer circuit based on symmetric and asymmetric four-terminal FinFET devices. Results shown in Table IV indicate that the asymmetric device based configuration has reduced leakage current by a factor of 7 with a very small delay improvement of 2% compared to the symmetric case. Also, using V_{bbn}=0V has the advantage of not requiring an additional power supply which impact on the overall area and cost.

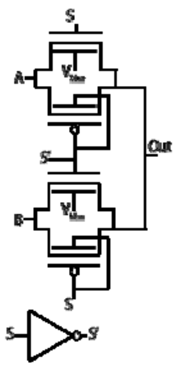

Fig. 6 Optimal configuration of transmission gates MUX

TABLE IV
RESULTS FOR TRANSMISSION GATES MUX

OPTIMAL MODE	SYMMETRIC V_{BBN}=-0.2V	ASYMMETRIC V_{BBN}=0V
I_{OFF} (pA)	38.02	5.62
T_P (pS)	12.11	11.89
STATIC POWER*DELAY (zJ)	552.50	80.19

B. Complex Gate MUX

The traditional configuration of complex gate multiplexer based on short gated FinFET transistors, which is called SG FinFET complex gate multiplexer, was extensively studied and analyzed in [7]. However, we modified the latter configuration as shown in Fig. 7, by merging each combination of two parallel transistors into one transistor in the pull up network by tying the individual gates of the same PFinFETs to two independent signals to reduce area. We refer to this topology as *hybrid mode*. The back gates of devices in the pull down network are also tied to V_{bbn}=-0.2V to reduce leakage current. This configuration makes use of both stacking effect and back gate biasing techniques to reduce sub-threshold leakage current.

Simulations were conducted for this hybrid mode of operation based on symmetric devices, which used an additional 0.2V power supply, and asymmetric devices, without using an extra power supply. Results shown in Table V indicate that utilizing asymmetric devices achieved a factor of 6 decrease in leakage current with a small delay penalty of 5% compared to the circuit based on symmetric devices.

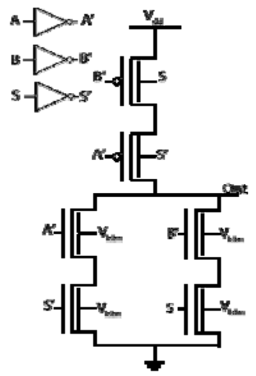

Fig. 7 Hybrid mode of FinFET static CMOS MUX

TABLE V
RESULTS FOR COMPLEX MUX

HYBRID MODE	SYMMETRIC V_{BBN}=-0.2V	ASYMMETRIC V_{BBN}=0V
I_{OFF} (pA)	34.95	5.79
T_P (pS)	28.59	30.24
STATIC POWER*DELAY (zJ)	1.20	0.21

C. IG FinFET MUX

The independent gate (IG) FinFET implementation of a MUX circuit shown in Fig. 8 was examined and analyzed extensively in [8] as a best candidate to make efficient use of the FinFET structure based on multiplexer function. The gates of each transistor are driven from two independent signals, hence reducing the total number of transistors, to provide drivability and to reduce leakage current. Simulations were conducted for symmetric devices utilized in this configuration.

As an extension to this work, we have examined other possible configuration using asymmetric transistors. Results shown in Table VI indicate that by applying asymmetric work functions, the leakage current of the circuit using asymmetric devices decreased by a factor of 20 with a delay penalty of 27% compared to symmetric ones.

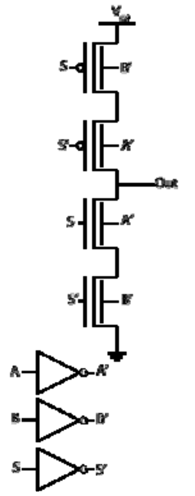

Fig. 8 IG FinFET MUX

TABLE VI
RESULTS FOR IG MODE MUX

IG MODE	SYMMETRIC V_{BBN}=-0.2V	ASYMMETRIC V_{BBN}=0V
I_{OFF} (pA)	108.57	5.38
T_P (pS)	22.57	31.03
STATIC POWER*DELAY (zJ)	2.94	0.20

D. Pass Transistor Logic MUX

The pass transistor logic (PTL) topology uses single transistor to replace the transmission gates with NFinFET transistors as shown in Fig. 9. The main draw back with this topology, besides the possible skew of the control signal S, is signal degradation at the output.

One technique to fix this degradation problem is to add a weak pull up PFinFET transistor in a feedback configuration [7]. However, this results in an increase in the nodal capacitance at the output. Another technique, used in this paper, is to increase the threshold voltage of the PFinFET transistor of the inverter by using a back gate biasing voltage V_{bbp} equal to 1.4V.

Simulations were conducted for both symmetric and asymmetric devices for the FinFET configuration shown in Fig. 9. The simulation results presented in Table VII show that by using asymmetric devices, the leakage current decreased by a factor of 19 with a small delay penalty of 12% compared to symmetric work functions based configuration.

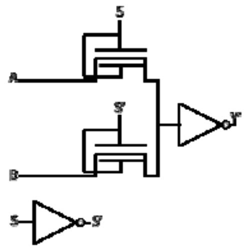

Fig. 9 PTL MUX

TABLE VII
RESULTS FOR PTL MODE MUX

PTL MODE	SYMMETRIC V_{BBP}=1.4V	ASYMMETRIC V_{BBP}=1.2V
I_{OFF} (pA)	131.58	7.10
T_P (pS)	17.23	19.53
STATIC POWER*DELAY (zJ)	2.72	0.17

E. Comparison of Different Topologies for MUX Circuit

The simulation results shown in Table VIII compares different topologies of symmetric based FinFET MUX circuits. The data shows that the transmission gates topology (TG) is the best topology for implementing the FinFET MUX function in terms of trade-off between delay and leakage and even better area density in terms of number of transistors. This topology is the best performer in terms of delay, being faster by 58% and 47% compared to the Hybrid and IG FinFET [8] respectively. In terms of sub-threshold leakage current, the TG topology achieved significantly lower leakage current by a factor of 3 compared to the IG FinFET [8]. However, the Hybrid topology has a slightly lower leakage current compared to the TG topology.

TABLE VIII
COMPARISON OF DIFFERENT TOPOLOGIES FOR THE MUX CIRCUIT

TOPOLOGY	I_{OFF} (pA)	T_P (pS)	STATIC POWER*DELAY (zJ)	NUMBER OF TRANSISTORS
TG	38.02	12.11	0.55	6
HYBRID	34.95	28.59	1.2	12
IG[8]	108.57	22.57	2.94	10
PTL	131.58	17.23	2.72	6

IV. SYMMETRIC AND ASYMMETRIC FINFET XOR GATES

Exclusive OR (XOR) gates are also considered to be a major component required to realize arithmetic circuits, specifically adders and compressors. Various CMOS based circuit topologies of XOR gates were introduced in the literature. However, in this paper, skew free, transmission gates and pass transistor logic topologies are used to realize FinFET counterparts using both symmetric and asymmetric four-terminal devices.

A. Skew Free XOR Circuit

The optimal configuration of this topology based on the design strategies discussed in the previous section is shown in Fig. 10. This configuration is achieved by tying the back gates of the pull up devices to their front gates due to their lower leakage current. Also, connecting the back gates of the pull down devices to a bias voltage V_{bbn}= -0.2V. This configuration is insensitive to the signal skew and there is no direct path between V_{dd} and ground. In addition, both pull up and pull down networks have series transistors which are more beneficial to reduce sub-threshold leakage current due to the stacking effect.

Simulations were conducted for symmetric and asymmetric devices. Results shown in Table IX illustrate that utilizing asymmetric work functions achieved a factor of 8 reduction in leakage current with a slight 4% improvement in delay performance compared to its symmetric based counterpart.

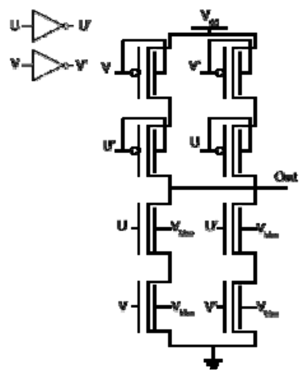

Fig. 10 Skew free configuration of XOR

TABLE IX
RESULTS FOR SKEW FREE XOR CIRCUIT

OPTIMAL MODE	SYMMETRIC V_{BBN}=-0.2V	ASYMMETRIC V_{BBN}=0V
I_{OFF} (pA)	17.30	2.18
T_P (pS)	18.01	17.34
STATIC POWER*DELAY (zJ)	0.31	0.05

B. Transmission Gates Based XOR

The optimal configuration of this topology to achieve the best trade-off between leakage and delay is shown in Fig. 11. It is implemented by applying back gate biasing for the NFinFET devices, and by shorting the back and front gates of the PFinFETs.

Simulations were conducted for both symmetric and asymmetric devices based on the optimal configuration of the transmission gate based XOR function. Results shown in Table X illustrates that using asymmetric devices achieved a factor of 11 reduction in leakage current with a small delay penalty of 10% compared to symmetric based circuit.

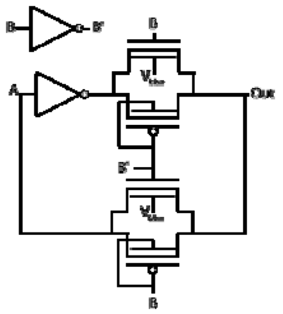

Fig. 11 Optimal configuration of transmission gates XOR

TABLE X
RESULTS FOR TRANSMISSION GATES BASED XOR

OPTIMAL MODE	SYMMETRIC V_{BBN}=-0.2V	ASYMMETRIC V_{BBN}=0V
I_{OFF} (pA)	47.53	4.15
T_P (pS)	14.07	15.69
STATIC POWER*DELAY (zJ)	0.80	0.08

C. Pass Transistor Logic (PTL) XOR

A pass transistor logic XOR configuration based on FinFET transistors is shown in Fig. 12. This topology needs a level restoration at the output, and the same approach used for the case of multiplexer is employed to solve this problem. This topology is insensitive to the skew of the input signals.

Simulations were conducted for both symmetric and asymmetric FinFETs used for this configuration. Results presented in Table XI show that by using asymmetric devices, the leakage current will be reduced by a factor of 18 with a small delay penalty of 9% compared to the symmetric configuration of PTL XOR.

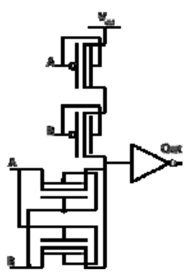

Fig. 12 PTL XOR

TABLE XI
RESULTS FOR PTL XOR CIRCUIT

PTL MODE	SYMMETRIC V_{BBP}=1.4V	ASYMMETRIC V_{BBP}=1.2V
I_{OFF} (pA)	50.92	2.82
T_P (pS)	13.73	15.01
STATIC POWER*DELAY (zJ)	0.83	0.05

D. Comparison of Different Topologies for XOR Circuit

Simulation results for different topologies of XOR gate are shown in Table XII. We see that the skew free topology is the better candidate in terms of achieving a good trade-off between leakage current and delay. This topology has much lower leakage current then either of the TG and PTL based topologies. However, the TG and PTL based topologies are 22% and 23% faster respectively compared to the skew free topology. In addition, the TG and PTL topologies have better area density since they use fewer transistors compared to the skew free topology.

TABLE XII
COMPARISON OF DIFFERENT TOPOLOGIES OF FINFET XOR

TOPOLOGY	I_{OFF} (pA)	T_P (pS)	STATIC POWER*DELAY (zJ)	NUMBER OF TRANSISTORS
SKEW FREE	17.3	18.01	0.31	12
TG	47.53	14.07	0.8	8
PTL	50.92	13.73	0.83	6

V. CONCLUSION

In this research work, four terminal FinFET devices have been analyzed with the goal of reducing sub-threshold leakage current. We applied both back gate biasing and asymmetric work functions, which are two possible methods to achieve ultra low sub-threshold leakage current in FinFET devices. The methods were employed in designing multiplexer and XOR circuits used in computer arithmetic functions. Our simulation results show that by applying asymmetric work functions, the sub-threshold leakage current can be reduced significantly with low delay penalty or even a slight reduction in delay for some configurations. Also, we are avoiding the use of additional power supply. However, asymmetric circuits are more costly to implement since careful adjustment of the doping profiles is required for both sides of the same FinFET transistor.

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