Influence of Paralleled Capacitance Effect in Well-defined Multiple Value Logical Level System with Active Load

Chih Chin Yang, Yen Chun Lin, and Hsiao Hsuan Cheng

Abstract—Three similar negative differential resistance (NDR) profiles with both high peak to valley current density ratio (PVCDR) value and high peak current density (PCD) value in unity resonant tunneling electronic circuit (RTEC) element is developed in this paper. The PCD values and valley current density (VCD) values of the three NDR curves are all about 3.5 A and 0.8 A, respectively. All PV values of NDR curves are 0.40 V, 0.82 V, and 1.35 V, respectively. The VV values are 0.61 V, 1.07 V, and 1.69 V, respectively. AllPVCDR values reach about 4.4 in three NDR curves. The PCD value of 3.5 A in triple PVCDR RTEC element is better than other resonant tunneling devices (RTD) elements. The high PVCDR value is concluded the lower VCD value about 0.8 A. The low VCD value is achieved by suitable selection of resistors in triple PVCDR RTEC element. The low PV value less than 1.35 V possesses low power dispersion in triple PVCDR RTEC element. The designed multiple value logical level (MVLL) system using triple PVCDR RTEC element provides equidistant logical level. The logical levels of MVLL system are about 0.2 V, 0.8 V, 1.5 V, and 2.2 V from low voltage to high voltage and then 2.2 V, 1.3 V, 0.8 V, and 0.2 V from high voltage back to low voltage in half cycle of sinusoid wave. The output level of four levels MVLL system is represented in 0.3 V, 1.1 V, 1.7 V, and 2.6 V, which satisfies the NMP condition of traditional two-bit system. The remarkable logical characteristic of improved MVLL system with paralleled capacitor are with four significant stable logical levels about 220 mV, 223 mV, 228 mV, and 230 mV. The stability and articulation of logical levels of improved MVLL system are outstanding. The average holding time of improved MVLL system is approximately 0.14 μs. The holding time of improved MVLL system is fourfold than of basic MVLL system. The function of additional capacitor in the improved MVLL system is successfully discovered.

Keywords—Capacitance, Logical level, Constant current source

I. INTRODUCTION

BECAUSE the technologies of 3C including computer, control, and communication are researched and developed in large quantities and proposed for human living. The needs of memory volume are more and more in software and hardware. The logical levels of traditional memory device with "0" and "1" levels are not enough, which is encoded to the two bits memory. In this paper, the logical level of above two bits is proposed to fabricate high volume memory. The logical device with multiple level values is so called multiple value logical

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level (MVLL) system, including logical gates, oscillator, decoder, counter, convertor etc. To produce well-defined memory device, the basic elementary of resonant tunneling devices (RTD) applied in MVLL system, plays an important role in completion of memory function. The literatures have proposed memory systems [1-5], high frequency systems [6-10], encoding and decoding systems [11-15] by the use and design of traditional circuit. The previous proposed MVLL system is not yet discussed in active load application of system and optimum of logical levels. In this paper the active load of constant current source and capacitance effect are studied in detail.

II. RESEARCH THEORY

The MVLL system is fabricated by using traditional semiconductor RTD (TSRTD) early. The TSRTD, although, possesses high performance properties in peak to valley current density ratio (PVCDR) value and peak current density (PCD) value [16-19], the fabrication cost and fabrication technique of TSRTD is expensive, complex and dangerous, respectively. The source materials of TSRTD would be with pollutant in living environment, which is including III-V or II-VI organic and metal compound mostly. The rare and contaminate of source material are the predicament of TSRTD in future. This paper proposes the RTD structure with composition of electronic elements, but not the use of semiconductor devices. The TSRTD is substituted by electronic elements, which is constructed by the electronic circuit with negative differential resistance (NDR) characteristic. The electronic elements with RTD property are so-called resonant tunneling electronic circuit (RTEC) element. The parameters of RTEC element would be designed to produce the phenomena of double PVCDR and triple PVCDR in NDR characteristic in this research. The NDR characteristic of RTEC element is defined by equation (1).

$$R_{NDR} = \frac{dv_N(i_N)}{di_N} = \frac{v_{n+1} - v_n}{i_{n+1} - i_n} \tag{1}$$

where the v_N and i_N are the voltage and current of RTEC element, respectively. The R_{NDR} is the negative differential resistance of RTEC element. v_{n+1}, v_n, i_{n+1}, and i_n are the variables of RTEC current and RTEC voltage. The nonlinear and negative differential characteristics of NDR curve can be expressed in the equation, which the equation will be applied in the simulation of RTEC element and MVLL system. The piecewise I-V curve of NDR characteristic is also the

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simulating technique for solving the nonlinear system in RTEC element. The RTEC element is constructed by using resistors and transistors. The NDR-like phenomenon in RTEC element is similar with the NDR curve in TSRTD. The RTEC element, therefore, will be suitable in application of MVLL system. Fabrication of such MVLL system with traditional electronic element by integrated circuit technology will be easier than of TSRTD. The schematic diagram of RTEC element is shown in Fig.1.
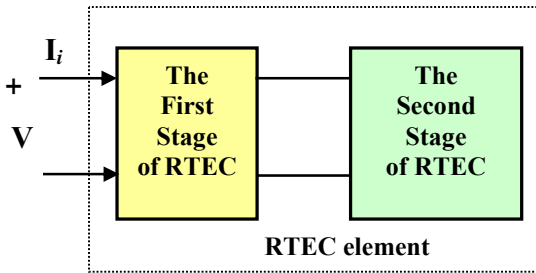

Fig.1 Schematic diagram of RTEC element

There are two electronic circuit stages which are arranged in RTEC element. The first stage is including three resistors and one transistor which constructed the resistance bias transistor circuit. The first stage is with I-V characteristic of positive slope which the transistor is the "on "state but the transistor at the second stage is "off" state at the same time. When the applied bias voltage is increased slightly, the transistor of the first stage turns "off" state and the transistor of the second stage turns "on" state, which the I-V characteristic of RTEC exhibited the NDR region. The PVCDR value and PCD value of RTEC element are decided by the resistance of two electronic circuit stages. The suitable selection of resistances in RTEC will produce optimum NDR curve which the PVCDR value is maximum, PCD value is also maximum, and the three PVCDR curves are similar each other in triple PVCDR RTEC. I-V characteristic of triple PVCDR RETC possessed obvious three NDR curves, but the PVCDR value and PCD value are less than those in double PVCDR RTEC element and single PVCDR RTEC element because of load effect and inference effect. The parasitic effect is not considered in this paper, because a paralleled capacitance will be added in this study to understand its influence in logical level of MVLL system. The MVLL system is built using RTEC element with an active load, which active load can decline the load effect and volume of MVLL system in integrated circuit, as indicated in Fig. 2.

The RTEC element with passive load or active load can organize a MVLL system. The operation region for logical level of MVLL system with passive load is smaller than that with active load. The passive load is generally the resistance, metal oxide semiconductor field effect (MOSFET), and RTEC element, which would be connected with RTEC element. The passive loads can be fabricated by integrated circuit fabrication process, but the load effect of passive loads in MVLL system is obvious. The active load such as current source or voltage source will produce low load effect in MVLL system, which results in large noise margin of logical levels. The current

steady state equation of MVLL system with active load can be described in equation (2),

$$\frac{dv_N^2}{dt^2} + A(R_{NDR})\frac{dv_N}{dt} + B(R_{NDR})v_N = C(R_{NDR}, i_N) \quad (2)$$

where the v_N and i_N are the voltage and current of RTEC element in time variable. The R_{NDR} is the negative differential resistance of RTEC element. A, B, and C are the variables of RTEC current and negative differential resistance R_{NDR}. The parasitic elements including series resistance, series inductance, and parasitic capacitance are also considered in this calculation. In this research, the MVLL system adopted the constant current source as the active load. The logical level is also studies in MVLL system with use of constant current source load, which is easily fabricated by using fabrication process of integrated circuit.
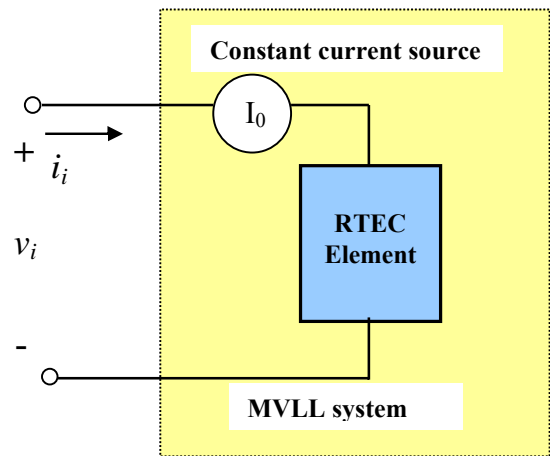

Fig.2 Schematic diagram of MVLL system using RTEC element with an active load

III. RESEARCH METHOD

The multiple PVCDR RETC elements are used to complete the MVLL system in this paper. The RTEC element is composed with two transistor stages including the first transistor stage with positive differential resistance characteristic and the second transistor stage with negative differential characteristic. Every stage is including controlled resistors which the resistors play an important role for logical levels of MVLL system. The "on" and "off" states of transistors in the RTEC stages are exhibited the "high" logical level and "low" logical level in the MVLL system. Three single PVCDR RTEC elements can compose one triple PVCDR RTEC element, which the triple PVCDR RTEC element is with three PVCDR values. The three well-defined PVCDR curves will enhance the property of MVLL system. In the triple PVCDR RTEC element, the three single PVCDR RTEC elements are either paralleling in or series with each other, which different modes are with different triple PVCDR curve. The optimum resistors in the triple PVCDR RTEC element are confirmed in regular to obtain the balance and similar PVCDR

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characteristics in every NDR curves. The PVCDR value and PCD value of single PVCDR RTEC element is better than those of every NDR characteristics of triple PVCDR RTEC element. In this research, the MVLL system using triple PVCDR RTEC element is improved by improvement of NDR characteristic of triple PVCDR RTEC element. The RTEC element with optimum NDR characteristic is used to design the MVLL system, as shown in Fig.3. The constant current source is as active load of the triple PVCDR RTEC element, so as to the MVLL system is constructed. The constant current source is composed by MOS FET and bipolar junction transistor (BJT) elements. The constant current source can be fabricated by using integrated circuit fabricated technology. The applied bias voltage in the MVLL system is directly applied in series with constant current source and triple RTEC element. The alternate current (AC) input signal is applied in order to observe the multiple logical levels output. The pulse generator and switching element are arranged in order to monitor the signal of multiple logical levels.
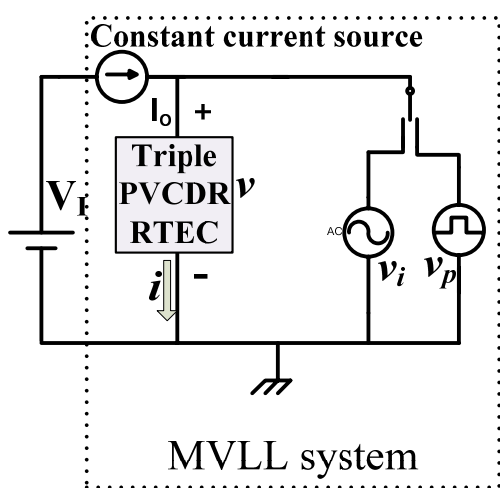

Fig.3 MVLL system using triple PVCDR RTEC element
with an active load

In Fig.3, three NDR curves will be represented due to the circuit design of triple PVCDR RTEC element. The single PVCDR RTEC element is just with the function of producing one NDR curve. The characteristic of single NDR curve is not properly developed in fabrication of the MVLL system of multiple values. The single NDR curve of RTEC element, crossed with load line, will result in only two logical levels, which is the same as the traditional logical gate, but the logical gate using RTEC element will possess faster switching speed than traditional logical gate. The single NDR characteristic of single PVCDR RTEC element is with high output power, because of its high PCD output value, although the NDR curve is a single alone. Characteristic of two NDR curves is exhibited to apply it in double PVCDR RTEC element. The output power of double PVCDR RTEC element with double NDR curve is less than that of single PVCDR RTEC element, because of lower PCD output value of every NDR curve in double PVCDR RTEC element, although it possesses two NDR curves. In this study, the triple PVCDR RTEC element is studied as a

research structure, because the number of NDR curve are important for MVLL system, but not PCD output value. The detail research of MVLL system, in this paper, is to understand the influence of capacitance effect in logical phenomenon. System diagram of Fig. 3 in MVLL system using triple PVCDR RTEC element is propose in this paper.

IV. RESULTS AND DISCUSSION

The triple PVCDR RTEC element is developed with three NDR curves, as indicated in Fig.4. The triple PVCDR RTEC element is composited using bipolar junction transistors and resistors, which is constructed with two transistor stages in every single PVCDR RTEC element, as above statement and exhibition of Fig.1.

Fig.4 shows the three similar NDR curves with both high PVCDR value and PCD value. The PCD values and valley VCD values in the three NDR curves are all about 3.5 A and 0.8 A, respectively. The PV values in three NDR curves are 0.40 V, 0.82 V, and 1.35 V, respectively. The VV values in the three NDR curves are 0.61 V, 1.07 V, and 1.69 V, respectively. The PVCDR values in the three NDR curves are calculated by equation (3).
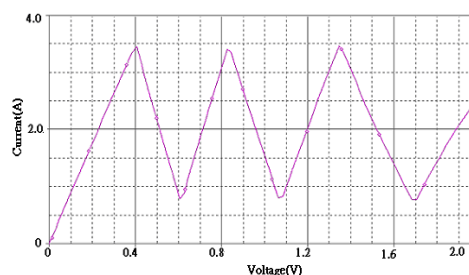

Fig.4 I-V characteristic of triple PVCDR RTEC element
with three NDR curves

$$\text{PVCDR value} = \frac{\text{PCD value}}{\text{VCD value}} \qquad (3)$$

All PVCDR values are about 4.4, after the equation (3) is calculated, in three NDR curves, respectively. The PVCDR value at above calculation is normal for RTEC element with three NDR curves, which should be less than either double NDR curves or single NDR curve in RTEC element. In this research, the similar three NDR characteristics in triple PVCRD RTEC element is because of suitable regulation and selection of resistors in RTEC elements, which is the optimum NDR characteristic for the triple PVCDR RTEC element, applied in MVLL system. The PCD value of 3.5 A in triple PVCDR RTEC element is better than that of other RTD element, which value can be applied in high power MVLL system. Lower VCD value about 0.8 A is contributed in the high PVCDR value. The low VCD value in TSRTD is because of low thermal current, but the low VCD value in triple PVCDR RTEC element is because of suitable selection of resistors. The PV value of triple PVCDR RTEC element is less than 1.35 V, which there is a benefit in the commercialization

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of RTEC element, because of low power consumption in element. Because of the critical NDR curves in triple PVCDR RTEC element, the fabricated MVLL system using triple PVCDR RTEC element will produce equidistant logical level. The equidistant level of logical state is important for the logical system.

In this work, the triple PVCDR RTEC element is used to design the MVLL system. The logical level of MVLL system is exhibited in Fig. 5. The logical levels are about 0.2 V, 0.8 V, 1.5 V, 2.2 V, 1.3 V, 0.8 V, and 0.2 V from low voltage to high voltage and then back to low voltage in half cycle of sinusoid wave in MVLL system. The logical levels of basic MVLL system are not flagrant contrast in voltage output. The number of logical level from low voltage to high voltage reaches four levels, which values be completed critiaclly. The number of logical level from high voltage back to low voltage is also four levels. The maximum voltage value V_{max} of input sinusoid wave is ±2 V. Fig. 5 also shows the sinusoid wave (V_{max} = ±2 V) with logical levels approximately, but the logical pattern is not regular, because of the parasitic effect, which results in current charge and current discharge phenomena.
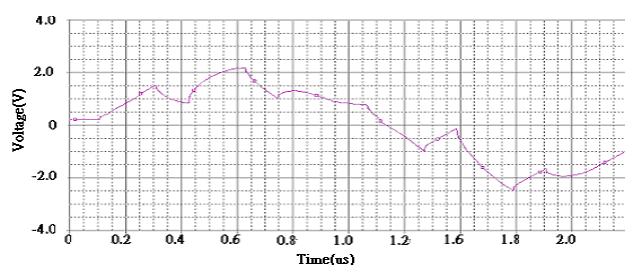

Fig.5 Logical characteristic of MVLL system using basic triple PVCDR RTEC

The charge and discharge phenomena will make the logical levels of input sinusoid wave transmogrification. Eventually, the noise margin of logical levels will be depressed unexpectedly. The noise margin of logical level is significantly a critical factor for the well-defined MVLL system. The noise margin is defined by the difference between input voltage and output voltage in the same logical level either in "high" level or in "low" level. The more irregularity is, the more noise margin is. The high noise margin will engender the liable blunder in the digital signal transmission of communication system. The regularity of logical level in MVLL system is more serious for application of digital signal process. In this basic system, the differences of between logical levels are respectively 0.6 V, 0.7 V, 0.7 V, 0.9 V, 0.5 V, and 0.6 V. The average value of level differences between logical levels in four levels MVLL system is about 0.67 V, which is less than that in traditional two bits system about 2.0 V. However, as the high level outputs both in traditional two bits system and in four levels MVLL system is the same as 2.0 V, although the difference of logical levels in four levels MVLL system is certainly less than that in traditional two bit system, the logical levels of MVLL system is more than that of traditional two bit system. In this MVLL

system, therefore, the difference of between four logical levels is much important to identify the reliable signal transmittance. In this research, the voltage difference of logical levels about 0.67 V is more than the noise margin of traditional two bit system about 0.4 V, therefore the four logical levels MVLL system can be applied in current digital logical system. For example, output voltage of the second logical level about 0.8 V is considered to discuss noise margin as below. When the noise margin is considered after the second logical level is imported, the output voltage is decided about 0.8 V±0.4 V, which is less than the third logical level of 1.5 V and more than the first logical level of 0.2 V, as presented in Fig. 6. It is a well-defined four logical levels MVLL system, as completed in this paper. The maximum output value of level 2 is exceed the minimum output value of level 3, and the minimum output value of level 2 is above the maximum output value of level 1 in Fig. 6, but the noise margin percent (NMP), as expressed in equation (4), is larger than the traditional two bit system.

$$NMP\,(\%) = \frac{noise\ margin}{input\ signal} \times 100\% \qquad (4)$$

The NMP value of traditional two bit system is 20%, but the MNP value of four levels MVLL system in second logical level is 50%. The NMP value of four levels MVLL system satisfies the critical NMP condition for tradition two-bit system. The output level of four levels MVLL system is represented in Fig. 7. The NMP values are respectively 20%, 30%, 40%, and 50% in four levels MVLL system. If the output value is larger than input level, the well-defined and critical four levels MVLL systems will be in accord with the logical specification.
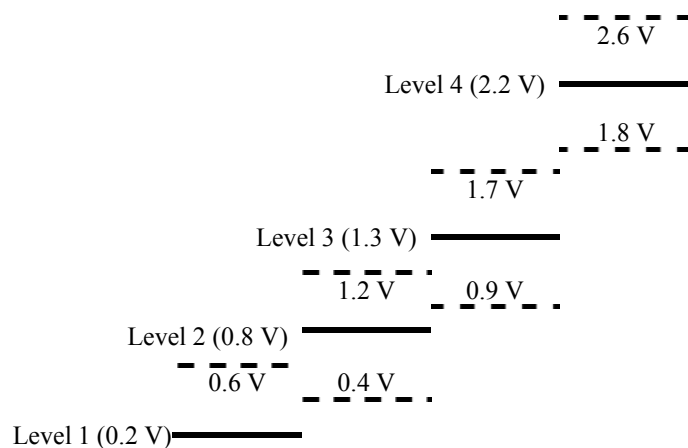

Fig. 6 Well-defined logical levels in MVLL system. (Dash line is maximum output and minimum output values. Solid line is input value)

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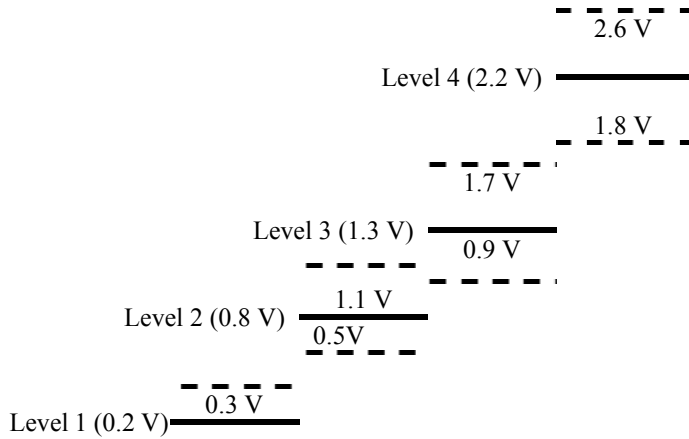International Journal of Electronics and Communication Engineering
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Fig. 7 Critical logical levels of four levels MVLL system. (Dash line is maximum output and minimum output values. Solid line is input value)

The outstanding result of four levels MVLL system in this research has been stated as above. The critical output of four logical levels in MVLL system fulfills the specification of noise margin in digital logic circuit. However, the logical levels of well-defined four levels MVLL system are unstable state in time domain as shown in Fig. 5. The well-defined four levels MVLL system must be improved to acquire stable and regular logical output. The ameliorations logical stability and logical regularity are proposed in Fig.8.
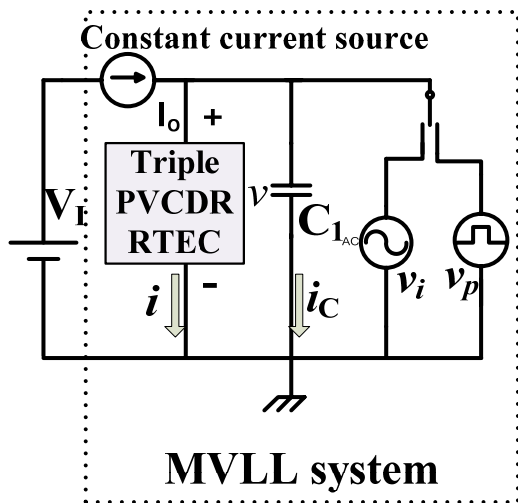
Fig.8 Improved critical four levels MVLL system using basic triple PVCDR RTEC

The capacitance is recommended into the well-defined four levels MVLL system to achieve explicit logical levels. The acceded capacitor is paralleled in the triple PVCDR RTEC. The capacitor is about 200 μF. Because of the appropriate culling of capacitance in MVVL system, the whole MVLL system with capacitor would be integrated both in one chip and in silicon foundry. The influence of capacitor in fabrication of MVLL system is scarce, but the function of capacitor in MVLL system

is hinge. The paralleled capacitor although likes the parasitic element of triple PVCDR RTEC element, the proper capacitance value in the MVLL system must be explored to acquire well improvement in stability and regularity of logical level. By way of strict exploration, the capacitance value will be prudently decided.The logical characteristic of improved critical four levels MVLL system using basic triple PVCDR RTEC is demonstrated in Fig. 9. The adopted input signal is also sinusoid wave with maximum voltage of 0.23 V. In this improved MVLL system, the remarkable logical characteristic with four significant stable logical levels about 220 mV, 223 mV, 228 mV, and 230 mV are appeared. The output voltage value of logical levels is notwithstanding tiny. The difference of between logical levels is slightly in variety. The stability and articulation of logical levels are outstanding. This logical levels diagram shows the significance of paralleled capacitor to improve the MVLL system. The input of alternating current (AC) for capacitor plays important roles in circuit analysis. The capacitor is the bypass capacitor of amplification circuit and charged capacitor of instantaneous state circuit in the improved MVLL system. The capacitor combines the triple PVCDR RTEC element with transistors and resistors, which results in the stable output of RTEC element and filtration of direct current (DC) signal in MVLL system. As a result, the logical image of improved MVLL system is better than of basic MNLL system. The less logical output level for improved MVLL system may be meliorated by the involvement of amplification circuit. In addition, the level difference of between logical levels is also reformed by appropriated adjustment of passive element values in RTEC element. On the whole, the most difficult problem is the stability of logical level in MVLL system, but not regularity of logical level and the high voltage level. The stability and controlling of logical level are settled by put capacitor into the basic MVLL system.
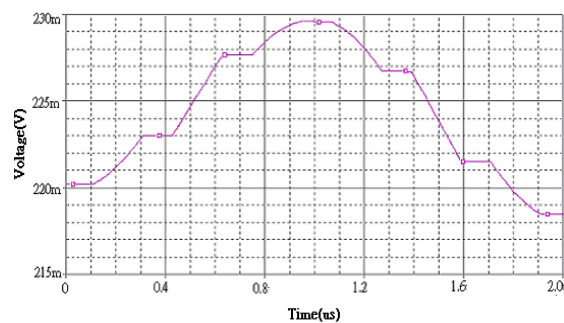
Fig. 9 Logical characteristic of improved MVLL system using basic triple PVCDR RTEC

Both MVLL systems are compared in the logical levels as shown in Table 1. The logical level of level 1 in both MVLL systems is almost similar, because the load effect of triple PVCDR RTEC element in the first stage is less. The NMP value of basic MVLL system without paralleled capacitor is smaller than that of the improved MVLL system with paralleled capacitor, because of high output level of basic MVLL system.

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TABLE I
LOGICAL LEVELS OF BOTH MVLL SYSTEMS WITH DIFFERENT CIRCUIT MODE

Logical level (mV) / MVLL system	Level 1	Level 2	Level 3	Level 4
Without capacitance	200	800	1,300	2,200
With capacitance	220	223	228	230

The improved MVLL system possesses the stable logical output level, which is more important for the aspect of general logical system. Table 2 shows the comparison of holding time in every logical level between both MVLL systems. In Table 2, the information of holding time in logical level, as defined in the maintaining time of every logical level, emerges the excellent achievement in improved MVLL system. The average holding time of improved MVLL system is approximately 0.14 µs. The holding time of improved MVLL system is distinctly better than of basic MVLL system about only 0.03 µs. The property of long holding time is to achieve the stable and exact logical output in logical system. The holding time of improved MVLL system is fourfold than that of basic MVLL system. The function of additional capacitor in the improved MVLL system is successfully discovered.

TABLE II
STABILITY OF BOTH MVLL SYSTEMS IN DIFFERENT CIRCUIT MODE

Holding time (µs) / MVLL system	Level 1	Level 2	Level 3	Level 4
Without capacitance	0.09	0.01	0.02	0.01
With capacitance	0.11	0.14	0.12	0.18

V. CONCLUSIONS

RTEC element of three similar NDR curves with both high PVCDR value and high PCD value are developed in this paper. The PCD values and VCD values of three NDR curves are all the same. The PV and VV values of three NDR curves are droopy, respectively. Also, the PVCDR values are all the same in three NDR curves. The PCD value in triple PVCDR RTEC element is better than other RTD element. The low VCD value contributes the high PVCDR value. The low VCD value is reached by suitable selection of resistors in triple PVCDR RTEC element. The low PV value of triple PVCDR RTEC element is a benefit in the commercialization of RTEC element. The logical output levels of input signal from low voltage to high voltage and then back to low voltage in half cycle of sinusoid wave in MVLL system are authenticated. The NMP value of four levels MVLL system satisfies the NMP condition of tradition two-bit system. The remarkable logical characteristic with four significant stable logical levels is appeared. The stability and articulation of logical levels are outstanding. The holding time of improved MVLL system is distinctly better than that of basic MVLL system. The property of long holding time is to achieve the stable and exact logical

output in logical system. The holding time of improved MVLL system is fourfold than that of basic MVLL system. The function of capacitor, added in the improved MVLL system, is discovered in serious.

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