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Three Dimensional MEMS Supercapacitor Fabricated by DRIE on Silicon Substrate

Wei Sun, Ruilin Zheng and Xuyuan Chen

***Abstract*—**Micro power sources are required to be used in autonomous microelectromechanical system (MEMS). In this paper, we designed and fabricated a three dimensional (3D) MEMS supercapacitor, which is consisting of conformal silicon dioxide/titanium/polypyrrole (PPy) layers on silicon substrate. At first, "through-structure" was fabricated on the silicon substrate by high-aspect-ratio deep reactive ion etching (DRIE) method, which enlarges the available surface area significantly. Then the SiO_2/Ti/PPy layers grew sequentially on the "through-structure". Finally, the supercapacitor was investigated by electrochemical methods.

***Keywords*—**MEMS, Supercapacitor, DRIE, 3D.

I. Introduction

SUPERCAPACITORS, including double layer supercapacitors and electrochemical supercapacitors, are being considered of various applications such as portable systems and vehicles [1-2]. For MEMS application, supercapacitors can not only couple with batteries to provide peak power, but also store energy from energy harvesting devices [3].

By using MEMS technology, Sung fabricated planar electrochemical supercapacitor with PPy electrodes on Si substrate [4]. Y. Q. Jiang fabricated a double layer supercapacitor utilizing vertically aligned carbon nanotube forests with 80 μm height on silicon wafer [5]. The 3D carbon nanotube forests enlarge the capacitance of the supercapacitor significantly because of increasing surface area of electrodes.

For both double layer supercapacitor and electrochemical supercapacitor, the most important parameter to affect the geometric capacitance (capacitance per unit substrate area) is the available surface area of electro-active materials. So far, research groups worldwide have mainly focused on increasing the surface area of electro-active materials themselves [6]. But there is much less attention on increasing the geometric capacitance of supercapacitor by structuring the supercapacitor with big effective surface area per unit volume of the structure. On silicon substrate, there are some methods to fabricate 3D structures by MEMS technologies. One way is by using LIGA-like technology based on thick resist photolithography and electroforming [7], another approach is based on carbon-MEMS [8], and the last method is using DRIE, which is very convenient high-aspect-ratio process with good quality [9].

In this study, a 3D MEMS supercapacitor was designed and fabricated by MEMS technologies, which included the most key step DRIE for "through-structure" etching, thermal oxidation for SiO_2 growing, RF sputtering for Ti current collectors depositing and electrochemical polymerization for PPy synthesis. Then the electrochemical behavior of the 3D MEMS supercapacitor was investigated.

Wei Sun is with the Institute for Microsystems Technology, Vestfold University College, Tonsberg, 3103, Norway, also with the School of Physics and Mechanical & Electrical Engineering, Xiamen University, Xiamen, 361005, China (phone: 0047-3303-7926; e-mail: wei.sun@ hive.no).

Xuyuan Chen is the corresponding author, with the Institute for Microsystems Technology, Vestfold University College, Tonsberg, 3103, Norway, also with the School of Physics and Mechanical & Electrical Engineering, Xiamen University, Xiamen, 361005, China (phone: 0047-3303-1161; e-mail: xuyuan.chen@ hive.no).

II. Design of 3D MEMS Supercapacitor

A. Design of 3D "Through-structure"

Fig. 1 shows the schematic drawing of the 3D "through-structure", the interdigitated beams provide much more effective surface area than similarly planar structure does for a same footprint. The 3D structure has two disconnected periodic beams as the substrates of anode and cathode respectively. Fig. 2 is the protection mask for DRIE. In where, the two "ears" will be used to separate anode and cathode after Ti sputtering. According to the 3D design, the surface area gain (AG) can be calculated by equation (1):

$$AG = s_{3D} / s_{planar} = 2(l + w_b + w_c)d / lw_b + 2 \quad (1)$$

where S_{3D}, S_{planar}, l, d, w_b and w_c are the surface area of the 3D substrate, the surface area of the similarly planar substrate, the length of the beam, the thickness of the wafer, the width of the beam, and the width of the "through-channel", respectively. In this study, l, d, w_b and w_c are respectively 0.99 cm, 525 μm, 100 μm and 100 μm. Thus the AG is 12.7.

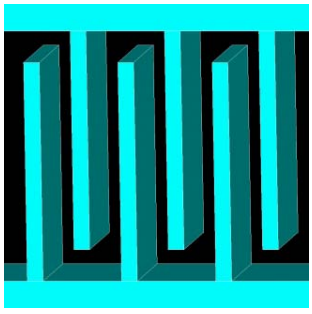


Fig. 1 Schematic drawing of the 3D "through-structure"

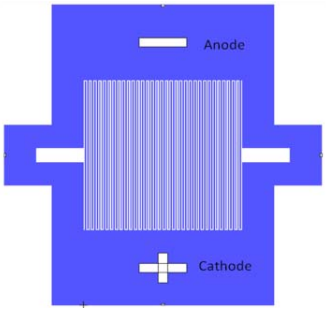


Fig. 2 Mask for DRIE protection

B. Design of Fabrication Processes Flow

The designed process flow for fabricating the 3D MEMS supercapacitor is shown in Fig, 3. At first, 300 nm Cr layer is deposited by RF sputtering on Si wafer and patterned by photolithography, then 2 μm Al film is thermal evaporated on the back side of the Si wafer as DRIE stop layer. Secondly, DRIE is carried out to etch through the whole thickness of the wafer, and then the metal Al and Cr are etched after dicing. Thirdly, the formed 3D "through-structure" is thermal oxidized to form a SiO_2 layer as insulator. Fourthly, conformal Ti current collector is RF sputtered, and then divided into anodic and cathodic current collectors by etching the Ti on the "ears" which is shown in Fig. 2. Finally, PPy electro-active materials are electrochemical deposited on the Ti collectors as anode and cathode respectively.

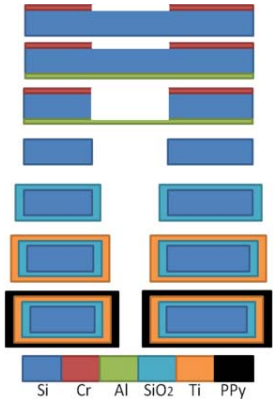
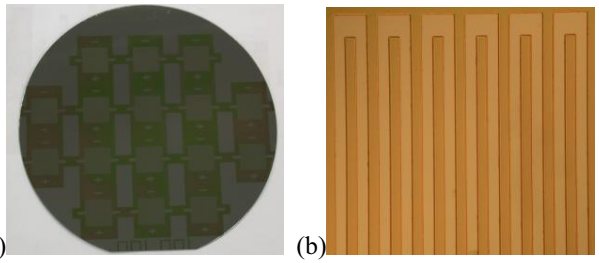


Fig. 3 Processes flow for fabricating 3D supercapacitor

III. Experimemtal

According to the design, we successfully developed the processes for fabricating the 3D MEMS supercapacitor. Because "Etching through" is a long time job, partterned Cr layer was used instead of SiO_2 as the DRIE protection mask, Fig. 4 presents the photos after Cr protection layer patterning. The key step DRIE was carried out on AMS200 (Alcatel, France) by using SF_6 as etching gas and C_4F_8 as passivation gas. We achieved a about 7μm min^{-1} etching speed in the first 30 minutes, then "black silicon" with the grass-like silicon occurs on both side wall and bottom of the being etched channel. Fig. 5 presents the side wall morphology with "black silicon", we can see that the length of the "grasses" is at the level of hundreds of micrometers. The "black silicon" is result from the big etching area (in Fig. 4(a)), in where the amount of heat produced and cannot dissipate immediately. The "black silicon" can be eliminated by changing the composite of etching gas, but the etching speed became slow significantly.



(a) (b)

Fig. 4 Photos after Cr patterning (photoresist was not removed), (a) the whole wafer; (b) part of single cell

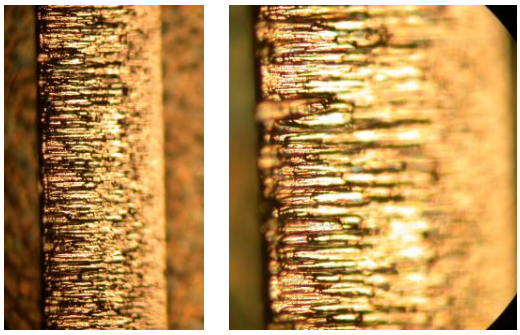


Fig. 5 Morphology of "black silicon"

It is well known that the lag effect always accompanying when the width difference of etching area exists. In our experiment, the lag effect is about 12.95% (as shown in Fig. 6).

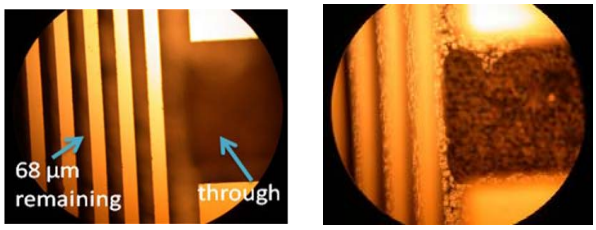
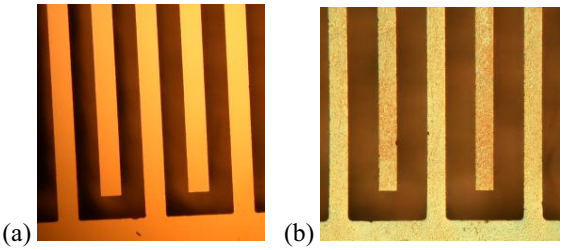


Fig. 6 Lag effect of DRIE

The total time is 210 minutes to etch the unprotected area through the whole thickness of the wafer. Fig. 7(a) gives the photo of single cell with "through-structure" after dicing. It can be seen the channel is extremely vertical.



(a) (b)

Fig. 7 "Through-structure", (a) after DRIE; (b) after coarsening

After DRIE, the protection Cr layer and stopping Al layer were etched sequentially. Then the single cell was soaked in an isotropic etching solution $HF/HNO_3/HAc$ to reduce the stress at edge and coarsen the surface of all effective surfaces (Fig. 7(b)).

A layer of SiO_2 with the thickness of 1.5 μm formed on all the effective surfaces of the 3D structure as insulator. Then 400 nm Ti layer was sputtered and divided into anodic and cathodic current collectors.

Finally, electro-active PPy films were electrochemical polymerized on current collectors as anode and cathode respectively. The preparation solution contained Pyrrole (Py) monomer and sodium *p*-toluenesulfonate as supporting salts.

IV. Electrochemical tests

Cyclic voltammetry (CV) and electrochemical impedance spectroscopy (EIS) were used to investigate the electrochemical properties of the 3D MEMS supercapacitor. The tests were performed on electrochemical workstation (Solartron 1260) in a two-electrode system with the two PPy electrodes as work electrode and counter electrode respectively in1M KCl solution.

Fig. 8 presents the CV curve of the 3D supercapacitor with the potential range from 0.0 V to 1.0 V at the scanning rate of 20 mVs^{-1}. The shape of the curve is rectangle-like which means good supercapacitor behavior. The geometric charge capacitance (C_{charge}) and discharge capacitance ($C_{discharge}$) of the 3D supercapacitor can be calculated by integrating the current of the CV curve in the half charge cycle and half discharge cycle, respectively. Here, 0.033 Fcm^{-2} C_{charge} and 0.026 Fcm^{-2} $C_{discharge}$ were obtained. Thus, the Coulombic efficiency equals $C_{discharge}/C_{charge}$, the value of 78.8%

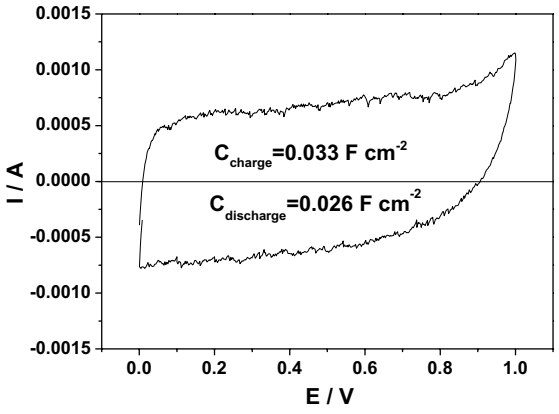


Fig. 8 CV of the 3D supercapacitor

The EIS data were acquired over a frequency range from 10 mHz to 100 kHz and with potential amplitude of 10 mV. Fig. 9 presents the EIS curve and the modeling result fitted by equivalent circuit which is shown as insert in Fig. 9. In high frequency area, a depressed semi-circle is observed, which implied the charge transfer performance at the interface between electrode and electrolyte. While in low frequency area, the diffusion of charge in the polymers dominated which results in straight lines on impedance. Table 1 gives the value of each element in the equivalent circuit. The sum of R_1 and R_2 means the internal resistance of the 3D supercapacitor, with the value of 26.20 ohm cm^{-2}. Two constant phase elements CPE_1 and CPE_2 instead of capacitance C describe the capacitance properties of the 3D supercapacitor. The magnitude of CPE_1 and CPE_2 are 0.0012 and 0.028, which means the doping/undoping of ions made much larger contribution on the geometric capacitance of the 3D supercapacitor. The total geometric capacitance is 0.029 Fcm^{-2}. The geometric power density P can be calculated by equation (2),

$$P=0.5CU^2/t-I^2(R_1+R_2) \quad (2)$$

where I is the reactive current in CV, U is the potential window of CV, t is the discharge time of each cycle. When the scanning rate of CV is 20 mVs^{-1}, the geometric density P is 0.281 $mWcm^{-2}$.

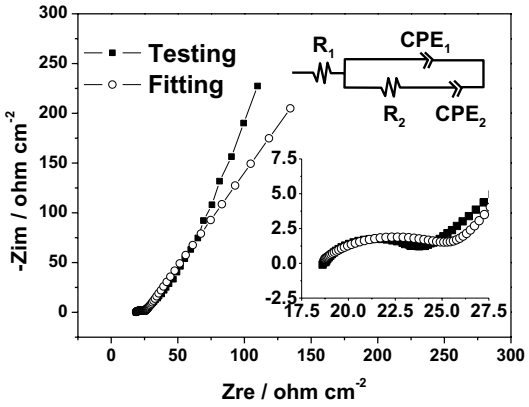


Fig .9 EIS of the 3D supercapacitor

TABLE I
Parameter of elements in equivalent circuit

Element	Value	Error%
$R_1(ohm/cm^2)$	18.45	1.55
$CPE_1(Fs^{1-\alpha\,1}/cm^2)$	0.0012	50.45
α_1	0.57	11.01
$R_2(ohm/cm^2)$	7.75	8.41
$CPE_2(Fs^{1-\alpha\,2}/cm^2)$	0.028	2.34

From the EIS, we can also calculate the diffusion coefficient of the doping ions D by using the "finite diffusion model" as equation (3) [10],

$$D=L^2/3R_LC_L \quad (3)$$

L is the thickness of PPy film, about 10μm here, R_L is the limiting resistance of the PPy film, which can be determined by equation (4), C_L is the limiting capacitance, which is determined by equation (5).

$$R_L=R-R_1-R_2 \quad (4)$$

$$1/C_L=d(-Z_{im})/d(\omega^{-1}) \quad (5)$$

In equation (4), R is the total resistance, extrapolated to very low frequencies. When the frequency is 10 mHz, R equals 109.8 ohmcm^{-2}, thus R_L is 83.6 ohm cm^{-2}. Fig. 10 presents the linear ($-Z_{im}/\omega^{-1}$)-plots, from which C_L is calculated as 0.080 Fcm^{-2}. Thus, the value of the diffusion coefficient D is 4.98×10^{-8} cm^{2}s^{-1}. And the value of $3R_LC_L$ is the time constant τ, equals 20.06 s. So, the critical scanning rate for CV tests is U/τ, equals 49.8 mVs^{-1}.

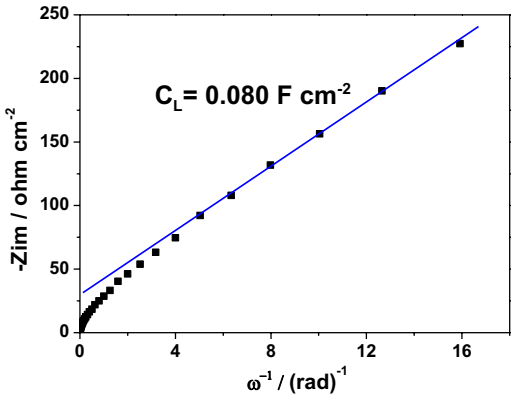


Fig. 10 $-Z_{im}$ vs ω^{-1} of EIS data

V. Conclusions

MEMS supercapacitor consisting of SiO_2/Ti/PPy conformal layers on 3D interdigitated silicon structure was fabricated successfully by MEMS technologies. DRIE is the key step which enlarged 12.7 times effective surface area for electrodes of the supercapacitor compared to corresponding planar structure. The 3D MEMS supercapacitor was investigated by CV and EIS methods. The results show our supercapacitor has geometric capacitance of about 0.03 Fcm^{-2}, with the Coulombic efficiency of 78.8% at the CV scanning rate of 20 mVs^{-1}. From the EIS test, we found that the inner resistance of the supercapacitor is 26.2 ohmcm^{-2}, the diffusion of ions in PPy film dominated the geometric capacitance, and the geometric power density is 0.281 mWcm^{-2}. By analyzing the EIS data, we also found the diffusion coefficient of doping ions was 4.98×10^{-8} cm^{2}s^{-1}, while time constant was 20.06 s. So our supercapacitor can be used at about 50 mVs^{-1} discharge rate and discharge completely. Our 3D MEMS supercapacitor is promising in MEMS application, especially in where high power is required.

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