World Academy of Science, Engineering and Technology
International Journal of Electronics and Communication Engineering
Vol:4, No:8, 2010

Estimation Of Attenuation And Phase Delay In Driving Voltage Waveform Of A Digital-Noiseless, Ultra-High-Speed Image Sensor

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Open Science Index, Electronics and Communication Engineering Vol:4, No:8, 2010 publications.waset.org/11926/pdf

Abstract—Since 2004, we have been developing an in-situ storage image sensor (ISIS) that captures more than 100 consecutive images at a frame rate of 10 Mfps with ultra-high sensitivity as well as the video camera for use with this ISIS. Currently, basic research is continuing in an attempt to increase the frame rate up to 100 Mfps and above. In order to suppress electro-magnetic noise at such high frequency, a digital-noiseless imaging transfer scheme has been developed utilizing solely sinusoidal driving voltages. This paper presents highly efficient-yet-accurate expressions to estimate attenuation as well as phase delay of driving voltages through RC networks of an ultra-high-speed image sensor. Elmore metric for a fundamental RC chain is employed as the first-order approximation. By application of dimensional analysis to SPICE data, we found a simple expression that significantly improves the accuracy of the approximation. Similarly, another simple closed-form model to estimate phase delay through fundamental RC networks is also obtained. Estimation error of both expressions is much less than previous works, only less 2% for most of the cases . The framework of this analysis can be extended to address similar issues of other VLSI structures.

Keywords—Dimensional Analysis, ISIS, Digital-noiseless, RC network, Attenuation, Phase Delay, Elmore model

I. Introduction

ETOH et al. [1]- [2] developed a CCD image sensor for ultra high speed continuous image capturing. Its ultrahigh-speed shooting capability of 1,000,000 fps was made possible by directly connecting CCD storages, which record video images, to the photodiodes of individual pixels. The number of in-situ storage elements was more than 100 enables storing more than 100 consecutive frames at the speed of 1 Mega-frames per second (Mfps). Charge packets generated at each pixel are transferred to each storage area and simultaneously recorded at all pixels. The sensor was named the ISIS, the In-situ Storage Image Sensor.

With financial support from Japanese government, the authors have been designing much higher frame rate (100 Mfps and more) as well as high sensitivity for biological applications [3]- [5]. Currently, the most challenging task to achieve such high frame rate is attenuation and phase shift of driving voltages to drive the CCD caused by propagation delay within the sensor chip.

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For the next generation of ISIS, the authors have developed a digital noiseless transfer scheme with only sinusoidal waveforms for image capturing operation and a normal four-phase transfer scheme for read out operation [5].

To facilitate fast and accurate optimization of metal layout as well as pixel-based layout design, simple expressions to characterize attenuation and phase shift which capture high frequency effects are needed.

Utilizing a similar concept proposed by Dao et al [6] for attenuation of driving square waves, in this paper, the authors focus exclusively on RC trees that have constant series resistance, parallel resistance and capacitance, a commonly used model in CCD design. Elmore delay metric [7] for a fundamental RC chain was utilized as the first-order approximation, and dimensional analysis is applied to circuit simulator data to seek a simple expression to improve the accuracy. The expressions are also called - The Semi-Empirical Interconnect Model (SEIM).

II. Background

A. Delay and Attenuation Computation

Elmore metric [7], is the most widely applied interconnect delay metric. Given an RC tree circuit with n nodes $(i = 1, 2, ..., n)$, and corresponding resistor R_i and grounded capacitor C_i, Elmore delay at node i is given by:

$$T_{Di} = \sum_{k=1}^{N} R_{ki} C_k \tag{1}$$

where R_{ki} is the resistance of the unique path from input to node i that overlaps with the unique path between node i and node k and C_k is the capacitance at node k.

Though having simple expression, Elmore metric is known to give inaccurate delay results due to its nature of first-order moment approximation of the impulse response. To adjust the accuracy of Elmore model, different approaches have been presented. Some proposed correction coefficients by means of analytical method or empirical methods as listed in [8]. Some proposed higher order moments method which required extensive computation, known as model order reduction technique as in [9]- [11].

In this paper, the authors proposed a correction coefficient to improve the accuracy of Elmore model. The coefficient is a function of dimensionless numbers that are dependent on circuit parameters. This is an interesting extension to the work done previously also by the authors [6]. Similar works such as

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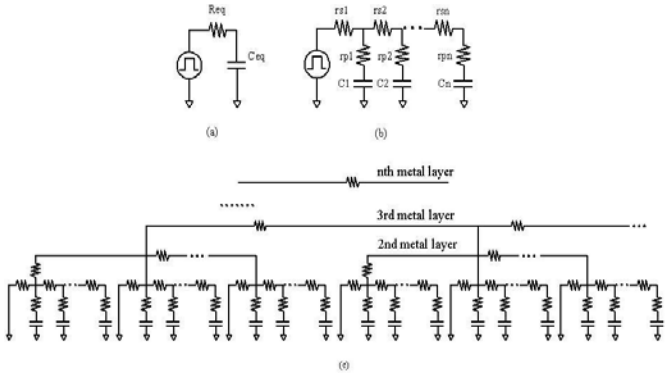


Fig. 1. Circuit structure (a) Equivalent RC circuit (b) Fundamental RC circuit (c) Multi-level RC circuit.

[8], [12] also utilized dimensional analysis for interconnect analysis.

Eventhough there are a lot of researches on delay calculation for a step or ramp input as listed in [7]- [13], not much work has been done for periodic type input in which the frequency effect must be considered when building necessary models. Celik and Pillegi [14] approximate amplitude response of a trapezoidal wave over RC(L) networks by a function of the fundamental frequency of the input signal and the second central moment.

B. Multi-level structure of the ISIS

CCD structure is usually represented by a multi-level model of the fundamental structure (b) as shown in Fig. 1(c). Parasitic capacitance of interconnects is neglected, since that of of polysilicon gate is dominant for CCD. We can adjust the total capacitance later by introducing a correction factor. Therefore, it is safe to use the model in Fig. 1(b) for evaluation of propagation delay of CCD structure.

Fig. 1(b) shows a fundamental RC chain circuit with series resistance r_S, parallel resistance r_P and grounded capacitor c. The fundamental model can be replaced by the electrically-equivalent model with equivalent resistance R_{eq} and capacitor C_{eq} as shown in Fig. 1(a). Similar steps are repeated depending on the number of metal layers of the ISIS. The final equivalent resistance and capacitance are used to balance the RC delay.

Interconnect model derived in this paper is based on the following assumptions:

(1) Uniformly distributed RC networks in Fig. 1(b) with constant r_S, r_P and c;

(2) Sinusoidal input waveform

(3) Performance evaluation is based on amplitude response and phase delay of the furthest-end node.

C. Digital noiseless transfer scheme

Due to its special architecture, ISIS can be operated independently during image capturing phase and read-out phase. Therefore, Vo Le et al [5] proposed a digital noiseless transfer scheme for image capturing operation to suppress electromagnetic noises.

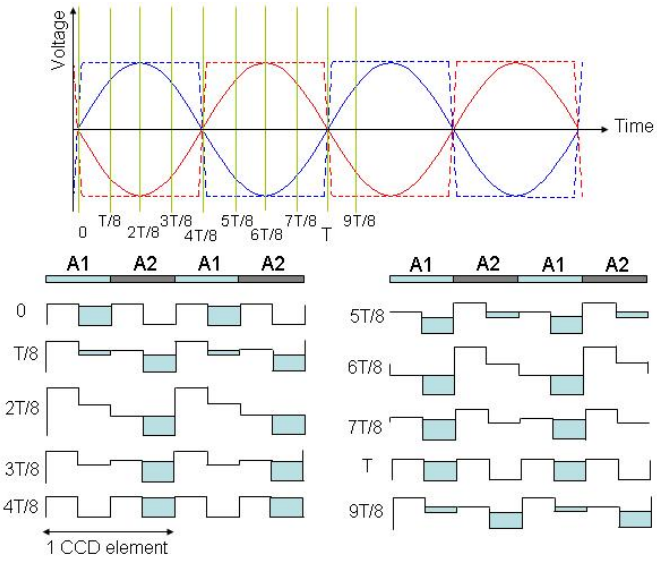


Fig. 2. Sinusoidal waveforms for a two-phase transfer CCD and transfer of electron packets

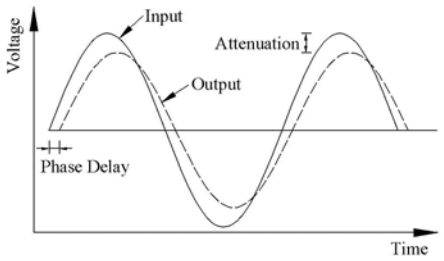


Fig. 3. Input-output pair under sinusoidal wave.

The dotted lines in Fig. 2 show a conventional two-phase transfer CCD with typical pulse train, duty cycle is exactly 50%. And the continuous lines show a newly proposed "digital noiseless transfer scheme" which employed two sinusoidal waveforms. The two waveforms are exactly complementary with a phase shift of half duty cycle, 180 degrees. Charge packets are transferred from under A1 electrode to A2 electrode. After one cycle, charge packets are completely transferred to the next CCD element. And the process repeats until the image capturing phase stops.

D. Dimensional Analysis

There are seven factors involved in evaluating attenuation of driving voltage from a fundamental RC chain as in 1(b) such as: parallel resistance r_P, series resistance r_S, grounded capacitance c, clock period T, input amplitude V_0, amplitude loss ΔV, number of sub-circuit segments n.

To reduce the number of governing parameters of the system and derive a generalized expression for the RC delay, parameters selected as "base" parameters are: n, r_S, r_P, c and T.

The following three dimensionless parameters are introduced:

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(1) Dimensionless amplitude loss (attenuation):

$$\overline{\Delta V} = \Delta V / V_0 \tag{2}$$

(2) Ratio of equivalent parallel resistance and series resistance:

$$A = \frac{R_P}{R_S} = \frac{2}{n(n+1)} \frac{r_P}{r_S} \tag{3}$$

(3) Ratio of the first-order approximation of RC delay (Elmore model) and clock period:

$$B = R_E C_E f \tag{4}$$

where f is the clock frequency. Thus, dimensional analysis results in the following dimensionless equation:

$$\Phi(\overline{\Delta V}, A, B) = 0 \tag{5}$$

While an explicit expression is more useful, we focus on finding the function:

$$\overline{\Delta V} = \Phi_1(A, B) \tag{6}$$

The functional relationship in equation (6) can be estimated through an equivalent circuit with the resistance Req and the capacitance C_{eq}, where: $C_{eq} = C_E = nc$.

The expression of Req is assumed as follows:

$$R_{eq} = \alpha(R_P + \beta R_S) \tag{7}$$

Then, our problem is reduced to obtain an expression of and in terms of dimensionless parameters A and B. They were determined experimentally by using a practical procedure described in the following section.

Theoretically, B can vary from 0 to ∞. However, if B is too small, attenuation becomes almost negligible, and if B is too large, signal becomes completely attenuated; both cases are of no interest for practical applications. Therefore, the range of B is fixed between 0.055 and 0.22 which corresponds to the one-side attenuation of 2.7% and 20.7% of input voltage amplitude of a single RC circuit shown in Fig. 1(a).

III. SEMI-EMPIRICAL INTERCONNECT MODEL (SEIM) FOR ATTENUATION ESTIMATION

A. Two extreme cases (A = ∞ or A = 0)

For $A = \infty (r_S = 0)$, we have an exact solution: $R_{eq} = R_P = r_P/n; C_{eq} = nc$. Therefore, $\alpha = 1$.

For A = 0 ($r_P = 0$), hence,$r_P = 0$, and from equation (7), we have: $R_{eq} = \alpha\beta R_S$. We can expect that the value of α distributes around unity, which is the exact solution for A = ∞. It is convenient for the following analysis if α can be fixed at a constant. Therefore, α is assumed to be one. Then, we searched for an expression of β with respect to B.

The coefficients were found by applying a curve fitting technique to fit SPICE data with a wide range of number of circuit segments (n) from 10 to 20,000 with different B. The result of β is as follows:

$$\beta = 0.0478B + 0.8148; 0.055 \leq B \leq 0.22 \tag{8}$$

We can see that when A = 0, $\alpha = 1, \beta$ is expressed almost solely in terms of B. In fact, Fig. 3 shows an excellent linear fitting result between SEIM and Spice data.

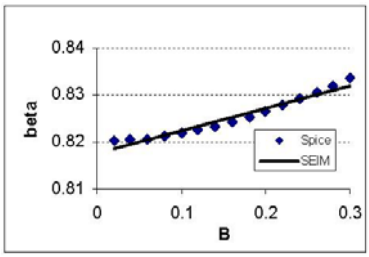


Fig. 4. β fitting result when A = 0

B. Fundamental RC trees ($A \neq 0 and A \neq \infty$)

The previous two extreme cases are used as "boundary conditions" to find the functional relationship in equation (7) for the whole range of A. For the general cases of A which distributes from 0 to ∞, we assume that expression of β with respect to B remains unchanged, and α changes around unity.

We employed the following expression to approximate the change of α with respect to A for $0 < A < \infty$ as follows:

$$\alpha(A) = 1 + aA^b e^{-cA}; a = a(B); b = b(B); c = c(B) \tag{9}$$

The coefficients a, b and c in equation (9) were found by using Powell conjugate minimization technique to fit SPICE data with a wide range of circuit at different combinations of $(n, r_S, r_P, c$ and $f)$ for different cases of B as shown in Fig. 4. Finally, we have a simple functional form of SEIM as follows:

$$\begin{aligned} R_{SEIM} &= \alpha(R_P + \beta R_S); \\ \beta = 0.0478B + 0.8148; &\alpha = 1 + aA^b e^{-cA}; \\ a &= 17.53B^2 - 3.31B + 0.22; \\ b &= 24.25B^2 - 4.87B + 0.65; \\ c &= 81.3B^2 - 16.47B + 0.97; \\ 0.055 &\leq B \leq 0.22; \end{aligned} \tag{10}$$

We can further simplify the expression of α by using the average values of α each case of B. Therefore, a simplified closed-form model is created, the Simplified - Semi Empirical Interconnect Model (S-SEIM).

$$\begin{aligned} R_{S-SEIM} &= \alpha(R_P + \beta R_S); \\ \beta &= 0.0478B + 0.8148; \\ \alpha_{S-SEIM} &= 0.0724B + 1.0138; \\ \text{where: } &0.055 \leq B \leq 0.22 \end{aligned} \tag{11}$$

Estimation errors of amplitude response of S-SEIM, SEIM, Elmore [7] and Celik [14] models are shown in Table I. SEIM and S-SEIM give much better results compared with Celik model.

IV. SEIM FOR PHASE DELAY ESTIMATION

Phase delay or phase shift is also an important factor besides signal attenuation. In the following section, the authors derive phase delay closed-form expression by employing similar approach.

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TABLE I
COMPARISON BETWEEN ESTIMATION ERRORS OF AMPLITUDE RESPONSE

n	B	Celik	SEIM	S-SEIM
5880	0.14	-23.4%	-0.7%	3.9%
1280	0.06	-1.0%	-0.1%	0.1%
720	0.11	-11.8%	-0.6%	1.0%
360	0.14	-22.9%	-1.4%	2.0%
144	0.06	-1.0%	-0.2%	0.3%
90	0.14	-24%	-1.0%	1.3%
10	0.11	-9.8%	-0.2%	1.3%

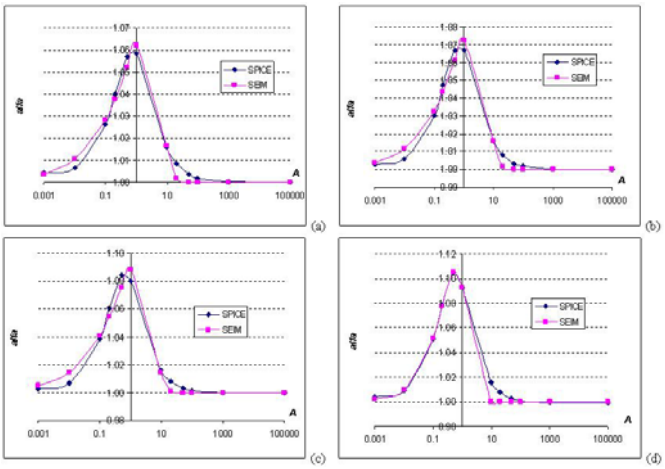


Fig. 5. α fitting result when B = 0.055(a); 0.11(b); 0.165(c) and 0.22(d).

A. Two extreme cases (A = ∞ or A = 0

For $A = \infty (r_S = 0)$, we also have an exact solution: $R_{eq} = R_P = r_P/n, C_{eq} = nc$. Therefore, $\alpha = 1$.

For A = 0 ($r_P = 0$), hence, $r_P = 0$, and from equation (7), we have: $R_{eq} = \alpha\beta R_S$. We can expect that the value of α distributes around unity, which is the exact solution for A = ∞. It is convenient for the following analysis if α can be fixed at a constant. Therefore, α is assumed to be one. Then, we searched for an expression of β with respect to B as follows:

$$\beta = 17.09B^2 - 1.55B + 1 \tag{12}$$

B. Fundamental RC trees ($A \neq 0$ and $A \neq \infty$)

When $0 < A < \infty$, we employed the following expression to approximate the change of α with respect to A as follows:

$$\beta = 17.1B^2 - 1.55B + 1; \alpha = 1 + aA^b e^{-cA};$$

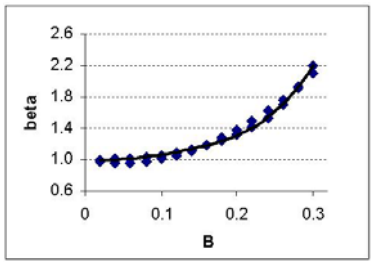


Fig. 6. β fitting result with delay approach.

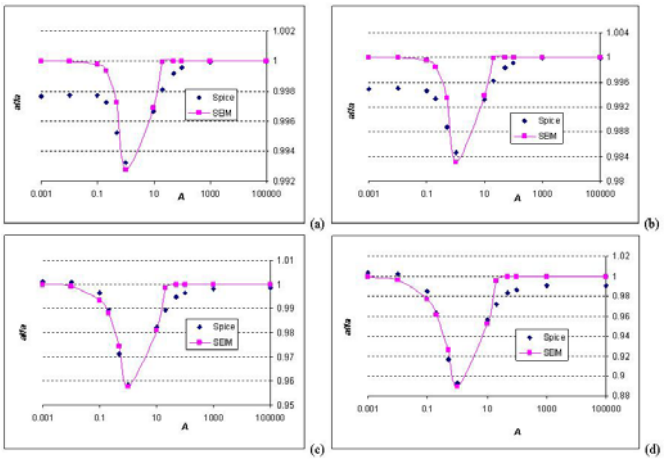


Fig. 7. α fitting result when B = 0.055(a), 0.11(b), 0.165(c) and 0.22(d) respectively

TABLE II
DELAY ESTIMATION ERROR FOR FUNDAMENTAL RC CHAINS WITH N =10

n	B	Elmore	SEIM	S-SEIM
5880	0.14	22.8%	-0.7%	2.8%
1280	0.06	4.5%	0.2%	0.9%
720	0.11	14.0%	-1.2%	2.3%
360	0.14	21.5%	-2.1%	3.3%
144	0.06	4.3%	0.2%	0.9%
90	0.14	20.5%	-1.7%	3.7%
10	0.11	12.0%	0.0%	2.6%

$$\begin{aligned} a &= 3.57B^2 - 0.11B - 0.006; \\ b &= -8.09B + 2.49; \\ c &= -2.12B + 0.74 \\ \text{where: } & 0.055 \leq B \leq 0.22 \end{aligned} \tag{13}$$

Similar to previous section, we can further simplify SEIM to S-SEIM by utilizing a constant value of α for each case of B and use a fitting curve to fit α as follows:

$$\begin{aligned} R_{S-SEIM} &= \alpha(R_P + \beta R_S); \\ \beta &= 17.1B^2 - 1.55B + 1; \\ \alpha_{S-SEIM} &= -0.9B^2 + 0.07B + 1; \\ \text{where: } & 0.055 \leq B \leq 0.22 \end{aligned} \tag{14}$$

Table 3 shows that S-SEIM gave better delay estimation results than Elmore model even with simplified format while Celik et al. [14] utilize Elmore delay as upper bound for their phase delay estimation.

V. Conslusion

We have derived simple, closed-form metrics for the phase delay and the attenuation in the responses of fundamental RC networks as a function of input clock frequency and dimensionless numbers. We have shown that combination of dimensional analysis with analytical approaches is a powerful

tool to address a complex physical phenomenon involved many parameters. Dimensional analysis helps to correlate physical parameters governing the phenomena. We only need to focus on a much smaller number of dimensionless numbers, from then, simple, closed form expression to express the phenomenon can be found.

Practically, with this paper and previous works on [6], the authors show that it is possible to derive attenuation and phase delay for any given input waveform type of a fundamental RC network.

Finally, it is worth noting that the proposed approach could be extended to address other issues in VLSI design by proper choosing of governing parameters to adjust some simple analytical model and apply mathematical fitting functions to reach a simpler expression yet keeping the fundamental importance of the problem.

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