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Low Voltage High Gain Linear Class AB CMOS OTA with DC Level Input Stage

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Abstract**—**This paper presents a low-voltage low-power differential linear transconductor with near rail-to-rail input swing. Based on the current-mirror OTA topology, the proposed transconductor combines the Flipped Voltage Follower (FVF) technique to linearize the transconductor behavior that leads to class-AB linear operation and the virtual transistor technique to lower the effective threshold voltages of the transistors which offers an advantage in terms of low supply requirement. Design of the OTA has been discussed. It operates at supply voltages of about ±0.8V. Simulation results for 0.18µm TSMC CMOS technology show a good input range of 1Vpp with a high DC gain of 81.53dB and a total harmonic distortion of -40dB at 1MHz for an input of 1Vpp. The main aim of this paper is to present and compare new OTA design with high transconductance, which has a potential to be used in low voltage applications.

Keywords**—**Amplifier class AB, current mirror, flipped voltage follower, low voltage.

I. Introduction

With the scaling down of CMOS technology and the increasing market for portable electronic equipment, the design of high performance low voltage low power analog circuits is becoming increasingly challenging with the persistent trend towards reduced supply voltages.

Thus, for a given technology, reducing the supply voltage can generally degrade the speed of conventional analog circuits. To accomplish these requirements, it is necessary to develop new design technique circuits with low voltage supply without loss of performance [1]-[3]. The operational transconductance amplifier (OTA) is an important bottleneck for various analog circuits and systems. It is widely used as active element in variable gain amplifiers, data converters, interface circuits, continuous time oscillators, switched capacitor filters and sample and hold circuits, etc [1], [4]-[6].

Depending on system needs, OTA circuit with high open loop gain, high slew rate and large bandwidth is highly desired. The high slew rate and bandwidth ensure a small settling time, whereas the high gain improves the settling accuracy [7]-[8]. Unfortunately, all these requirements are difficult to reach with class-A circuits since the maximum output current is limited by the bias current. Hence, a trade-off between slew rate and power consumption exists [5], [8]. To achieve these desired features, class-AB circuits are often employed. These circuits provide well-controlled quiescent currents, which can be made very low in order to drastically reduce static power dissipation. Traditionally, class-AB transconductors have been designed using two approaches: increasing the tail current of the input pair for large input signals or increasing the current at the active load of the differential input pair. However, a new category of class-AB single stage OTAs which boosts the current both at the differential input transistors and at the active load has been reported. These have been coined as "super class-AB OTAs" [9].

Another limiting factor for OTA performance is the linear output current range which is limited by the supply voltage. So, to provide an extended performance, we are interested in improving dynamic range techniques.

The most common method to achieve extended range is to use a complementary differential amplifier at the input stage [10]-[11]. This method uses a n-type and a p-type differential pairs simultaneously, where the currents of the two input pairs are summed and then sent to the next stage. Complex circuitry is usually required in these circuits to ensure that the sum of the g_ms of the two input pairs remains constant.

For simplicity and accuracy, it is better to use a single differential pair at the input. In this case, the common mode range of the input pair must be boosted to accept rail to rail inputs.

This paper presents a new approach based on the use of virtual transistor concept to improve input dynamic range. Hence, a new implementation of class-AB transconductance cell using this technique and suited for low voltage operation is obtained. Simulation results of the latter confirm enhancement in linearity input swing and frequency response.

II. Transconductor Circuit Description

A. Basic concept: Super class AB OTA

Given that the function of transconductor is a voltage to current converter, the most critical design requirement is to have high linearity with a good high frequency capability. It is possible to find many researches focusing on this feature. So, different techniques have been proposed to improve the linearity of MOS transconductors such as : source degeneration using resistors or MOS transistors [12]-[13], crossing-coupling of multiple differential pair [14]-[15], class-AB configuration [16]-[17], adaptive biasing [18]-[19],

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constant drain-source voltages [20]-[21], pseudo differential stages [22]-[23] and feed-forward technique [4], [24]. In this paper, we will focus on the use of class-AB stages since they may improve considerably the dissipation-speed trade off in analog circuits, as mentioned before.

One topology to implement a linear transconductor suitable for low voltage and low power operation is shown in Fig. 1. It is noted "super" class AB OTA in which a double current boosting technique is used : an adaptively biased differential pair [8] and an active load based on current mirrors whose gain is made dependent on their input current [8], [25].

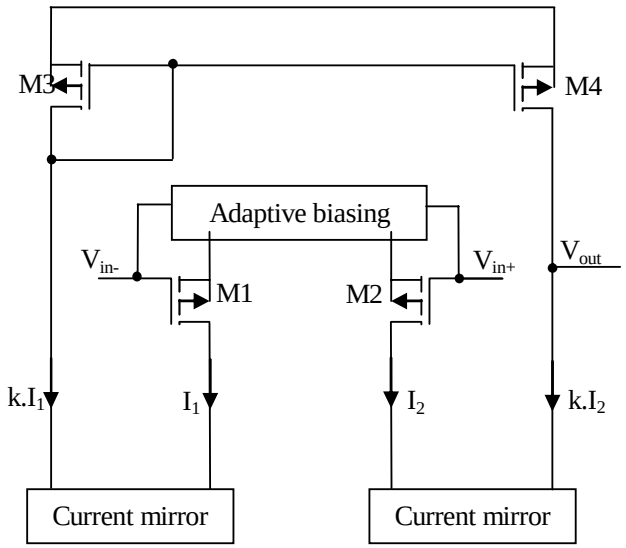

Fig. 1 Bloc diagram of super class AB OTA

Figure 2(a) shows the chosen adaptively biased input pair as proposed in [5], [8]-[9], [16]. It consists of two matched transistors M1 and M2 cross-coupled by two DC level shifters in order to keep constant sum of source to gate voltages.

The current drain of a conventional differential pair (M1 and M2) operating in saturation mode are given by

$$I_i = \frac{\beta_i}{2}(V_{SGi} - |V_{TP}|)^2 \quad (1)$$

where i=1, 2 denotes transistors Mi, $\beta_i = \mu_n C_{ox}(W/L)_{M_i}$ is the transconductance factor of transistors Mi and $|V_{TP}|$ is the threshold voltage of PMOS transistor.

Assuming $\beta_1 = \beta_2 = \beta$, the differential output current is defined as

$$I_d = I_1 - I_2 = \frac{\beta}{2}(V_{SG1} + V_{SG2} - 2|V_{TP}|)(V_{SG1} - V_{SG2}) \quad (2)$$

From the latter, to have a linear current I_d, the term $V_{SG1} + V_{SG2} - 2|V_{TP}|$ should be kept constant. An efficient way consists in integrating two floating DC voltage sources with values $V_B + |V_{TP}|$ as depicted in Fig. 2(a).

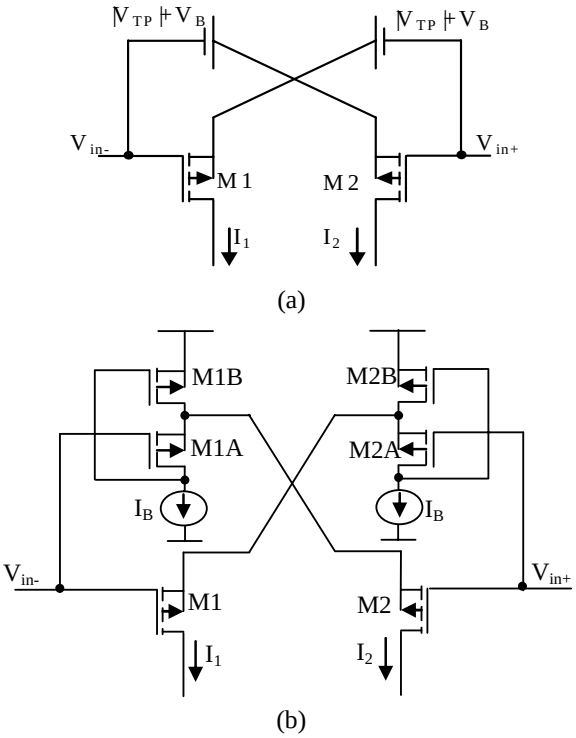

Fig. 2. Class AB input stage using cross coupled differential pair (a) diagram (b) implementation using FVF

From the loop around the input transistors, the relationship between V_{SG1} and V_{SG2} as a function of V_{in+} and V_{in-} are given by

$$\begin{aligned} V_{SG1} &= (V_{in+} - V_{in-}) + (V_B + |V_{TP}|) \\ V_{SG2} &= (V_{in-} - V_{in+}) + (V_B + |V_{TP}|) \end{aligned} \quad (3)$$

The sum and difference of these two relations gives

$$V_{SG1} + V_{SG2} = 2(V_B + |V_{TP}|) \quad (4)$$

$$V_{SG1} - V_{SG2} = 2(V_{in+} - V_{in-}) \quad (5)$$

Substituting expression (4) and (5) in expression (2), the output differential current, which shows the well by V_B, is written as

$$I_d = 2\beta V_B(V_{in+} - V_{in-}) = g_m V_{id} \quad (6)$$

The linear input signal range is bounded by

$$|V_{id}| < V_B \quad (7)$$

The linear output range is bounded by

$$|I_d| < 2\beta V_B^2 \quad (8)$$

Figure 2(b) shows an efficient implementation of very low impedance voltage source which offers more accurate voltage level shift than a conventional source follower buffer. Each level shifter is built by “Flipped Voltage Follower” FVF cell. FVF cells are composed by two transistors (M1A, M2A and M1B, M2B) and a current source I_B. Assuming matched transistors M1, M2, M1A and M1B, the source-gate voltage of M1A respectively M2A is defined as

$$V_{SG,1A,2A} = V_{SDsat,1A,2A} + |V_{TP}| = V_B + |V_{TP}| \quad (9)$$

in which the DC level shifter voltage, V_B, is written as

$$V_B = \sqrt{\frac{2I_B}{\beta_{1A,2A}}} \tag{10}$$

By replacing this expression in (6), the differential current I_d, which shows the well controlled bias current I_B, is derived as

$$I_d = I_1 - I_2 = 2\beta\sqrt{\frac{2I_B}{\beta_{1A,2A}}}V_{id} \tag{11}$$

Obviously, I_d is linearly proportional to differential input voltage V_{id} and the transconductance g_m is expressed as

$$g_m = 2\beta\sqrt{\frac{2I_B}{\beta_{1A,2A}}} \tag{12}$$

This class-AB input stage using cross coupled differential pair can be operated with a minimum supply voltage of

$$V_{DD,\min} = |V_{TP}| + V_{SDsat,1} + V_{SDsat,2B} \tag{13}$$

where $V_{SD,sat}$ denotes source-drain saturation voltage.

This implementation features very low output impedance, large current sourcing capability, low voltage operation and low standby current consumption [16], [26].

However and especially for low voltage design, the most critical parameter of this transconductor is a limited common mode input voltage range as given by equation (14)

$$V_{SS} + V_{DSsat,mirror} - |V_{TP}| < V_{CMR} < V_{DD} - V_{SDsat,1} - V_{SDsat,2B} - |V_{TP}| \tag{14}$$

According to this relationship, a dissymmetric behavior of the input dynamic range is observed. The input dynamic range is significantly important in the negative part that in the positive one. In the following part, we will present an efficient approach to shift the input dynamic range with a symmetric behavior.

B. DC level input stage

In order to have a transconductor with higher linearity and wider input voltage differential mode range, we will try, in this section, to extend the linear region of the input stage

As shown in equation (14), the dynamic range is limited by the threshold voltage and the drain-source saturation voltage of the MOS transistor for operation in the strong inversion region. So, an efficient way to make the dynamic range symmetrical is to lower the threshold voltage. It is possible to find many researches focusing on this feature and considering low voltage applications or low threshold voltage transistor. Low voltage strong inversion operation can be achieved using bulk driven transistors [27], [28], floating gate transistors [29], [30] and dynamically biased stages [31]. Unfortunately, these approaches may introduce a loss of performance (g_m and g_0 will be degraded).

To overcome this limitation, an approach illustrated in Fig. (3) consists in adding a DC level shifter V_{dc}, in series with the gate of the PMOS transistor. This voltage introduces a translation of the operating point of the transistor in the amplification zone which leads to the reduction of the threshold voltage. The effective threshold voltage will be given by

$$|V_T'| = |V_{TP}| - V_{dc} \tag{15}$$

With this approach and biased at the same drain current level, g_m and g_0 of the transistor will be conserved.

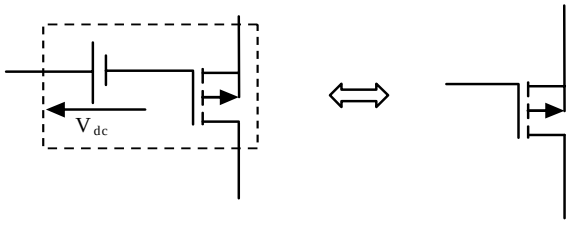

Fig. 3 "Virtual" transistor concept PMOS version

Figure 4 shows the modified version of Fig. 2 which uses "virtual" transistor concept. In this case, the common mode range will be extended by V_{dc} amount, as given by

$$V_{SS} + V_{DSsat,mirror} - |V_{TP}| + V_{dc} < V_{CMR} < V_{DD} - V_{SDsat,1} - V_{SDsat,2B} - |V_{TP}| + V_{dc} \tag{16}$$

The voltage V_{dc} is chosen to have simultaneously a symmetrical and maximum input dynamic.

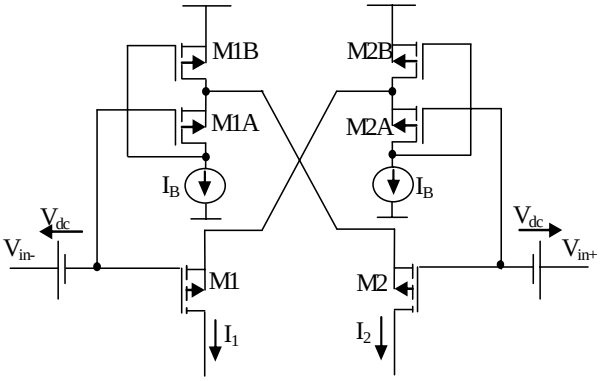

Fig. 4 Class AB input stage with extended input range

The chosen DC level shifter implementation is the conventional NMOS source follower, as shown in Fig. 5.

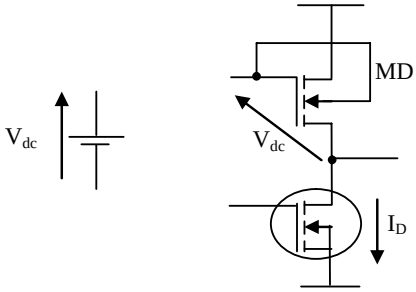

Fig. 5 DC level shifter implementation

If a high impedance current source is provided to the source follower, V_{dc} is considered to be constant. It is given by

$$V_{dc} = \sqrt{\frac{2I_D}{\beta}} + V_{TN} \tag{17}$$

C.. Full circuit implementation

As summarized in Fig. 6, a new high performance CMOS OTA topology is proposed by replacing the conventional class AB input stage using cross coupled differential pair with the modified input stage described above.

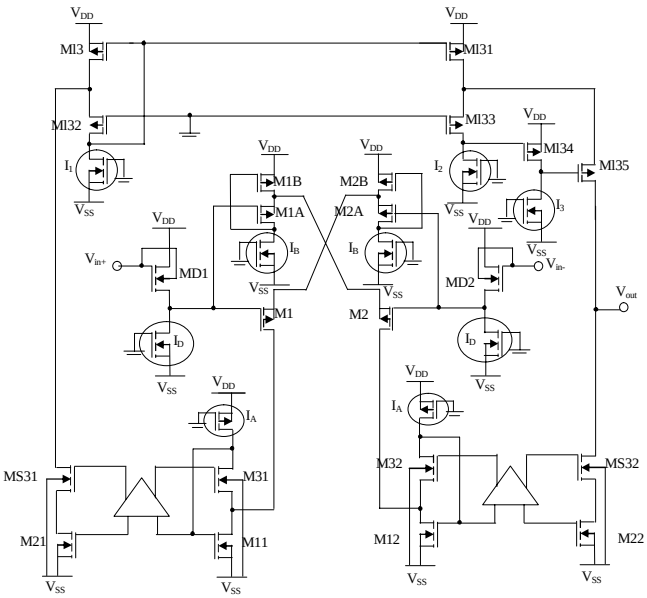

Fig. 6 Proposed transconductor implementation

The proposed OTA, whose synoptic schematic is seen in Fig.1, incorporates some important modifications. We have used two types of current mirror high performance with low operating voltage [32]-[33]. These two structures have a wide bandwidth and high output impedance to have a very high GBW the OTA.The PMOS current mirror connected to V_{DD} is the one proposed in [32]. Due to the input feedback, which consists of the transistor Ml32, the current source I_1 and the voltage source V^B, it reaches low input impedance given by

$$R_{in} = \frac{1}{g_{m,l32} g_{m,l3} r_{o,l32}} \tag{18}$$

and very high output impedance given by

$$R_{out} = g_{m,l34} r_{o,l34} g_{m,l35} r_{o,l35} g_{m,l33} r_{o,l33} r_{o,l31} \tag{19}$$

The NMOS current mirrors connected to V_{SS} are of type flipped voltage follower (FVF) current mirror with regulated cascode output based on full balanced pseudo amplifier's A [33]. Its input impedance is further reduced by the input shunt feedback loop. It's given by

$$R_{in} = \frac{1}{A g_{m1} g_{m1C} r_{o1C}} \tag{20}$$

This version allows very high output impedance by the amplifier's gain A. Its value is

$$R_{out} = A r_{o2} g_{m2C} r_{o2C} \tag{21}$$

III. Simulation Results

The proposed transconductor is simulated using BSIM3v3 Spice models for a TSMC 0.18µm CMOS technology with deep-Nwell process available from MOSIS [34]. Nominal PMOS- and NMOS- transistor threshold voltages in this technology are 0.51V and 0.5V, respectively. This circuit is operated at ± 0.8V supply voltage with a capacitive load of 10pF. The proposed circuit, with and without DC level input stage designated respectively OTA3, OTA2, is validated through the one presented in [8] denoted OTA1. Transistor sizes and values of biasing currents are shown in Table I.

TABLE I
TRANSISTOR SIZES AND BIAS CONDITION FOR ALL CIRCUITS OF OTA

Transistor	Size [a]		
	OTA3	OTA2	OTA1
M1, 2		5µm/0.18µm	
M2A, 2B		30µm/0.18µm	
M1A, 1B		3.5µm/0.18µm	
MD1, D2	23µm/0.18µm	-	-
M11, 12, 21, 22,		30µm/0.18µm	
MS31,S32		90µm/0.18µm	
M31, 32	3µm/0.18µm		30µm0.18µm
Ml3, l31	50µm/0.18µm		2µm0.18µm
Ml32, l33	3µm/0.18µm		-
Ml34	5µm/0.18µm		-
Ml35	40µm/0.18µm		-
$I_{1,2}$	5.12µA		-
I_3	10µA		-
$I_{A,B}$		10.64µA	
I_D	8.10µA	-	-

Figure 7 shows the DC characteristic for all circuits of OTA. The latter shows the differential output current, for a DC sweep of differential input voltage from -0.8V to +0.8V. It proves the effectiveness of the virtual transistor concept in improving the dynamic range of the transconductor with nearly the same slope. The DC transconductance (g_m) is approximately 700µS. Differential output current shows a symmetrical and linear behavior over a differential input voltage range of ±0.5V for OTA3 while it is about of ±0.2V for both OTA2 and OTA1.

Figure 8 shows the linearity error against differential input voltage curve for all circuits of OTA. The error is defined as:

$$\varepsilon(\%) = \frac{I_{out} - I_{out}(0) - g_m(0) V_{id}}{g_m(0) V_{id}} \times 100 \tag{22}$$

where $I_{out}(0)$ and $g_m(0)$ denote respectively the differential output current and the transconductance value for V_{id}=0. $I_{out}(0)$ must be subtracted from I_{out} to remove the contribution of any dc offset to I_{out}. For the proposed circuit (OTA3), the linearity error is less than 0.2% for the whole dynamic range.

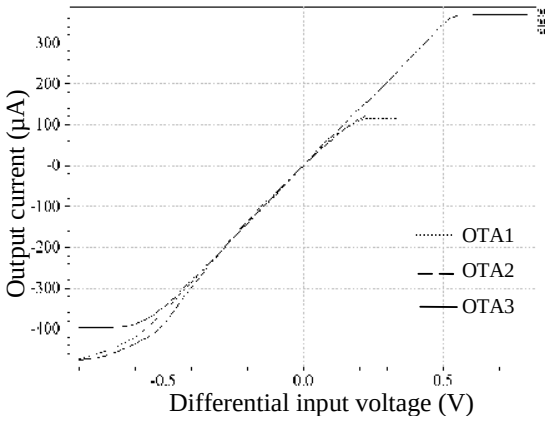

Fig. 7 I-V characteristics of the OTA1, 2, 3

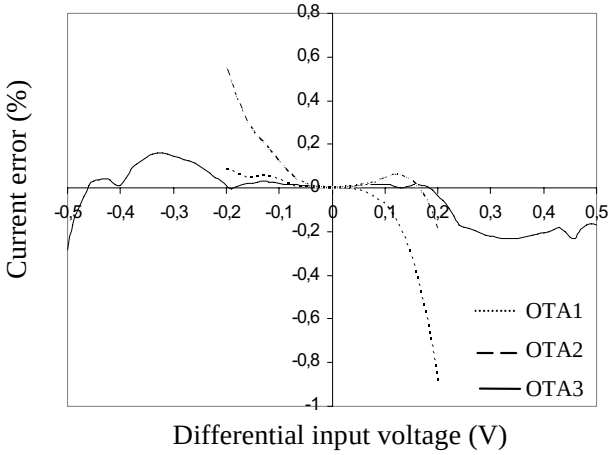

Fig. 8 Linearity error of the transconductor OTA1, 2, 3

Figure 9 shows the open loop frequency response for all circuits of OTA. A high open loop gain of 81.53dB with a large GBW of 12.45MHz is reached by OTA3. For OTA2, we note a low open loop gain closed to 34.86dB. The least one is attained by the basic transconductor (OTA1), it is about 26.46dB.

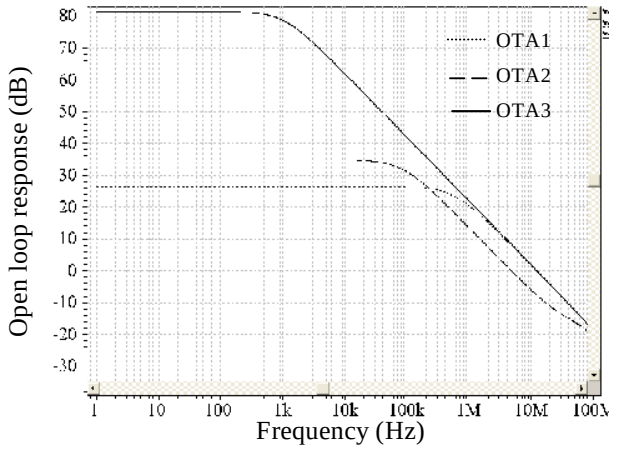

Fig. 9 Open loop frequency response of the OTA1, 2, 3

The simulated rise and fall step response of all circuits of OTA for 0.2Vpp and 1Vpp input differential voltage is, respectively, shown in Fig. 10 and Fig. 11.

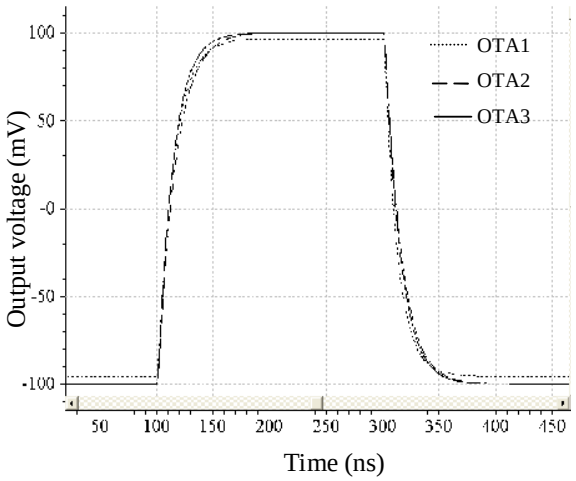

Fig. 10 Step response of the OTA1, 2, 3

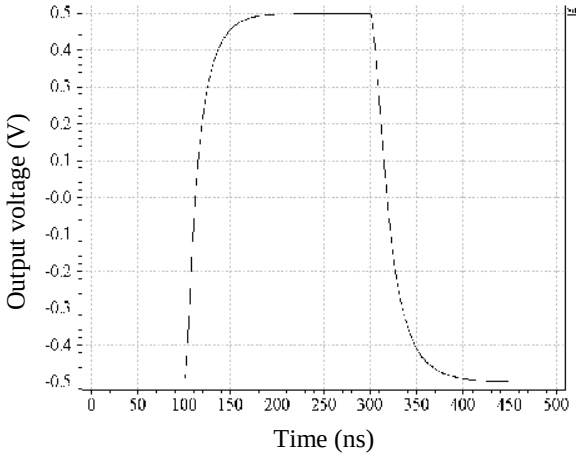

Fig. 11 Step response of the OTA 3

TABLE II
SIMULATION AND BIAS COMPARISON RESULTS

Parameter			OTA3	OTA2	OTA1
Capacitive load				10pF	
Supply voltage				±0.8V	
Positive slew rate (V/μs)	0.2Vpp		5.37	4.63	4.93
	1Vpp		24.09	-	-
Negative slew rate (V/μs)	0.2Vpp		5.31	5.10	6.25
	1Vpp		18.71	-	-
1% settling time (ns)	positive	0.2Vpp	61.33	69.69	62.53
		1Vpp	75.53	-	-
	negative	0.2Vpp	64.63	68.63	57.03
		1Vpp	83.43	-	-
THD (dB) @ 1MHz	0.2Vpp		-46.35	-39.33	-42.81
	1Vpp		-39.86	-	-
Noise level nV/$\sqrt{Hz}$ @ 1MHz			23.07	15.678	14.112
CMRR (dB)			67.51	72.98	41.43
PSRR+ (dc) (dB)			65.59	70.81	32.88
PSRR- (dc) (dB)			68.16	47.92	33.43
Static power consumption (mW)			0.325	0.225	0.191
Open loop voltage gain(dB)			81.53	34.86	26.46
GBW (MHz)			12.45	4.74	12.05
Phase margin (degrees)			86.09	95.3	90.21

Table II summarizes all the simulated results of the proposed OTA (OTA3, 2) and compares them with the basic one (OTA1).In order to evaluate our work towards other works, the defined Figure Of Merit, which weighs the tradeoff between

the transconductance value, linearity performance, speed of the circuit, input swing range and power consumption into account, is expressed as follows:

$$FOM = 10\log\left(\frac{g_m \cdot V_{id} \cdot \left|THD_{dB}\right| \cdot f_0}{Power}\right) \quad (23)$$

This comparison is given in Table III.

TABLE III
PERFORMANCE COMPARISON WITH PREVIOUSLY REPORTED WORKS

Performance design	OTA3	OTA [5]	OTA [8]	OTA [9]	OTA [16]	OTA [17]	OTA [25]	OTA [35]
Technology CMOS (µm)	TSMC 0.18	AMI 0.5	AMI 0.5	0.5	AMS 0.8	0.8	AMS 0.35	0.5
Supply voltage (V)	±0.8	±1	±1	±1	+1.5	+2	±0.75	1.8
Load (pF)	10	80	80	80	-	-	15	-
Transconductance value (µS)	700	-	-	-	155	207	-	80
Input swing range (Vpp)	1	0.9	0.9	0.9	0.6	0.6	-	2
DC gain (dB)	81.53	43	37	-	-	51.37	78	-
GBW (MHz)	12.45	0.725	3.27	0.900	-	-	8.9	-
Phase margin (degrees)	86.09	89.5	56		-	-	81	-
PSRR+ (dB)	65.59	55	41	-	-	-		-
PSRR- (dB)	68.16	58	52	-	-	-		-
CMRR (dB)	67.51	68	85	-	-	-	126	-
THD (dB)	-39.86	-56	-37	-56.47	-37.33	-40	-	-67
@ voltage peak -peak	1Vpp	0.9Vpp	0.9Vpp	0.9Vpp	0.2Vpp	-		1Vpp
@ frequency	1MHz	100kHz,	100kHz,	100kHz	5MHz	10.7MHz		1MHz
Figure of merit	83.26	82.36	76.76	83.54	84.33	84.60		86.96
Output Noise Density	-152,8 $dBV_{rms}/\sqrt{Hz}$	230 μV_{rms} @1MHz	-145.5 $dBV_{rms}/\sqrt{Hz}$	-	-	-	-	-
Power consumption (mW)	0.325	0.120	0.220	0.120	0.042	0.46	0.169	0.360

IV. CONCLUSION

The resulting topology achieves a good input range of 1Vpp with a high DC gain of 81.53dB in ±0.8V supply voltage. The GBW is 12.45MHz and the total harmonic distortion THD is about –40dB for 1Vpp input signal at 1MHz. Besides, the OTA shows high slew rate and low settling time.

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