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Effect of Flaying Capacitors on Improving the 4 Level Three-Cell Inverter

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***Abstract*—**With the rapid advanced of technology, the industrial processes become increasingly demanding, from the point of view, power quality and controllability. The advent of multi levels inverters responds partially to these requirements. But actually, the new generation of multi-cells inverters permits to reach more performances, since, it offers more voltage levels. The disadvantage in the increase of voltage levels by the number of cells in cascades is on account of series igbts synchronisation loss, from where, a limitation of cells in cascade to 4. Regarding to these constraints, a new topology is proposed in this paper, which increases the voltage levels of the three-cell inverter from 4 to 8; with the same number of igbts, and using less stored energy in the flaying capacitors. The details of operation and modelling of this new inverter structure are also presented, then tested thanks to a three phase induction motor.

***Keywords*—**Flaying capacitors, Multi-cells inverter, pwm, switchers, modelling.

I. Introduction

THE important development which touched the technology of semiconductors [1] opens new research orientations, particularly in the energy conversion techniques. Like first step of development, one can cites the integration of inverters with multi levels NPC structures in electrical power systems [2].The field of application of these inverters is very varied: control of electrical energy conversion in the industry [3], transmission power system stability (FACTS) [4, 5], and improvement of power quality in the networks by active filters [6], renewable energies interfaces [7-10], etc…Also they are an interesting alternative for medium and high power drives [11], because the control of this type of motors by the traditional techniques is on the one hand very delicate, and on the other hand, generates disturbances in the neighbouring network of which they are connected. One of the strong points of multi levels structure is its soft adjustment [3]. The new inverters generation is actually the multi-cells ones. The invention of this type of inverter is likely to discredit the traditional multi-level inverter, because, they offer a better performance with more flexibility, low cost and commutations [12].Several researchers studied these new structures, from the point of view: topological [13], comparative with the other existing structures [14], techniques of controls [12], insertion in the power grid [12], etc…

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II. Multi-Cells Structure

The multi-cell inverter is designed by the connection of cells in cascade Fig. 1, separated by capacities operating in series [15]. The alternating voltage which feeds load is obtained via an artificial neutral (*N*), taken at the medium point of the DC source (*E*) The operation of this inverter can be grouped on the Table I, in which one presents all the possible sequences of commutations offered by switchers *SW*.

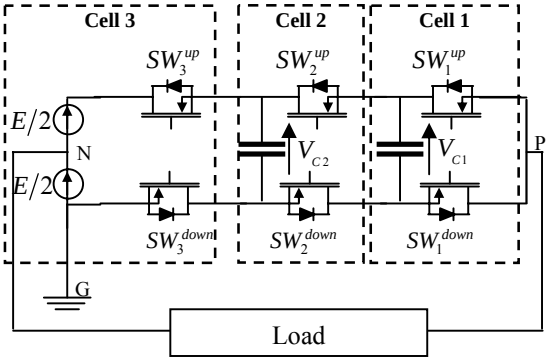


Fig. 1 Three cells inverter Structure

TABLE I
Inverter Operation

	SW_1	SW_2	SW_3	V_{PG}	V_{PN}
V_1	up	up	up	E	E/2
V_2	up	up	down	E-V_{C1}	E/2-V_{C1}
V_3	up	down	up	E-V_{C2} +V_{C1}	E/2-V_{C2} +V_{C1}
V_4	up	down	down	E-V_{C2}	E/2-V_{C2}
V_5	down	up	up	V_{C2}	V_{C2}-E/2
V_6	down	up	down	V_{C2} -V_{C1}	V_{C2} -V_{C1}-E/2
V_7	down	down	up	V_{C1}	V_{C1}-E/2
V_8	down	down	down	0	-E/2

The function of switchers is to allow the passage through all possible voltage levels Vk; $K \in [1 \div 8]$. Against, the diodes are used to make a stress distribution at the flaying capacitors, during the micro phases of switchers break time, thus allowing, maintaining their voltages around a fixed value.

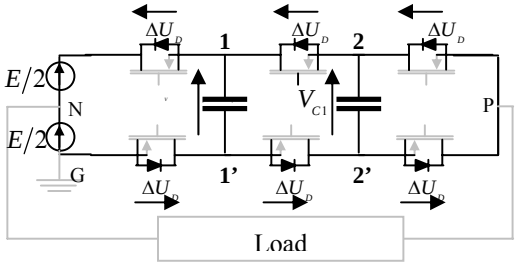


Fig. 2 Flaying capacitors distribution voltages

As the diodes are identical, they present then, the same voltage drops, so, this results to write: $E = 6\Delta U_D \Rightarrow \Delta U_D = E/6$. The diode voltage drop (ΔU_D) will imposes at the flaying capacitors the voltages $V_{C1} = E/3$ (see circuit *2, P, 2 '*), & $V_{C2} = 2E/3$ (see circuit *1, 2, P, 2 ', 1 '*) Fig. 2. Thus, in accordance with these two values of V_{C1} and V_{C2}, one notices that this inverter offers 4 level voltages $V_{PN} = [E/2 \quad E/6 \quad -E/6 \quad -E/2]$; Table I.

With an aim of generalization, and so that this study will not be limited to an inverter with 3 cells, a relation which gives the terminal flaying capacitors voltage for an inverter with n cells is defined Fig. 3.

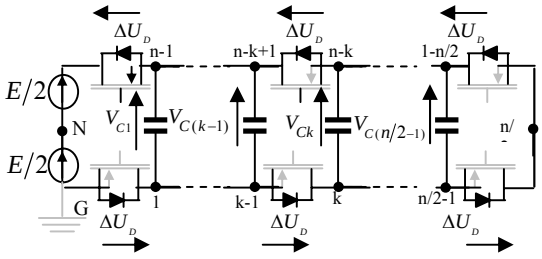


Fig. 3 Multi-cells structure

The voltage of each diode $\Delta U_D = E/n$, so one can define the terminal voltages of flaying capacitors $V_{C(n-K)} = (n-2k).E/n$

Let us study more in detail the inverter with 3 cells. The voltage V_{PG} is the sum of each cell voltage (1). They even depend on the conductions state of switchers' (Fig. 1).

Phase to ground voltage

$$V_{PG} = V_{Cell1} + V_{Cell2} + V_{Cell3} \qquad (1)$$

Cells voltages

$$V_{Cell3} = \begin{cases} E & if \quad SW_3^{up} \\ -E & if \quad SW_3^{down} \end{cases}$$

$$V_{Cell2} = \begin{cases} -V_{C2} & if \quad SW_3^{up} \quad \& \quad SW_2^{down} \\ 0 & if \quad SW_3^{up} \quad \& \quad SW_2^{up} \\ 0 & if \quad SW_3^{down} \quad \& \quad SW_2^{down} \\ V_{C2} & if \quad SW_3^{down} \quad \& \quad SW_2^{up} \end{cases}$$

$$V_{Cell1} = \begin{cases} -V_{C1} & if \quad SW_2^{up} \quad \& \quad SW_1^{down} \\ 0 & if \quad SW_2^{up} \quad \& \quad SW_1^{up} \\ 0 & if \quad SW_2^{down} \quad \& \quad SW_1^{down} \\ V_{C1} & if \quad SW_2^{down} \quad \& \quad SW_1^{up} \end{cases}$$

Since the switchers of the same cell must be complementary, in order to avoid the open circuits or the parallel connection of two various values of voltages. Then, if one of the switchers is at the state on, the other one must be at the state off. Thus in number language, it is proposed, for the switcher up SW^{up} "1" and for the switcher down SW^{down} "- 1" Table II. This made, and in accordance with the system (2) we define the switching functions for each cell.

$$V_{Cell3} = (1 + SW_3).E/2$$
$$V_{Cell2} = (SW_2 - SW_3).E/3$$
$$V_{Cell1} = (SW_1 - SW_2).E/6$$
$$V_{PN} = V_{PG} - E/2$$

After replacement of these last expressions in the relation (1), one finds: $V_{PG} = (3 + SW_3 + SW_2 + SW_1).E/6$

The fact of having the same voltage for various sequences of commutations can be used in the loop of control, like additional degree of freedom for the voltage maintaining of each capacitors to its fixed value [15]. In order to pass through all the sequences (Table II) same authors propose 3 carriers shifted to 1/3 of period each [16] (Fig. 4). The control technique presented is the pulse wide modulation PWM, with triangular carriers.

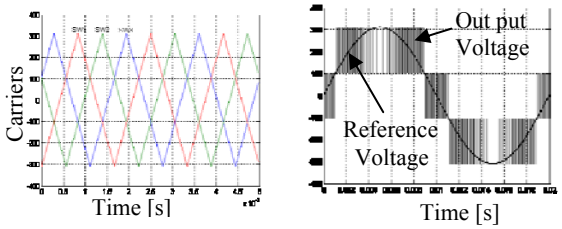


Fig. 4 Three carriers and the corresponding output voltage

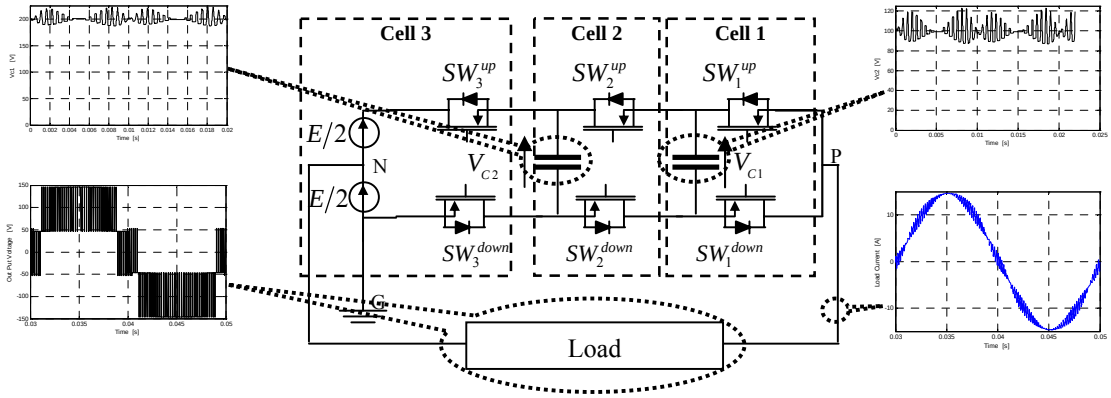
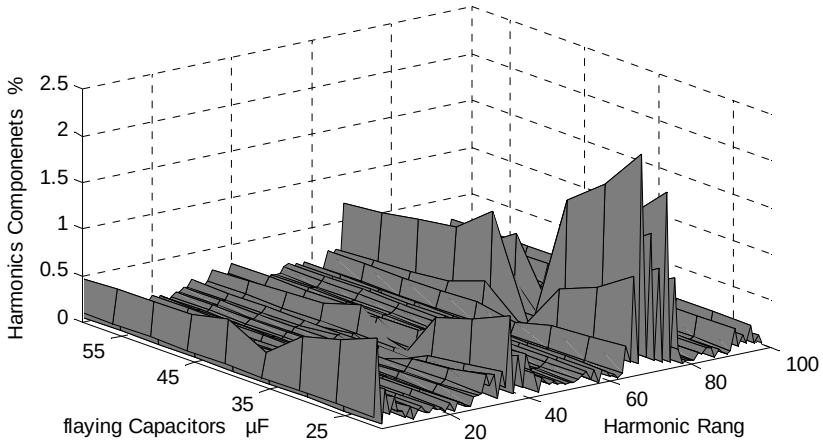
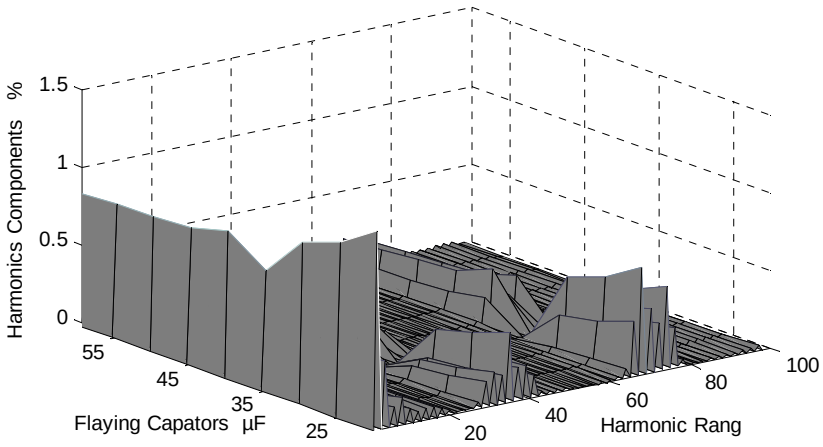


Fig. 5 Simulation model



(a)



(b)

Fig. 6 Harmonics Spectrum
(a) Voltage
(b) Current

TABLE II
FLAYING CAPACITORS EFFECT

C µF	20	25	30	**35**	40	45	50	55	60
THD_V %	4.3649	3.5388	3.0069	**1.2744**	2.3764	1.9133	1.8207	1.7461	1.6839
V_{OutPut}	145.23	145.34	145.41	**145.66**	145.48	145.54	145.55	145.56	145.57
THD_I %	1.8968	1.5995	1.4195	**0.9759**	1.2241	1.0967	1.0733	1.0564	1.0419
I_L	14.52	14.53	14.54	**14.56**	14.54	14.55	14.556	14.55	14.55

III. SIMULATION AND RESULTS

The single phase multi-cell inverter is modelled then simulated for a fixed RL load "R=10Ω & L=1.5mH" with different Flaying Capacitors values.

Varying the capacitor on can notice a clear improvement of the output variables and the power quality delivered by the inverter. This says the optimization of the capacitors sizes used make it possible to reach the best performances of the multi-cellular inverter:

- A great stability of intermediate voltages V_{C1} and V_{C2}.
- The THD_V and THD_I are on their low level respectively 1.2744% and 0.9759% .
- All the energy of the DC bus is transferred towards the alternate consumer as a fundamental frequency with a minimum energy waste, evaluated to 2.93%.

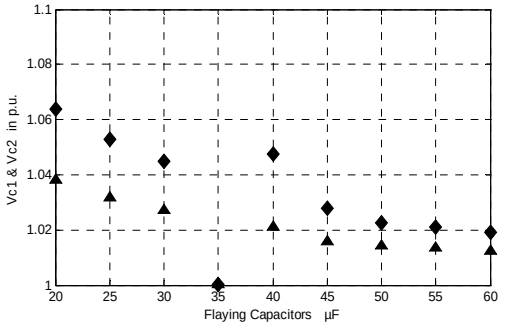


Fig. 7 Effect of capacitors sizes on the distributed voltages

IV. CONCLUSION

The wished inverter output voltage defined by the reference is an average value between successive levels commutations, in an interval time fixed by carrier period. This voltage sample influences the sinusoid current thickness, because the commutation from one level to another imposes important electromagnetic energies exchange stored in the reactive elements. This unwanted exchange can be attenuated by the optimal choice of the Flaying Capacitors values.

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