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# A High-Speed and Low-Energy Ternary Content Addressable Memory Design Using Feedback in Match-Line Sense Amplifier

Syed Iftekhar Ali, M. S. Islam



***Abstract*—**In this paper we present an energy efficient match-line (ML) sensing scheme for high-speed ternary content-addressable memory (TCAM). The proposed scheme isolates the sensing unit of the sense amplifier from the large and variable ML capacitance. It employs feedback in the sense amplifier to successfully detect a match while keeping the ML voltage swing low. This reduced voltage swing results in large energy saving. Simulation performed using 130nm 1.2V CMOS logic shows at least 30% total energy saving in our scheme compared to popular current race (CR) scheme for similar search speed. In terms of speed, dynamic energy, peak power consumption and transistor count our scheme also shows better performance than mismatch-dependant (MD) power allocation technique which also employs feedback in the sense amplifier. Additionally, the implementation of our scheme is simpler than CR or MD scheme because of absence of analog control voltage and programmable delay circuit as have been used in those schemes.

***Keywords*—**content-addressable memory, energy consumption, feedback, peak power, sensing scheme, sense amplifier, ternary.

## I. Introduction

IN last two decades ternary content-addressable memory (TCAM) has become popular in internet protocol (IP) packet forwarding and classification applications performed in network routers and switches. These applications require high speed search capability to decide which action to be taken on the packet. Routers extract the packet header information (such as destination address) and search the routing table to find the most suitable match. Software based search techniques are also available. But these techniques are slow because of the need for multiple instructions execution and multiple memory accesses to external RAM to find a match [1]. Ternary content-addressable memory (TCAM) offers a high speed hardware based solution to this problem. TCAM can compare an input search word against a table of stored words and can return the address of the matching word in a single cycle. It can store don't care values which may result in multiple matches with the search word. The most suitable match is selected by a priority encoder. This capability of finding the longest prefix match i.e. match with the word having least number of don't care values makes TCAM even more attractive for network applications.

Syed Iftekhar Ali is with the Islamic University of Technology, Board Bazar, Gazipur 1704, Bangladesh (phone: +88-02-9291250; fax: +88-02-9291260; e-mail: s_ali@iut-dhaka.edu).

M. S. Islam is with Bangladesh University of Engineering and Technology, Dhaka 1000, Bangladesh (e-mail: islams@eee.buet.ac.bd).

Conventionally a TCAM cell contains two SRAM cells and a comparison logic circuit as shown in Fig. 1(a). Both NAND and NOR versions of comparison logic are in use. But the NOR type comparison logic as shown in the figure is more prevalent due to higher speed and absence of charge sharing problem [2]. The stored data (Data1Data2) is coded to represent three states such as '0' (01), '1' (10) and don't care or 'X' (00). Search data (SL1SL2) is provided through search line (SL) pair. In case of a mismatch the match line (ML) is pulled down to ground by one of the paths through M1M2 or through M3M4. In case of a match (Data1Data2=SL1SL2)

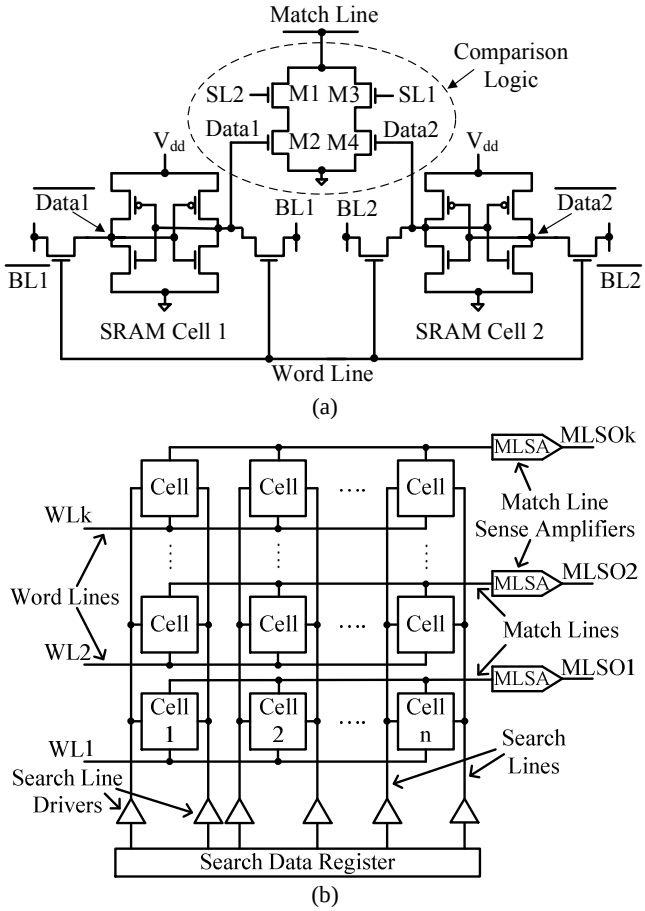


Fig. 1 (a) A conventional TCAM cell consisting of two SRAM cells and NOR-type comparison logic. (b) Block diagram of a simplified k-word × n-digit TCAM array. Bit lines (BLs) have not been shown for clarity.

there is no connection between ML and ground. Multiple cells having a common ML form a TCAM word and multiple words form a TCAM array as shown in Fig. 1(b). One pair of SLs is shared by all TCAM cells in a column. A major disadvantage of TCAM is the high energy consumption resulting from frequent switching of highly capacitive MLs and SLs. So, reduction of dynamic energy consumption remains a major challenge for TCAM designers.

## II. Previous Work

In conventional TCAM the MLs are precharged to high and the SLs are precharged to ground [3]. Then search word is supplied through search data register. If there is a match between the search word and a stored word there is no conduction path from corresponding ML to ground and ML voltage remains high. But if there is even a single mismatch, the ML voltage discharges to 0 through the comparison logic in the mismatched TCAM cell. The match line sense amplifier (MLSA) outputs (at MLSO) low for all mismatched MLs and outputs high for all matched MLs. As only a few MLs are matched in a search, a large amount of energy is wasted in charging large number of mismatched MLs which are eventually discharged to ground during match evaluation.

Different techniques have been proposed for reducing TCAM energy consumption. Some popular schemes are selective precharge scheme [4], pipelining scheme [5], pre-computation based scheme [6], bank selection scheme [7], block encoding scheme [8], charge sharing techniques [9] – [12], current race technique [13], and mismatch dependent technique [14]. Selective precharge scheme [4] divides ML into two segments and performs initial comparison in the first segment. Only if the first segment fully matches with the search word fragment then the second segment is activated and compared. The pipelining scheme [5] divides ML in to more than two segments and performs the comparison segment by segment starting from the first one. Only if the current segment being compared matches fully then the next segment is compared. Otherwise the later segment remains inactive. The effectiveness of these two techniques depends on the distribution of the data and in the worst case there is no energy saving at all. Pre-computation based scheme [6] performs some initial comparison to determine which MLs need to be activated for comparison. For example, in the initial comparison total number of ones present in the stored words and the search word may be compared. This technique requires additional circuits and evaluation time to perform the initial comparison. Bank selection scheme [7] divides all the words into groups called banks. During the search only the relevant bank in activated and compared. The problem with this technique is bank overflow which happens when the number of input combinations exceeds the storage capacity of a bank. Block encoding scheme [8] uses some special encoding technique to compress IP addresses and thus reduces number of words needed to be stored in the routing table. Energy reduction is achieved by reduction of TCAM array size. Charge sharing techniques use either a separate capacitor [9], [10] or segment(s) of the ML [11], [12] to store charge in the precharge or partial comparison phase, respectively. This charge is shared with the ML or remaining ML segment(s) in the next phase. Techniques in [9], [10] are also called low swing schemes as they reduce the ML power by reducing the ML swing voltage. These techniques suffer from the problem of low noise margin and area penalty arising from the extra capacitor. The technique in [11] divides ML into four segments and precharges two segments to full $V_{dd}$ (in case of a match) in the initial phase. In the next phase the stored charge is shared with the remaining two segments and the resulting ML voltage is sensed using a match sensor block. The implementation of the match sensor block is complex and it requires additional control signals for its operation. The enhancement of search time and the reduction of energy consumption in charge shared scheme in [12] compared to the conventional scheme are small. So far, the most popular energy reduction scheme is the current race (CR) technique [13]. Fig. 2 shows the MLSA of CR scheme in mixed block and circuit diagram form.

In CR scheme the MLs are pre-discharged to ground. MLEN signal initiates the search operation. During the search MLs are charged towards high. SLs need not to be pre-discharged to ground in this technique. This reduced SL switching activity compared to the conventional scheme [3] saves around 50% SL energy. For fully matched words the corresponding MLs get quickly charged to a threshold which

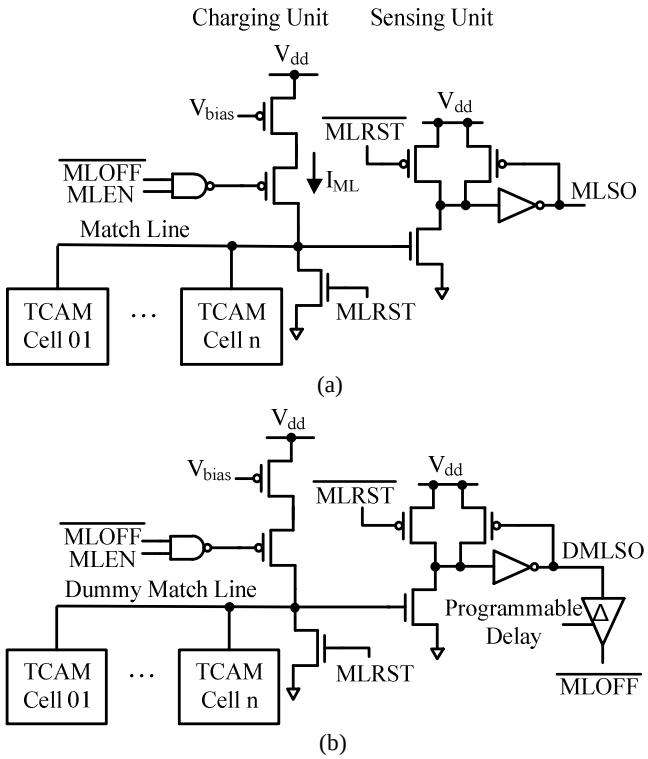


Fig. 2 Current-race sensing scheme - (a) one TCAM word with MLSA consisting of charging unit and sensing unit and (b) a dummy word resembling an always-matched ML.

causes the sensing unit to output high at MLSO. For mismatched words, MLs have discharging paths to ground and hence cannot be charged up to that threshold. So, outputs of the associated MLSAs remain low. A dummy word resembling a fully matched word is used to control the charging duration of MLs. As soon as the dummy word output becomes high further charging of all MLs is discontinued by the $\overline{\text{MLOFF}}$ signal. During the ML charging phase CR scheme supplies similar currents to both matched and mismatched MLs. So, here also large amount of energy is wasted in large number of mismatched MLs. Feedback in MLSA have been used in [14] to reduce the current to the mismatched MLs. The mismatch dependant (MD) MLSA proposed in [14] uses the same sensing unit and the dummy word concept of CR scheme. But the charging unit in this scheme contains a level shifter and a feedback circuit to implement feedback as shown in Fig. 3.

In speed-optimized setting of MD scheme the MLs and $V_{VAR}$ nodes are precharged to ground first. MLEN starts the charging of all MLs. Initially, both ML voltage ($V_{ML}$) and voltage at $V_{VAR}$ node increase by currents $I_{ML}$ and $I_{bias}$, respectively. As $V_{VAR}$ voltage increases current $I_{ML}$ decreases. But with increases of $V_{ML}$ the level shifter output also increases. For a matched ML the level shifter output becomes sufficiently high to turn on N1 and hence $V_{VAR}$ node starts to discharge again. With reduced $V_{VAR}$ voltage $I_{ML}$ for matched ML increases. For mismatched MLs the ML voltages rise slowly and to lower values depending on number of mismatches present in the word. So, for mismatched MLs N1 may get weakly turned on or it may remain off depending on number of mismatches resulting in small or no reduction in $V_{VAR}$ voltage. So, matched MLs get higher currents than mismatched MLs and in terms of ML energy this techniques can offer significant energy reduction compared to CR scheme. But, the level shifter and the feedback circuit also consume some energy and in terms of total energy the saving is not significant. Moreover, for proper operation the transistors have to be large specially in the level shifter which

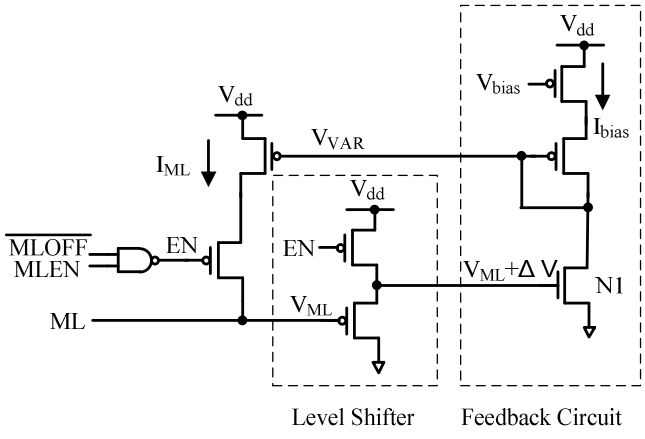


Fig. 3 Charging unit with level shifter and feedback circuit in mismatch-dependent sensing scheme. Signal $\overline{\text{MLOFF}}$ comes from the output of dummy word after a programmable delay.

makes match detection process significantly slow. The transistor count in the MLSA is also high compared to CR MLSA. And finally, the feedback action is extremely sensitive to $V_{bias}$ and MLSA transistor sizing. So, small process variation may completely destroy the feedback mechanism nullifying the effectiveness of this scheme.

In this paper we propose a ML sensing scheme which employs a simple but effective feedback mechanism to speed up the match detection process and reduce energy consumption. We have used CR-type MLSA with some modification in the charging unit to incorporate the feedback action while keeping the implementation complexity and transistor count low. The match detection has been performed with low ML voltage to save energy. Same dummy word concept as in CR has been used to control the charging durations of MLs. We have also eliminated the need for additional control signals such as $V_{bias}$.

The rest of the paper is organized as follows. Section III presents the circuit diagram and operation of the proposed ML sensing scheme. Section IV presents simulation results and comparison of the proposed scheme with the CR and MD ML sensing scheme. In this section we also present simulation results considering process variations in our scheme. Section V includes conclusion.

## III. Proposed ML Sensing Scheme with Feedback in MLSA

Fig. 4 shows one n-digit TCAM word and the dummy word

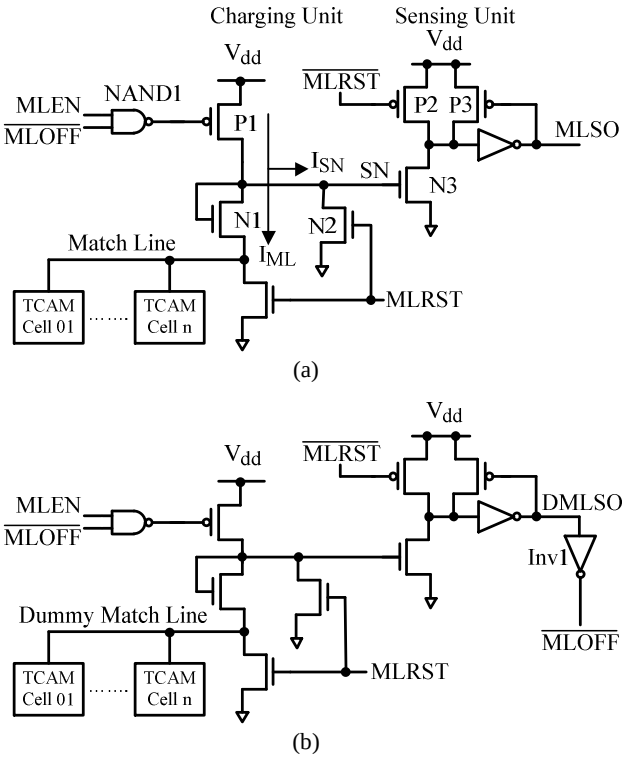


Fig. 4 The proposed ML sensing scheme - (a) one n-digit word containing MLSA consisting of charging and sensing units and (b) a dummy word which is always matched.

in the proposed scheme. It should be noted that one TCAM digit is actually coded two bits as mentioned in section I. Before the search operation begins the MLRST signal resets the ML voltages, sensing nodes (SNs) and MLSA outputs (MLSO, DMLSO) to ground. The search data is applied to the SLs (Fig. 1).

MLEN initiates the search. It starts charging all MLs and the dummy ML (DML) by turning on P1. Initially both matched and mismatched MLs and SNs get the same current through P1. As the ML voltage ($V_{ML}$) goes up the feedback action of nMOS N1 starts. With increasing ML voltage $V_{ds}$, $V_{gs}$ of N1 decrease and $V_{sb}$ increases causing threshold voltage to rise. So, the channel resistance increases. More current is diverted to the sensing node capacitance, $C_{SN}$. So, voltage at SN ($V_{SN}$) increases. Increase of $V_{SN}$ causes increase of $V_{ds}$, $V_{gs}$ of N1 causing more current to ML and increase in $V_{ML}$. Thus a positive feedback action goes on between $V_{ML}$ and $V_{SN}$. Since $C_{SN}$ is small it can be charged very quickly by this positive feedback action. Matched MLs are disconnected from ground and hence they charge much faster than the mismatched MLs. This makes $C_{SN}$ of a matched ML charge much quicker than $C_{SN}$ of a mismatched ML. As soon as the $V_{SN}$ of a matched ML exceeds the sensing threshold voltage ($V_t$ of N3) of the sensing unit, MLSO is pulled to high. DML works exactly like a matched ML. A high DMLSO stops flow of charging current to the ML (and DML) by turning off P1. The SN voltages of mismatched MLs do not charge up to the sensing threshold of the corresponding sensing units. So, outputs of MLSAs of mismatched MLs remain low.

The match line capacitance, $C_{ML}$ depends on many factors such as TCAM word size, bit values in the supplied search line word and MLSA input capacitance. $C_{ML}$ is generally large and varies from one search to another. Unlike CR and MD sensing scheme the proposed scheme isolates $C_{ML}$ from the sensing unit input and uses an intermediate node capacitance $C_{SN}$ to make the match decision. The value of $C_{SN}$ is determined by gate and drain capacitances of N1, drain capacitance of N2 and gate capacitance of N3. So, $C_{SN}$ is small and does not vary between searches. Unlike MD scheme where the feedback action is sensed in the ML charging current, in the proposed scheme the charging current to $C_{SN}$ senses the feedback action. Small value of $C_{SN}$ and positive feedback action to charge this small capacitance make it possible to detect a match with much lower ML voltage than CR or MD scheme. Since energy consumption is directly proportional to ML voltage swing [2] the proposed scheme can significantly reduce the energy consumption in a search.

If the initial charging current (before feedback starts) through P1 is too high and the channel resistance of the feedback nMOS N1 is too large then $C_{SN}$ charges so quickly that correct mismatch detection becomes impossible. So, the gate dimensions of the transistors P1 and N1 have to be chosen carefully so that the feedback action can become effective.

In both CR and MD schemes a programmable delay (Δ in Fig. 2(b)) was used after DML output to delay the termination of ML charging to ensure proper match detection. We find that in the proposed scheme the delay introduced by the series inverter and the NAND gate (Inv1 and NAND1) is sufficient to serve that purpose even under the worst case process variation. That is why, no programmable delay element has been used in our scheme. CR and MD schemes used an analog control voltage $V_{bias}$ to control the charging current or nullify the effects of process variations. We have avoided such voltages as our scheme is immune to worst case process variations as will be shown in the next section. Absence of programmable delay and additional control voltage (both generation and routing) make implementation of the proposed scheme much simpler than the other two schemes.

## IV. Simulation Results and Comparison

In internet protocol version 4 (IPv4) IP address length is 32 bit. The new internet protocol version 6 (IPv6) addresses are 128 bit long and the corresponding forwarding table requires a large TCAM array. In this paper we considered forwarding table containing smaller IPv4 addresses in order to keep the simulation time within reasonable limit. But of course the same concept can be applied to IPv6 forwarding table just by increasing the TCAM word size

In this paper we have performed all simulations using 64 words×32 digits TCAM array using 130nm 1.2V CMOS logic. Predictive technology model (PTM) [15] has been used in HSPICE for the simulation. Since our array size if different from [13] and [14], we have performed comprehensive simulations of proposed, CR [13] and MD [14] schemes to analyse and compare various aspects of the schemes. Unfortunately [13] does not provide any information on the sizes of the transistors used in the CR MLSA. We found that it is possible to design CR scheme with wide range of search speed, voltage margin, dynamic search energy and peak power consumption. But improvement in one parameter generally comes at the cost of deterioration of others e.g., increasing search speed cause decrease in voltage margin and increase in peak power consumption. We choose transistor sizes (and $V_{bias}$ value) to get two configurations of CR scheme – one which has search speed comparable to the speed in our scheme and one with the highest achievable search speed. The first configuration of the CR scheme has been used as the reference design. We call this two configurations reference CR and high-speed CR, respectively. The sizes of the transistors in MLSA, the value of control voltage ($V_{bias}$) and the amount of programmable delay were not specified in [14]. Without this information it was not possible for us to reproduce the exact ML currents reported in [14]. We found that the feedback action in MD scheme works only within a very limited range of transistor sizes and $V_{bias}$ values. After extensive simulations we could achieve excellent feedback action in the MD scheme as will be shown in the following subsection. For the sake of fair comparison no programmable delay has been used after DML in CR and MD MLSA (Δ=0 in Fig. 2(b)) as that would increase the energy consumption of these schemes. CR and

MD schemes function correctly with this setting when no process variations are considered.

*A. Charging Currents*

We have simulated the variations of all charging currents in all three schemes. Fig. 5 shows the ML charging currents in reference CR and MD schemes where $I_{ML0}$, $I_{ML1}$, and $I_{ML2}$ mean currents for TCAM words with full match (0-bit mismatch), 1-bit mismatch and 2-bit mismatch, respectively. In CR scheme the charging current increases with number of mismatches as ML to ground path has lower resistance for higher number of mismatches. In MD scheme initially same currents flow to all the MLs. The feedback action starts around 633ps after the initiation of MLEN (in all cases MLEN is initiated at 68ns). The feedback action causes maximum current to be sent to ML with full match and gradually decreasing currents to MLs with increasing number of mismatches.

Fig. 6 shows the variations of total charging current $I_T$ ($=I_{ML}+I_{SN}$) and SN charging current $I_{SN}$ for matched and mismatched MLs in our scheme where the numbers in

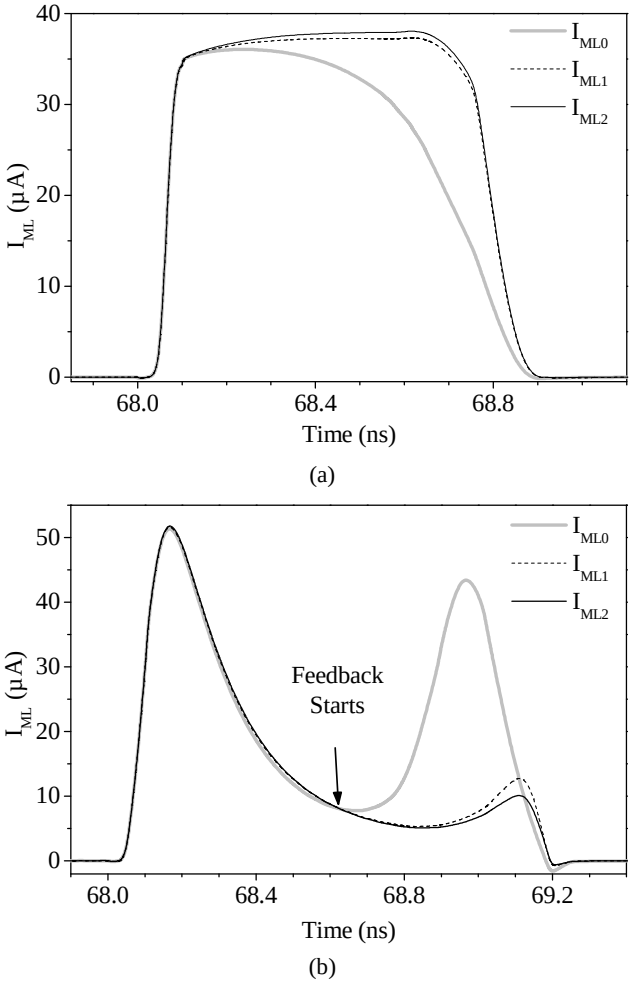


Fig. 5 ML charging currents for match and different mismatch conditions in (a) reference CR sensing scheme and (b) in MD scheme.

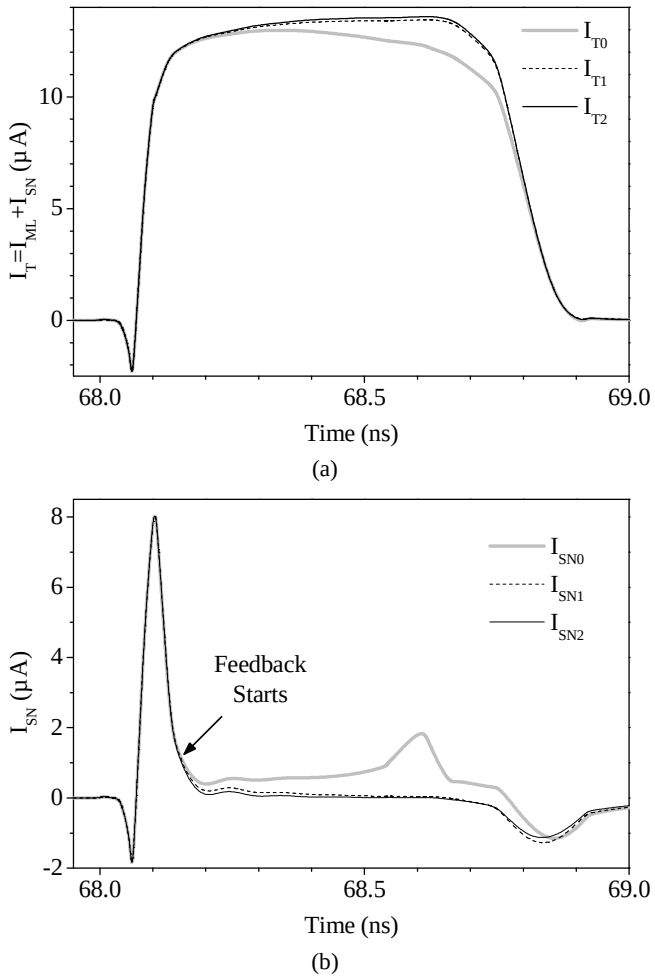


Fig. 6 (a) Total ML and SN charging current and (b) only SN charging current for match and different mismatch conditions in the proposed scheme.

subscripts 0, 1, and 2 mean full match, 1-bit mismatch and 2-bit mismatch, respectively. The variations in total charging current look similar to that in $I_{ML}$ in CR scheme and lack any indication of feedback. The magnitudes of currents are much smaller in our scheme signifying substantial energy savings. The feedback action is effective in $I_{SN}$ as explained in the previous section. Initially, for both matched and mismatched MLs, $I_{SN}$ charging currents are same. After ~155ps the feedback action begins which is much earlier than the initiation of feedback in MD scheme. Earlier initiation of feedback in the proposed scheme indicates that our scheme will detect a match earlier than MD scheme. Matched ML causes more current to be channelled to SN while for mismatched MLs SN currents decrease with increasing number of mismatches. After shutting off the ML charging current at the end of the search cycle the charge stored in $C_{SN}$ passes to ML through the feedback transistor N1 as N1 is still working in saturation mode. That is why, SN current becomes negative after the match decision has been made. The resulting reduction of SN voltage may turn off N3 (Fig. 4(a)) in case of a full match. The inverter of sensing unit can maintain a high output for

sufficiently long time (up to the commencement of the next search) even at this condition. The magnitudes of $I_{SN}$ currents are small signifying that charging of $C_{SN}$ consumes insignificant energy.

*B. Voltage Margin*

ML with 1-bit mismatch has the maximum resistance path to ground since there is only one path through two nMOS transistors as discussed in section I. If there are multiple mismatches, multiple ML to ground pull-down paths exist in parallel and hence the equivalent resistance of ML to ground path is lower. Among all types of mismatches, 1-bit mismatch causes minimum charge leakage from ML to ground during match evaluation. Hence ML with 1-bit mismatch charges faster than MLs with more than one mismatch. That is why, 1-bit mismatch is the hardest to detect and it has the highest probability to be detected as a false match. So, we compare voltage variations of MLs and SNs with full match and with 1-bit mismatch.

Fig. 7 shows the variations of voltages of ML and SN for a fully matched ML and for a 1-bit mismatched ML of the proposed scheme. The maximum voltage to which a matched ML needs to be charged for correct match detection is only 308mV (25.7% of $V_{dd}$). In CR and MD schemes the corresponding values are 1066mV and 1138mV, respectively. For 1-bit mismatch the maximum ML voltages are 68mV, 212mV and 171mV in the proposed, CR and MD schemes, respectively. $V_{ML}$ (and also $V_{SN}$) decreases with number of mismatches but the magnitude of $V_{ML}$ in our scheme remains lower than that in other schemes for same number of mismatches. Since most of the MLs are mismatched in a search, the reduced ML voltage of the proposed scheme will definitely result in large energy savings compared to other two schemes. Though some energy is consumed in charging $C_{SN}$ but this energy is small as $I_{SN}$ is small. Also it is clear from Fig. 7b that from initiation of charging up to ~155ps, $C_{SN}$ of both matched and mismatched MLs charge at the same rate due to same initial current supplied by the charging pMOS P1. After that the feedback action begins causing $C_{SN}$ of matched ML to charge at higher rate than that of mismatched ML though $C_{SN}$ values are same in both matched and mismatched MLs.

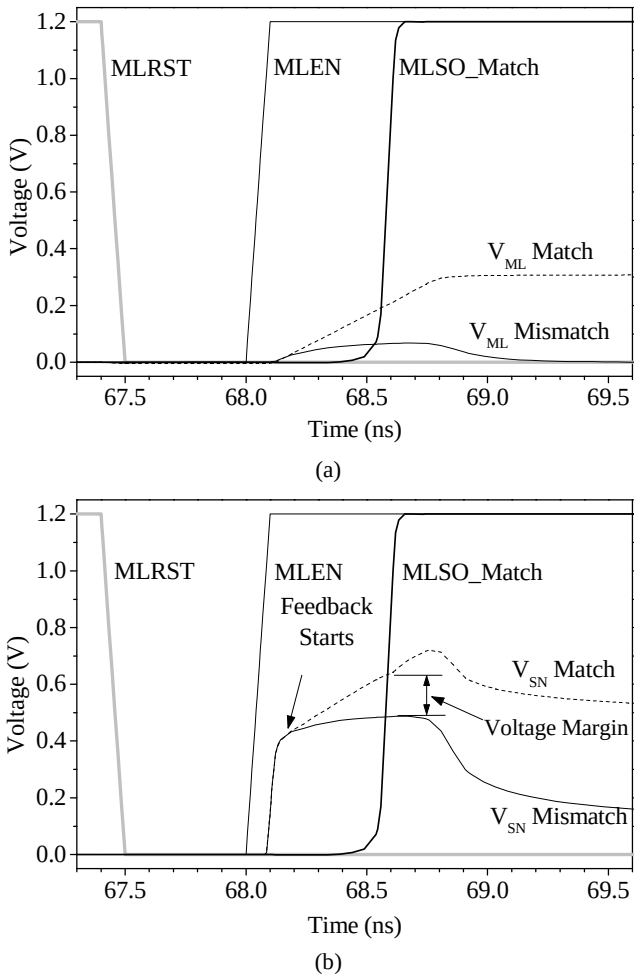


Fig. 7 Variations of (a) ML and (b) SN voltages with match and 1-bit mismatch of the proposed scheme.

Voltage margin is defined as the difference between the sensing threshold of the sensing unit and the maximum voltage to which a 1-bit mismatched ML (in CR and MD) or SN (in proposed) is charged. Higher is the voltage margin greater is the circuit's ability to handle process variations and noise. Table I shows the comparison of voltage margins in different techniques. Like all low swing schemes our scheme suffers from the problem of low voltage margin. But we will show later that this reduced voltage margin is still sufficient to take care of the worst process variations.

*C. Search Time*

Search time is defined as the time from 50% of MLEN to 50% of MLSO. Table I shows the comparison of search times of different schemes. Reference [14] did not report any speed comparison with the CR scheme. According to our simulation results, MD scheme is significantly slower (46.3%) than the reference CR scheme. As mentioned earlier we designed the reference CR scheme to have search speed comparable to our scheme. The high-speed CR scheme can achieve higher search speed at the cost of reduced voltage margin.

*D. Energy Consumption*

Energy consumption per word per search in any scheme varies with match or mismatch condition. Fully matched words consumes more energy than mismatched words as MLs are charged to higher voltages and MLSA outputs have to be pulled to high. If the word is mismatched then energy

TABLE I
VOLTAGE MARGIN AND SEARCH SPEED COMPARISON OF THE PROPOSED, CR AND MD SCHEMES

| | **Proposed scheme** | **Reference CR scheme** | **High-speed CR scheme** | **MD scheme** |
|---|---|---|---|---|
| Voltage margin | 150mV | 513mV | 150mV | 419mV |
| Search time | 534ps | 536ps | 214ps | 784ps |

consumption per word varies with number of mismatches present in the word. In our scheme the dominant currents which flow in the MLSA of a mismatched words are charging unit current through P1 and sensing unit current through P3 (Fig. 4(a)). As shown in Fig. 6(a), with increase of number of mismatches current through P1 increases by a small amount. But at the same time $V_{SN}$ decreases with increasing mismatch number. Smaller $V_{SN}$ means smaller gate voltage at N3, less subthreshold conduction through N3 and hence less current through P3 to keep the internal node (input of the sensing unit inverter) at high. This reduction in P3 current is more than the increase of P1 current. So, the total current supplied by $V_{dd}$ decreases with increasing number of mismatches. So, among all types of mismatches in our scheme maximum energy consumption per word per search occurs for 1-bit mismatch. In MD MLSA the dominant currents are $I_{ML}$ and $I_{bias}$ (Fig. 3). With increasing number of mismatches both currents decrease. Hence, energy consumption per word also decreases with increasing number of mismatches. In CR scheme ML charging current determines the dynamic energy consumption. This current increases with number of mismatches (Fig. 5(a)). So, the energy consumption per word per search is minimum for 1-bit mismatch.

Reference [14] used 130nm CMOS simulation and reported an average ML energy reduction of 40% in terms of fJ/bit/search compared to CR scheme. IP address distribution is never completely random and finding probabilities of match or different types of mismatches is difficult. Average energy saving calculation is based on probabilities of match and mismatches and hence is less accurate. We prefer a different approach for energy comparison. We have found the minimum (worst case) energy saving in our scheme compared to CR. So, we have constructed a routing table which will cause maximum energy consumption in our scheme (and also MD scheme). Since only a few words are fully matched in a search, in our routing table there are 4 fully matched words and the remaining 60 words are with 1-bit mismatch. We simulated all three schemes using this routing table and calculated the total energy consumption by the TCAM arrays from the dynamic power consumption curves. Table II shows the calculated energy consumption and minimum energy savings. The energy reduction in our scheme is much greater than that in MD scheme. This is due to the fact that lower charging current is supplied for smaller charging duration (because of higher speed) in our scheme. Also the reported average 40% energy saving in [14] is questionable as it seems the authors considered only the ML charging current $I_{ML}$ to calculate the energy saving. But the combined energy consumption in the feedback circuit (by current $I_{bias}$) and level shifter is not negligible and inclusion of this energy would result in reduced total energy saving.

TABLE II
COMPARISON OF ENERGY CONSUMPTIONS AND MINIMUM ENERGY SAVINGS COMPARED TO CR SCHEME

| | Proposed scheme | Reference CR scheme | High-speed CR scheme | MD scheme |
|---|---|---|---|---|
| Energy consumption | 1774fJ (maximum) | 2540fJ (minimum) | 2517fJ | 2397fJ (maximum) |
| Energy saving | 30% (minimum) | - | 0.9% | 5.6% (minimum) |

### *E. Peak Dynamic Power*

Peak power consumption with the worst case data pattern is a critical CAM performance parameter [2]. Most of the energy saving techniques concentrates on reducing average power consumption but ignores the increase of peak power consumption. Increased peak power consumption requires more power to be allocated for the TCAM chip which is useful only for a short duration. But during rest of the search cycle most of that allocated power remains unutilised. So, lower peak power consumption means cheaper supply can be used or the extra power can be allocated for other components. The worst case routing table used in the last subsection has been used to obtain peak power consumption of various schemes. Table III shows the comparison where positive percentage change means increase and negative means decrease. The proposed scheme requires the lowest peak power consumption. This is logical since the peak charging current magnitude in our scheme is lower than that in other scheme (Fig. 5 and Fig. 6). The high-speed CR configuration requires extremely large peak power to speed-up the match detection.

### *F. Transistor Count*

Table IV shows the number of transistors per MLSA required by different schemes. In the table the transistors used to reset ML and $V_{VAR}$ in MD scheme (not shown in Fig. 3) are also counted. Large level shifter transistors, higher transistor count and complex circuit design increase the circuit area and make routing of different signals more difficult in MD scheme.

### *G. Worst case process variations*

Since the voltage margin in our scheme is lower than the same in other schemes, we perform simulations to determine the robustness of our scheme to worst case process variations. Process variations can give rise to two problem scenarios.

TABLE III
COMPARISON OF PEAK POWER CONSUMPTIONS BY 64 WORD × 32 DIGIT TCAM ARRAYS IN DIFFERENT SCHEMES

| | Proposed scheme | Reference CR scheme | High-speed CR scheme | MD scheme |
|---|---|---|---|---|
| Peak power (μW) | 2849 | 3556 | 6975 | 4839 |
| Percentage change w.r.t. CR | -19.9% | - | +96.1% | +36% |

TABLE IV
COMPARISON OF TRANSISTOR COUNT PER MLSA

| | Proposed scheme | CR scheme | MD scheme |
|---|---|---|---|
| Number of transistors | 13 | 12 | 18 |

The first scenario is SN and ML voltages in 1-bit mismatched ML may rise faster than regular values and may trigger the sensing units to produce wrong match decision before the charging pMOS transistors are turned off by a regular DML. In order to identify the factors which can increase the voltages we reproduce the circuit with SN and ML charging and discharging paths in case of a 1-bit mismatch. Fig. 8 shows the circuit diagram.

The SN voltage will rise faster than the regular if

- larger charging current is supplied by P1. This can happen if the width of P1 ($W_{P1}$) increases due to process variation,
- transistor N1 offers greater channel resistance due to reduction in gate width ($W_{N1}$) causing greater portion of total charging current to be diverted to SN and
- $C_{ML}$ charges faster than the regular case causing $C_{SN}$ to be charged faster also. This can happen due to reduction in gate widths ($W_{M3}$, $W_{M4}$) and increase in threshold voltages ($V_{tM3}$, $V_{tM4}$) of M3 and M4 causing less charge leakage from $C_{ML}$ to ground.

All of the above scenarios can be implemented by

- increasing $W_{P1}$ by 20%, decreasing $W_{N1}$, $W_{M3}$ and $W_{M4}$ by 20% and increasing both $V_{tM3}$ and $V_{tM4}$ by 15% in only one word having 1-bit mismatch.
- keeping all other 63 words and the dummy word in the TCAM array regular (no process variation).

Fig. 9 shows the SN transient voltages in both the process varied (PV) and regular words. MLSA of the process varied mismatched ML can detect the mismatch correctly. Higher initial current to $C_{SN}$ causes higher $V_{SN}$ voltage resulting in reduction of voltage margin to 69mV. This margin is still sufficient to take care of significant threshold voltage rise of the sensing nMOS (N3 in Fig. 4) due to process variations.

The second problem scenario is when only dummy word goes through process variations such that its ML and SN charge faster than a regular fully matched word. The dummy word will turn off the charging pMOS transistors earlier. A regular matched word may not be able to trigger its sensing

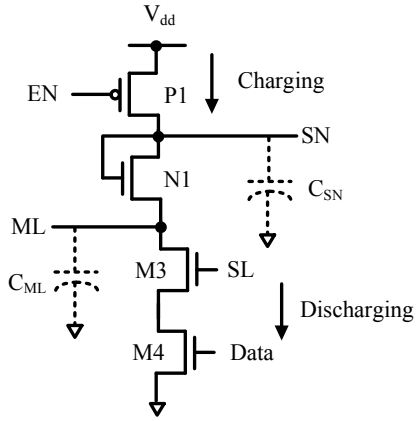


Fig. 8 Circuit diagram of ML and MLSA with 1-bit mismatch. M3 and M4 form the ML pull-down path in the comparison logic in the mismatched bit.

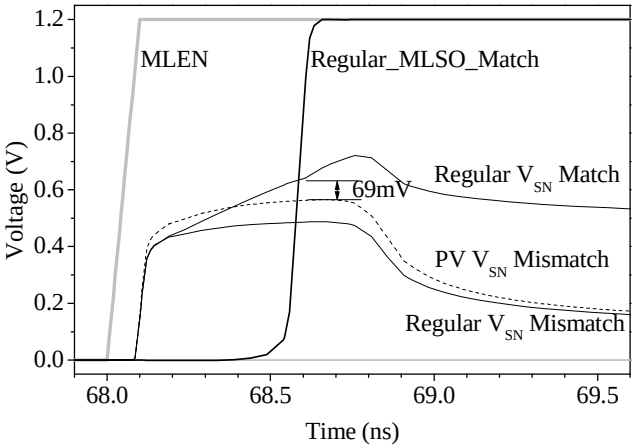


Fig. 9 Variations of SN voltages in case of regular match, regular 1-bit mismatch and process varied (PV) 1-bit mismatch.

unit by that time causing wrong match decision. Since a dummy word is always matched (M3 and M4 remain off), this scenario is simulated by assuming 20% increase in $W_{P1}$ and 20% reduction in $W_{N1}$ in MLSA of DML only.

Fig. 10 shows the SN voltages and MLSA outputs of the

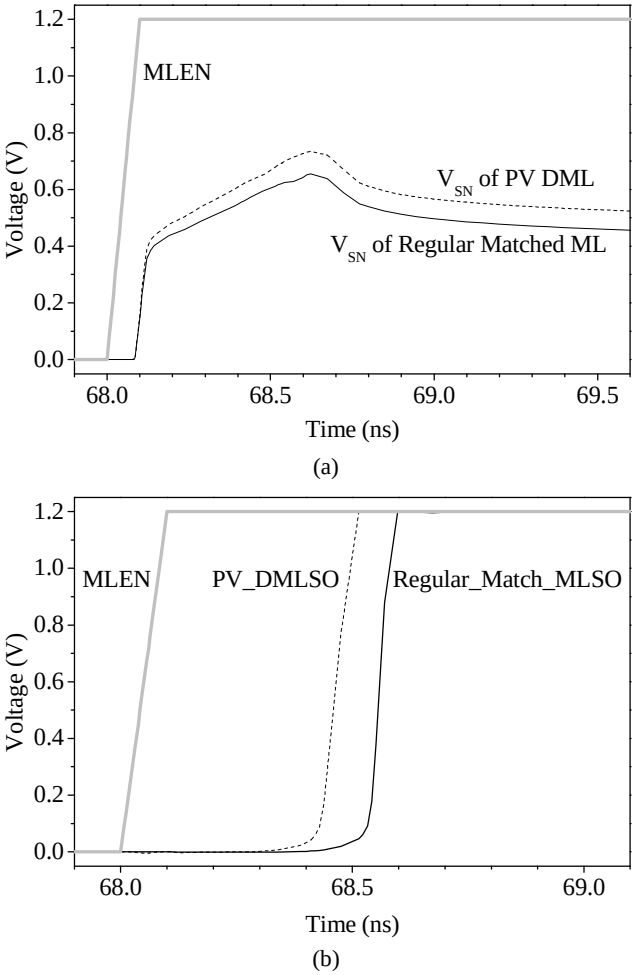


Fig. 10 Variations of (a) SN voltages and (b) MLSA output voltages with regular matched ML and process varied (PV) DML.

process varied DML and regular matched ML. As expected, $C_{SN}$ of DML charges faster and to a higher voltage than that of a regular $C_{SN}$. So, DMLSO becomes high before a regular MLSO. A regular MLSO can become high in spite of earlier transition of DMLSO because the transition of DMLSO is sensed by P1 (Fig. 4) after a finite delay caused by the series inverter (Inv1 in Fig. 4(b)) and the NAND gate (NAND1 in Fig. 4(a)).

## V. Conclusions

We presented a ML sensing scheme for TCAM using positive feedback in the MLSA. Here we have implemented TCAM cells in all schemes using popular 6T SRAM cells though the original CR scheme [13] used 4T asymmetric cells. But this does not affect the performance parameters i.e. voltage margin, search speed, energy consumption etc. discussed in this paper. The main objective of the proposed scheme was to achieve low energy consumption. Simulation of 64-word×32-digit TCAM array shows at least 30% energy saving compared to CR scheme. In contrast to many schemes available in literature we kept the implementation complexity low by eliminating the need for any analog control voltage and by using small number of transistors. It was shown that a trade-off has to be maintained between voltage margin, search speed, energy consumption, peak power consumption, circuit area and implementation complexity. Our scheme offers excellent enhancement to all performance parameters except the voltage margin. Here we have intentionally sacrificed voltage margin to get higher search speed. By choosing suitable transistor sizes in the MLSA it is possible to increase voltage margin at the cost of reduced search speed.

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**Syed Iftekhar Ali** received his B.Sc. and M.Sc. engineering degrees in Electrical and Electronic Engineering (EEE) from Bangladesh University of Engineering and Technology (BUET), Dhaka, Bangladesh in 1999 and 2002, respectively. He also received Master of Applied Science (MASc) in Electrical and Computer Engineering from University of Waterloo, Waterloo, Canada in 2004.

Currently he is an Assistant Professor in Electrical and Electronic Engineering Department, Islamic University of Technology (IUT), Gazipur, Bangladesh. He is also a part-time PhD student in the Department of EEE, BUET, Dhaka. He has authored and co-authored several papers published in international conference proceedings and refereed journals. His research interests are semiconductor device modeling, material characterization and low power VLSI circuits.

**M. S. Islam** received both the B.Sc. Eng. and M.Sc. Eng. degrees in Electrical and Electronic Engineering (EEE) from Bangladesh University of Engineering and Technology (BUET), Dhaka, Bangladesh in 1987 and 1989, respectively. He did his PhD degree in microelectronics from the Microelectronics Research Laboratory, School of Electronic Engineering, Dublin City University, Republic of Ireland in 1997. His doctoral research concentrated on the development and characterization of non-alloyed Pd/Sn ohmic contacts for GaAs devices.

He joined as a Lecturer in the department of EEE, BUET, Bangladesh in 1989 and became an Assistant Professor in 1992. He became an Associate Professor in the same department in 1999. From June 2003 to March 2005, he served as an Associate Professor in the Research Institute of Electronics (RIE), Shizuoka University, Japan. He also served as a Visiting Professor in the RIE, Shizuoka University, Japan from April 2005 to June 2005. Presently, he is serving as a Professor in the Department of EEE, BUET, Bangladesh. He has authored and co-authored more than 60 papers published in various conference proceedings and refereed journals. His research interests include device physics, modeling, fabrication and characterization of high-speed devices (MESFETs and HEMTs) using different III-V compound semiconductor materials such as GaAs, GaN, SiC and InP.

Dr. Islam is a senior member of the IEEE, USA and a Fellow of the Institution of Engineers Bangladesh (IEB). He is serving as the Vice Chair, IEEE Bangladesh Section.