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# Effective Scheduling of Semiconductor Manufacturing using Simulation

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***Abstract*—**The process of wafer fabrication is arguably the most technologically complex and capital intensive stage in semiconductor manufacturing. This large-scale discrete-event process is highly re-entrant, and involves hundreds of machines, restrictions, and processing steps. Therefore, production control of wafer fabrication facilities (fab), specifically scheduling, is one of the most challenging problems that this industry faces. Dispatching rules have been extensively applied to the scheduling problems in semiconductor manufacturing. Moreover, lot release policies are commonly used in this manufacturing setting to further improve the performance of such systems and reduce its inherent variability. In this work, simulation is used in the scheduling of re-entrant flow shop manufacturing systems with an application in semiconductor wafer fabrication; where, a simulation model has been developed for the Intel Five-Machine Six Step Mini-Fab using the Extend$^{TM}$ simulation environment. The Mini-Fab has been selected as it captures the challenges involved in scheduling the highly re-entrant semiconductor manufacturing lines. A number of scenarios have been developed and have been used to evaluate the effect of different dispatching rules and lot release policies on the selected performance measures. Results of simulation showed that the performance of the Mini-Fab can be drastically improved using a combination of dispatching rules and lot release policy.

***Keywords*—**Dispatching rules, lot release policy, re-entrant flow shop, semiconductor manufacturing.

## I. Introduction

THE semiconductor manufacturing industry is a rapidly growing industry, due to the increasing demand of its variant products, which are widely used in most of all modern devices. Any technology that increases factory output by even modest amounts can have significant impact on the bottom line. As a consequence, reducing inventories, decreasing cycle time, and improving the utilization of resources are very important issues in this industry.

Objectives like throughput time and outs must be optimized to push the technological development and secure the existence in a rapid growing global market. Especially in the frontend of the semiconductor manufacturing process, wafer fabrication; where, the later is dominated by cluster-tools and re-entrance flows making the production planning and control function highly complicated.

Re-entrant flow shop scheduling problem is closely related to semiconductor wafer fabrication facilities (fab). This is due to the fact that in semiconductor manufacturing the machines used in the product line are extremely expensive and comprise 75% of the total cost of the fabrication facility. Consequently, each wafer revisits the same machines several times to produce different layers.

Effective factory scheduling and dispatching plays a key role in improving equipment reliability and utilization, and in throughput time reduction and outs maximizing. This production control function decides how wafers should be released into a fab and how they should be dispatched among machines for processing.

Presented here is a simulation model that has been developed for a virtual five-machine six-step mini-fab using the Extend$^{TM}$ simulation environment. The Mini-Fab has been selected for this study as it captures the challenges involved in scheduling the highly re-entrant semiconductor manufacturing lines.

The aim of this work is to evaluate the impact of lot release policies and dispatching rules on the performance of semiconductor manufacturing facilities using simulation.

The remainder of this paper is organized as follows: in the next section, a brief review of literature related to scheduling in semiconductor manufacturing is given followed by a description of the system under study. Then, the design of the different simulation experiments is covered and the results of the experimentations carried out are detailed. Finally, the conclusions drawn from this work are pointed out.

## II. Literature Review

A lot of scheduling techniques for semiconductor manufacturing have been stated in publications over the last years. Authors classify the different scheduling techniques into four groups: dispatching heuristics (priority rule), mathematical programming, search methods and artificial intelligence techniques [1, 2].

Dispatching rules have been extensively applied to scheduling problems in semiconductor manufacturing such as wafer fabrication due to the complexity of the process as they are procedures designed to provide good solutions to complex problems in real time [1, 3]. It should be noted that the terms

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dispatching rules, scheduling rules, sequencing rules, or heuristics are often used synonymously in literature.

There are primarily two ways in which control is exercised over the plant. First, one can specify when new lots are to be released into the plant. This is done by the *release policy*. Second, for lots already in the plant, one has to decide which lot is processed next at each machine as it becomes available. This is done by the machine or lot scheduling policy, which is called the *scheduling policy* [4].

### A. Release Policy

Lot releasing policy has significant impact on system performances of semiconductor manufacturing line. There are generally two types of lot release strategy as discussed in [5]; static release strategy, and dynamic release strategy.

In the static strategy, the release velocity is determined before wafer fab, as: Deterministic input [5, 6], Poisson input [5, 7], and UNIF: Uniform release rule [8]. In the dynamic strategy, the release velocity is under human's control in wafer fab according to some performance measure, as: CONWIP: Constant work in process [5, 7-9], WR: Workload regulating rule [6, 8, 10], and SA: Starvation Avoidance rule [8, 10].

Each strategy has its own applied field. Static release strategy is simple and easy to implement, which is mainly used in some investigations. Dynamic release strategy is flexible according to changes in demand, so it is used in real manufacturing line [5].

### B. Scheduling Policy

For lot release control, it is necessary to select a wafer lot to be released into the fab and to determine the time to release the wafer lot, while it is necessary for lot scheduling to determine sequences of processing wafer lots waiting in front of workstations.

The scheduling strategy determines when specified lot(s) is/are processed by a specific machine, while the lot release strategy determines when and how many lots are released into the wafer fab.

From the most previous studies on lot scheduling problems in wafer fabrication, dispatching rules have been used for sequencing [10]. Literally hundreds of different dispatching rules have been proposed by researches as well as practitioners [11]. Dispatching rules for semiconductor manufacturing lines can be divided into the following categories [5]:

*1) Scheduling Based on Waiting Time*

The simplest dispatching rule is the FIFO (First In First Out), also called FCFS (First Come First Served), this rule chooses the job that has entered the queue at the earliest for loading. FIFO is an effective rule for minimizing the maximum cycle time. Opposing to the FIFO is the LIFO (Last In First Out), also called LBFS (Last Buffer First Serve), this policy is motivated by attempting to minimize the cycle-time. It is known from Little's Law that the mean time spent by the part in the system, is proportional to the total number of parts in the system [3, 7, 12-14].

*2) Scheduling Based on Cycle Time*

Dispatching rules based on cycle time are scheduling rules that are found effective in the reduction of cycle time. These include SPT (Shortest Processing Time), LPT (Longest Processing Time), SRPT (Smallest Remaining Processing Time) or LWKR (Least Work Remaining), LRPT (Largest Remaining Processing Time) or MWKR (Most Work Remaining), and SST (Shortest Setup Time) [1, 3, 7, 13].

*3) Scheduling Based on Due Date*

Probably the most popular dispatching rule based on the due date is the EDD (Earliest Due Date). This rule dispatch wafers according to the due date of the wafers, the earliest due date will be dispatched first [7], which can be shown to minimize the maximum lateness and the maximum tardiness [11]. Another rule is the CR (Critical Ratio), this is an index number computed by dividing the time remaining until due date by the work time remaining. As opposed to the priority rules, CR is dynamic and easily updated. The CR gives priority to jobs that must be done to keep shipping on schedule. A job with a CR less than 1.0, is one that is falling behind schedule. If CR is exactly 1.0, the job is on schedule. A CR greater than 1.0 means the job is ahead of schedule and has some slack [15]. Moreover, is the LDS (Least Dynamic Slack), where for each job a slack time is defined as the amount of time the lot can be delayed in queue before it is needed at the next important facility group in its route i.e. [(due date – today's date) – (days required to complete job)]. The lot with the smallest slack time is processed first [12, 13].

## III. System Under Study

Simulation models for semiconductor wafer fabrication are important for supporting the decision making processes in manufacturing operations. However, due to the complexity of these systems, usually simpler models of semiconductor wafer fabrication facilities are used as a test bed for evaluating different production control policies. Amongst the most popular models used by researchers is the Intel Five Machine Six Step Mini-Fab model [12, 16-20]. In spite of the fact that this model is relatively small; yet, it captures most of the challenges involved in scheduling wafer fabrication facilities.

Different simulation models have been developed for the Intel Mini-Fab model and were used to evaluate the impact of dispatching rules on a set of predetermined performance measures [12, 17, 21]; also, other simulation models evaluated the impact of changing lot release policies on the Mini-Fab performance [5, 18].

### A. Mini-Fab Model Description

The Mini-Fab model was developed by Intel and Arizona State University researchers. It features six processing steps and five machines distributed in three stations, as shown in Fig. 1.

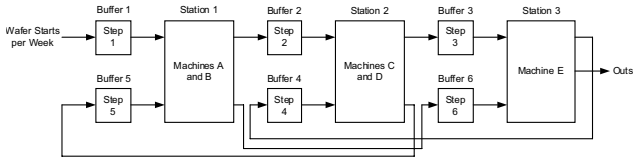


Fig. 1 The Intel five-machine six step Mini-Fab [19].

Table I presents the utilization of each station based on the production of six lots. This is achieved by dividing the available time (minutes per shift) of each station by the time required to produce the six lots (minutes per shift). It is clear from the table that station 3 (machine E) has the highest utilization; hence, this machine is the bottleneck machine[1].

TABLE I
UTILIZATION OF THE THREE STATIONS

| *Station* | *Machine* | *Time Available (min/shift)* | *Step* | *Time Required (min/shift)* | *Utilization* |
|---|---|---|---|---|---|
| 1 | A | 682.5 | S1 | 570 | 87.9% |
| | B | 682.5 | S5 | 630 | |
| | Total | 1365 | Total | 1200 | |
| 2 | C | 540 | S2 | 360 | 77.8% |
| | D | 540 | S4 | 480 | |
| | Total | 1080 | Total | 840 | |
| 3 | E | 690 | S3 | 450 | 91.3% |

### *B. Problem Formulation and Overall Objectives*

The problem can be characterized by a set of lots, where each lot requires six steps (operations). The steps of a lot must be performed in a specified sequence at specific stations. Since, there are three stations in the Mini-Fab and since each lot requires six steps; thus, each lot will visit each station twice.

The objective is to determine the job schedules at the bottleneck machine, machine E at station 3, that minimize (or maximize) a measure (or multiple measures) of performance.

The performance measures that are employed include throughput time (cycle time), Outs, and work-in-process (WIP). Of all these, the commonly used performance measure in wafer fabrication is throughput time (TPT), which is considered as a key performance criterion since reducing the throughput time can improve market responsiveness and reduce work-in-process inventory for any given level of Outs of semiconductor manufacturing [3, 22].

Some revisions and assumptions have been made to the Mini-Fab, these include:

- Neither maintenance technicians nor operators required for loading and unloading are modelled.
- No rework is needed.
- This model does not include travel times.
- Rules for lot batching at station 1 are simpler.
- Tool processing times are deterministic.
- Lots of 24 wafers is the unit being processed by tools.
- Minutes are the time units.

## IV. EXPERIMENTAL DESIGN

After defining the problem to be analyzed using simulation and preparing the different input data for the model, simulation model development takes place, which is described in details in [23]. The simulation model of the Mini-Fab has been developed using the Extend™ v5.0 simulation environment, from Imagine That, Inc.

This section provides a detailed description of the experimental design procedure applied; where, three groups of experiments are carried out:

- *Group (I)* assesses the effect of different dispatching rules on the performance measures.
- *Group (II)* tests the effect of the CONWIP lot release policy on the performance measures.
- *Group (III)* tests the impact of combining the dispatching rules with the CONWIP lot release policy on the performance measures.

The purpose of these experiments is to understand the behaviour of the Mini-Fab when introducing different dispatching rules separately, when introducing a lot release policy separately, and when combining both together.

### *A. Selected Performance Measures*

The performance measures that are evaluated are the average and standard deviation (STD) of TPT; Outs, and WIP. The objective of these experiments is to minimize the average TPT and WIP as well as to maximize the Outs. Moreover, the variability of these performance measures is to be minimized.

Although the standard deviation is recommended by the Mini-Fab; however, it is suggested that the coefficient of variation should also be used to represent the variability in the performance measures. Where, the coefficient of variation (CV) is equal to the standard deviation divided by the average; thus, it is a relative measure to what is being measured (Average TPT and Average Outs).

### *B. Simulation Parameters*

The different simulation parameters that are set for the experiments are the simulation runtime, number of replications, and the warm-up period. A single simulation run covers a time period of two years and the number of replications for each experiment is 20 replications.

In order to define the warm-up period, the simulation model has been run for two years (1,048,320 min.), output of different parameters is monitored, and it is found that the steady state is reached after one year (524,160 min.). Thus, the first year is removed for simulation model warm-up period giving a total of 40 years of data with the first 20 years removed for warm up period.

## V. EXPERIMENTATIONS AND RESULTS

As mentioned earlier, three groups of experiments are carried out; *Group (I)* assesses the effect of different dispatching rules on the performance measures; *Group (II)* tests the effect of the CONWIP lot release policy on the performance measures; while, *Group (III)* tests the impact of combining the dispatching rules with the CONWIP lot release policy on the performance measures.

### *A. Group I: Dispatching Rules*

Seven dispatching rules other than the FIFO (First In First Out), are selected to evaluate the performance measures of the Mini-Fab.

[1]*Detailed description of the Intel Mini-Fab is available at http://www.eas.asu.edu/~aar/research/intel/papers/fabspec.html.*

The other lot dispatching rules selected for this study are:

- LIFO (Last In First Out),
- SRPT (Smallest Remaining Processing Time),
- LRPT (Longest Remaining Processing Time),
- EDD (Earliest Due Date),
- CR (Critical Ratio),
- LDS (Least Dynamic Slack),
- SST (Shortest Setup Time).

The results for the scenarios are shown inTable II, where each result reported in the table is based on *20 replications*.

TABLE II
GROUP (I) SCENARIOS – SUMMARY OF RESULTS.

| *Rule* | *Throughput Time* | | | *Outs* | | | *Work-In-Process* | | |
|---|---|---|---|---|---|---|---|---|---|
| | *Avg.* | *STD* | *CV* | *Avg.* | *STD* | *CV* | *Avg.* | *STD* | *CV* |
| FIFO | 2,288 | 803 | 0.35 | 84.20 | 7.22 | 0.09 | 19.67 | 8.14 | 0.41 |
| LIFO | 2,519 | 3,426 | 1.36 | 83.93 | 9.56 | 0.11 | 21.55 | 11.17 | 0.52 |
| SRPT | 2,114 | 654 | 0.31 | 84.27 | 7.09 | 0.08 | 18.14 | 6.98 | 0.38 |
| LRPT | 2,734 | 1,471 | 0.54 | 84.17 | 11.36 | 0.13 | 23.34 | 13.91 | 0.60 |
| EDD | 2,076 | 603 | 0.29 | 83.84 | 7.35 | 0.09 | 17.75 | 6.62 | 0.37 |
| CR | 2,701 | 2,766 | 1.02 | 83.86 | 11.18 | 0.13 | 23.02 | 13.59 | 0.59 |
| LDS | 2,115 | 1,322 | 0.63 | 84.10 | 7.21 | 0.09 | 18.13 | 7.25 | 0.40 |
| SST | 2,313 | 978 | 0.42 | 83.95 | 8.75 | 0.10 | 19.73 | 9.26 | 0.47 |

Investigating the results of the first group scenarios, it is clear that the EDD dispatching rule has the minimum average, standard deviation, and coefficient of variation of TPT and WIP.

However, the maximum average Outs per week and minimum standard deviation and coefficient of variation of Outs per week are achieved by using the SRPT dispatching rule.

Comparing the results of the EDD and SRPT dispatching rules; it is evident that the EDD would increase the performance of the average TPT with 9.27%, increase the performance of the average WIP with 9.76%, and decrease the performance of the average Outs with 0.42%; whereas, the SRPT would increase the performance of the average TPT with 7.60%, increase the performance of the average WIP with 7.78%, and increase the performance of the average Outs with only 0.08%, thus, the EDD dispatching rule is selected.

It should be noted that these results are typical when using dispatching rules; where, in most cases no one single dispatching rule excels on all criteria.

### *B. Group II: Lot Release Policy*

When using CONWIP as a lot release policy, the WIP level to use must first be set. Different WIP levels are attempted and their effect on the average, standard deviation, and coefficient of variation of TPT and Outs are evaluated. Table III shows the summary of different WIP levels results.

The results depicted in Fig. 2 indicate that average Outs will start to stabilize at a WIP level of 21 lots till it reaches a maximum value of 92 Outs/week (CONWIP levels 24 to 30). Furthermore, it is clear that the lower the CONWIP level the lower the average TPT till it reaches an average of 1,222.40 minutes at CONWIP level of 3 lots, which is the minimum allowable number of lots required for batching at station 1.

TABLE III
GROUP (II) SCENARIOS – SUMMARY OF RESULTS.

| *CONWIP Level* | *Throughput Time* | | | *Outs* | | |
|---|---|---|---|---|---|---|
| | *Avg.* | *STD* | *CV* | *Avg.* | *STD* | *CV* |
| 3 | 1,222.4 | 136.66 | 0.11 | 24.74 | 1.42 | 0.06 |
| 6 | 1,264.0 | 156.23 | 0.12 | 47.84 | 1.98 | 0.04 |
| 9 | 1,396.9 | 186.25 | 0.13 | 64.95 | 2.31 | 0.04 |
| 12 | 1,524.9 | 205.47 | 0.13 | 79.33 | 2.44 | 0.03 |
| 15 | 1,706.4 | 209.18 | 0.12 | 88.61 | 2.01 | 0.02 |
| 18 | 1,984.4 | 208.30 | 0.10 | 91.44 | 1.23 | 0.01 |
| 21 | 2,301.4 | 185.40 | 0.08 | 91.98 | 0.74 | 0.01 |
| 24 | 2,629.6 | 176.03 | 0.07 | 92.00 | 0.12 | 0.00 |
| 27 | 2,958.3 | 176.01 | 0.06 | 92.00 | 0.01 | 0.00 |
| 30 | 3,287.0 | 175.79 | 0.05 | 92.00 | 0.01 | 0.00 |

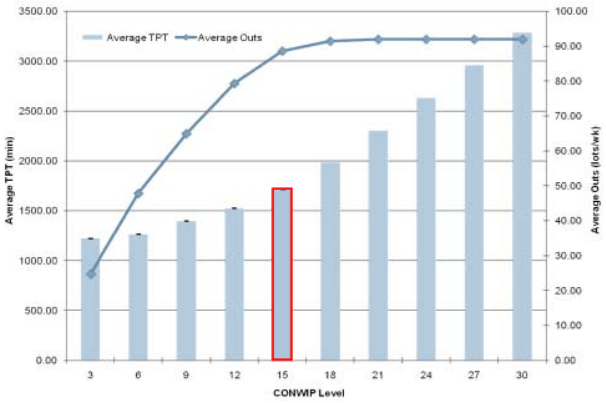


Fig. 2 CONWIP analysis

Average TPT is calculated as a percentage of the minimum TPT (1,706.40 minutes); similarly, average Outs is calculated as a percentage of the maximum Outs (92 lots per week). These values are shown in Fig. 2; where, average of both percentages is used to select the best CONWIP level which is 15 lots.

TABLE IV
SELECTING THE BEST CONWIP LEVEL.

| *CONWIP* | *TPT %* | *Outs %* | *Avg. %* |
|---|---|---|---|
| 3 | 100.00 | 26.89 | 63.45 |
| 6 | 96.71 | 52.00 | 74.35 |
| 9 | 87.51 | 70.60 | 79.05 |
| 12 | 80.16 | 86.23 | 83.20 |
| 15 | 71.64 | 96.32 | 83.98 |
| 18 | 61.60 | 99.39 | 80.50 |
| 21 | 53.12 | 99.98 | 76.55 |
| 24 | 46.49 | 100.00 | 73.24 |
| 27 | 41.32 | 100.00 | 70.66 |
| 30 | 37.19 | 100.00 | 68.59 |

### *C. Group III: Dispatching Rules with Lot Release Policy*

Seven scenarios are carried out by combining the dispatching rules presented earlier with the CONWIP lot release policy (at CONWIP = 15 lots). The results of these scenarios are shown in;

TABLE V
GROUP (III) SCENARIOS – SUMMARY OF RESULTS.

| Dispatch Rule | Throughput Time | | | Outs | | |
|---|---|---|---|---|---|---|
| | Avg. | STD | CV | Avg. | STD | CV |
| FIFO | 1,706.40 | 209.18 | 0.12 | 88.61 | 2.01 | 0.02 |
| LIFO | 1,761.80 | 322.28 | 0.18 | 85.81 | 3.22 | 0.04 |
| SRPT | 1,681.70 | 175.96 | 0.10 | 89.91 | 1.88 | 0.02 |
| LRPT | 1,811.80 | 292.44 | 0.16 | 83.43 | 3.68 | 0.04 |
| EDD | 1,681.60 | 162.83 | 0.10 | 89.91 | 1.83 | 0.02 |
| CR | 1,809.90 | 283.65 | 0.16 | 83.55 | 3.79 | 0.05 |
| LDS | 1,683.00 | 181.31 | 0.11 | 89.84 | 1.93 | 0.02 |
| SST | 1,760.90 | 273.74 | 0.16 | 85.85 | 3.50 | 0.04 |

Results of *Group (III)* scenarios indicate that using the CONWIP lot release policy with the EDD dispatching rule has the minimum average TPT and the maximum average Outs per week, as well as minimum standard deviation and coefficient of variation for both measures.

## VI. SUMMARY AND ANALYSIS OF THE THREE GROUPS

### A. Percentage Improvement

Percentage improvement in the average and coefficient of variation of TPT and Outs is evaluated compared to the base model (FIFO without CONWIP) and is depicted in Fig for the three scenario groups. The figure shows that the highest improvement in performance measures is achieved by *Group (III)* scenarios; specifically, the one using the EDD with CONWIP level of 15 lots.

This scenario results in a minimum average TPT (1,681.6 minutes with an improvement of 26.5%), a maximum average number of Outs (89.91 lots/wk with an improvement of 6.78%), a minimum coefficient of variation of TPT (162 minutes with an improvement of 71.43%), and a minimum coefficient of variation of Outs (1.83 lots/week with an improvement 77.78%).

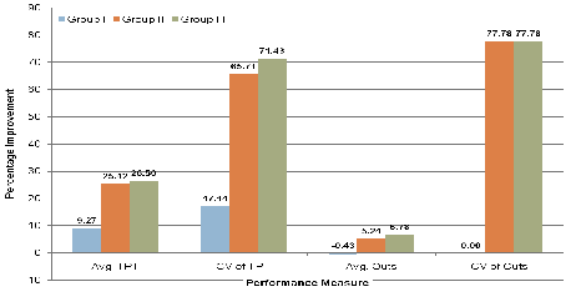


Fig. 3 Percentage improvement

### B. Effect of Lot Release Policy

Comparing results of *Group (I)* and *Group (III)* scenarios, it is concluded from Fig. 3 and Fig. 4 that combining the different dispatching rules with the CONWIP lot release policy decreased the average TPT and increased the average Outs. Thus, it is recommended to use the CONWIP lot release policy to further improve the performance of the Mini-Fab.

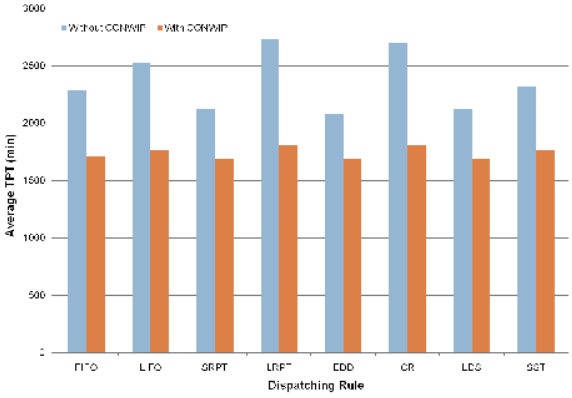


Fig. 3 Average of TPT results.

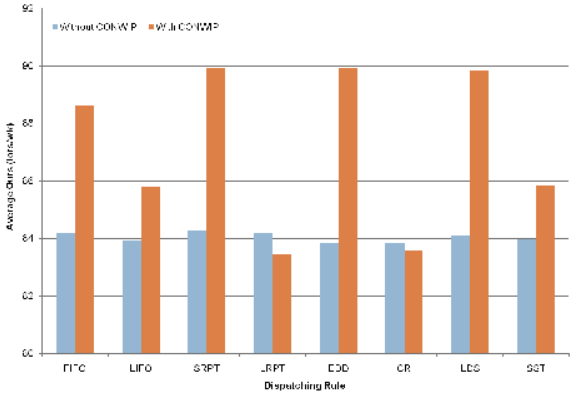


Fig. 4 Average of Outs results

### C. Variability of Performance Measures

As mentioned earlier, the coefficient of variation is a better measure for variability due to the fact that it is a relative measure of variance; in addition, it can help in quantifying the amount of variability in a system. Where, a system is said to exhibit low variability for CV values of up to 0.75, medium variability for CV values of 0.75 to 1.33, and high variability for CV values of greater than 1.33. Fig. 5 shows these three variability levels; where, almost all results are within the low variability limits. Consequently, the standard deviation and coefficient of variation are no longer considered for further analysis. Also, CONWIP drastically reduces the variability of the performance measures.

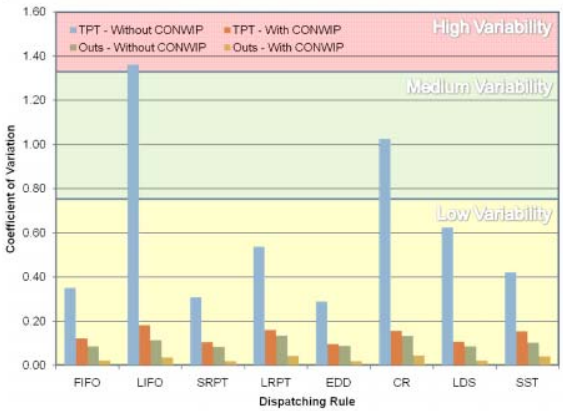


Fig. 5 Coefficient of variation of TPT and Outs

It is evident from the previous results that CONWIP should be used with the dispatching rules to improve the performance of the Mini-Fab; specifically, CONWIP reduces the variability inherent in the Mini-Fab and hence, reduces the amount of waiting time in queue for the bottleneck machine (Machine E).

Reduction of waiting time in queue results in reduction of lot throughput time. In addition, for a constant WIP level, throughput time reduction results in an increase in the number of lots out per week.

CONWIP ability to reduce system variability is the key to its ability to outperform the dispatching rule.

## VII. Conclusion

This work was undertaken to develop a simulation model and evaluate the effect of different input variables on selected performance measures for the Intel Five-Machine Six Step Mini-Fab. The developed simulation model incorporated most of the characteristics of the Mini-Fab such as the re-entrant flow of wafer fabrication, sequence-dependant setup times, lots batching, and scheduled and unscheduled breakdowns.

This section reports the most important findings and conclusions of this work resulting from the simulation runs:

- Using EDD as dispatching rule results in increasing the performance of the average TPT with 9.27%, increasing the performance of the average WIP with 9.76%, and decreasing the performance of the average Outs with 0.42%
- Using CONWIP at a level of 15 lots results in increasing the performance of the average TPT with 25.42% , and increasing the performance of the average Outs with 5.24%.
- Using a combination of EDD and CONWIP level of 15 lots results in increasing the performance of the average TPT with 26.5% , and increasing the performance of the average Outs with 6.78%.
- One of the more significant findings to emerge from this study is that lot release policy is more effective than dispatching rules for controlling the fab and improving its performance.
- Analysis of the coefficient of variance showed that the results obtained from the simulation models lie within the low variability region and has very low values in case of using CONWIP lot release policy.
- Lot release policy drastically improves the Mini-Fab performance as it reduces the variability of the system. This results in reduction of waiting times at the bottleneck machine and; consequently, reducing the throughput time and increasing the Outs.

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