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A Capacitive Sensor Interface Circuit Based on Phase Differential Method

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***Abstract*—**A new interface circuit for capacitive sensor is presented. This paper presents the design and simulation of soil moisture capacitive sensor interface circuit based on phase differential technique. The circuit has been designed and fabricated using MIMOS' 0.35µm CMOS technology. Simulation and test results show linear characteristic from 36 – 52 degree phase difference, representing 0 – 100% in soil moisture level. Test result shows the circuit has sensitivity of $0.79mV/0.1^0$ phase difference, translating into resolution of 10% soil moisture level.

***Keywords*—**Capacitive sensor, interface, phase differential.

I. Introduction

IN the last decade, CMOS-MEMS micro sensor systems development has grown rapidly. The systems can measure many physical variables like position, accelerometer, angular speed and liquid level to detect the environmental changes [1]. Capacitive CMOS-MEMS sensors are widely used due to its high detection and low temperature sensitivity. However, due to the manufacturing limitation, the sensing capacitances are very small. Typically, these capacitances are on the order of femto-farads, and the noise from large parasitic capacitance, which is much greater than the sensor capacitance, would limit the detection sensitivity. Furthermore, the variations of the post-CMOS process can cause the capacitance mismatch. The mismatch of sensing capacitance would result in significant AC distortion in the output signal of the conventional demodulator. Hence, designing a low noise CMOS-MEMS sensing circuit is an important issue.

There are various methods used to detect the capacitance change. These include switched-capacitor based readout technique [2], relaxation oscillator [3], analog-to-digital conversion, diode-quad circuit, voltage (or current) to frequency (or time) conversion [4] and phase detection method [5].

The most common technique used for capacitive sensor's interface circuit is the switched-capacitor technique. Switched-capacitor technique converts the capacitance change to equivalent voltage level directly. It provides high resolution for capacitors in the presence of parasitic capacitances [6]. Main drawback for switched-capacitor technique is the process variation of the capacitors. Capacitor's process variation of ±10% could affect the readout circuit's accuracy and sensitivity. They are also prone to charge injection and clock feed-through problems.

In this paper, phase detection circuitry is used to design an interface circuit for Fringing Electric Field (FEF) soil moisture sensor. Phase detection technique determines the phase shift of a sinusoidal wave passing through the FEF sensor. The phase detection instrumentation has the advantage that it can detect a change of phase resulting from either change of effective resistance or capacitance of the soil dielectric [5]. Phase detection circuit is immune to the surrounding noise since it detects only the phase shift. Process variation does not have big impact on circuit performance since it does not contain any capacitor. The phase detection circuit can be designed such that it can be easily integrated with processing unit such as microprocessor.

This paper is divided into four additional sections. Principles of FEF sensing and circuit requirements are explained in section II and circuit implementation is presented in section III. Section IV presents simulated results, test result and physical layout. Finally, the conclusions are drawn in section V.

II. Architecture

A. FEF Moisture Sensor

FEF moisture sensor uses fringing field capacitance (Fig.1) configuration, rather than the well-known parallel plate capacitance configuration. The fringing field capacitance is used to project the sensing electric field into the surrounding material [7]. Fig. 1 shows the schematic of an interdigitated fringing electric field sensor connected to a voltage sensing circuit. When an AC voltage signal is applied to the driving electrodes, the sensor generates a fringing electric field. The field strength and distribution pattern depend both on the input voltage signal and the sensor geometry.

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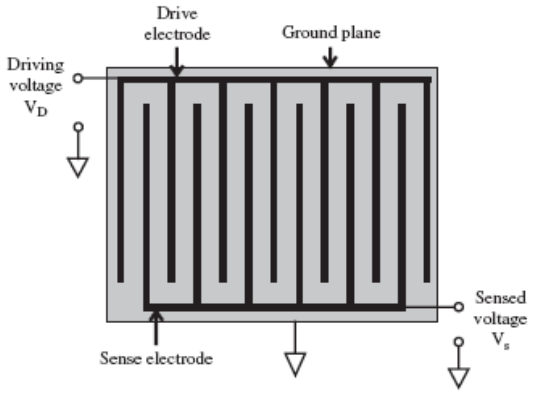

Fig. 1 Schematic representation of a fringing electric field sensor connected in voltage sensing configuration with its back plane grounded.

FEF sensor can be modeled as an RC network as shown in Fig. 2. Admittance (Y), relates to capacitance and conductance through the following equation.

$$Y = \frac{1}{Z_S} = j\omega C_S + G_S \tag{1}$$

Expanding the equation, Capacitance change can be a function of output voltage, input voltage, frequency, interface circuit load and phase-shift through the following equation.

$$C_S = \left(\frac{V_O}{\omega R_L (V_O - V_i)} \right) * \sin(\theta) \tag{2}$$

The equation (2) can be further simplified by setting all variables except phase-shift to be constant. As a result, a linear characteristic between capacitance change (C_s) and phase shift are shown in the following equation.

$$C_S = K * \sin(\theta) \tag{3}$$

When an AC sinusoidal signal is passed through FEF sensor, the signal will suffer phase shift depending on the values of its equivalent RC network. Since the phase shift imparted on the signal depends upon the soil permittivity, detection of phase gives a measure of soil moisture concentration. Sensor measurement shows that phase difference for dry soil is 52 degree while for water is 36 degree. Hence, conclusion can be made that phase difference is inversely proportional to soil moisture content and range from 36 to 52 degree is the phase difference which the interface circuit must be able to detect. In order to get accuracy of ~1% for the soil moisture reading in volumetric water content (VWC), accuracy of phase detection circuit must be 0.1 degree or better. Table I shows the requirement for FEF sensor interface circuit.

TABLE I
REQUIREMENTS FOR FEF SENSOR INTERFACE CIRCUIT

No.	Description	Specification
1	Phase detection range	36^0 - 52^0
2	Resolution	0.1^0
3	Number of points	160 points

III. CIRCUIT IMPLEMENTATION

Diagram of the proposed interface circuit is depicted in Fig. 2. It consists of 3 main components; phase detector, charge pump and low pass filter. An AC signal is supplied to FEF sensor and the same signal is compared with output from FEF sensor to detect any phase difference. Charge pump and low pass filter converts pulse width from phase detector circuit to equivalent DC voltage.

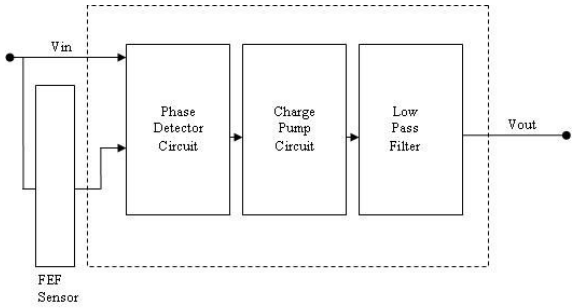

Fig. 2 Block diagram of FEF sensor interface circuit.

A. Phase Detector Circuit

A phase detector circuit is a frequency mixer or analog multiplier circuit. The phase detector circuit compares the output signal from the FEF sensor with the reference signal (Vin). In this design, a conventional Phase Frequency Detector (PFD) circuit has been used. The Vin signal is connected to **VINA** port in the PFD circuit whereas output signal from the sensor is connected to **VINB** port, as shown in Fig. 3.

The PFD circuit has four output ports, **UP**, **DN, UPB** and **DNB**. **UP** signal is a pulse signal, where the width of the signal is equivalent to the delay or phase difference between the two input signals. **DN** signal is a very small pulse to reset the current in charge pump circuit. The **UPB** and **DNB** signals are the inverted signals of **UP** and **DN**. The four signals will be connected to switches in charge pump circuit to control the current flow in the charge pump circuit. The PFD circuit is also more immune to the process, supply voltage and temperature variations since it comprise of CMOS digital components.

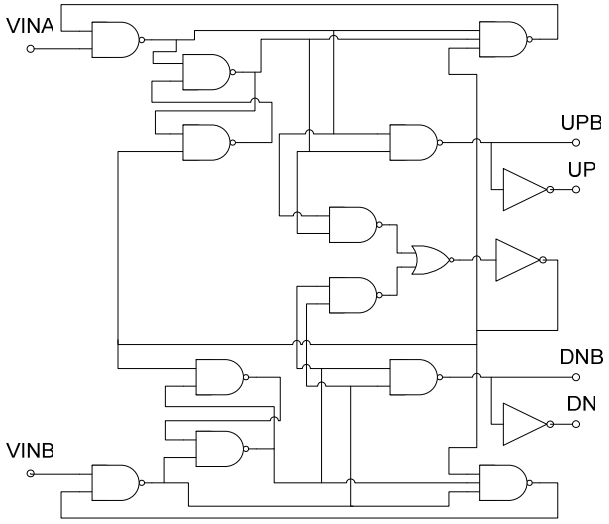

Fig. 3 Schematic representation of Phase Frequency Detector

B. Charge Pump Circuits

Charge pump circuit is a circuit consists of current source component and current sink component. The function of charge pump circuit is to control the current flow. It generates positive current levels in response to the frequency **Up** signal and negative current levels in response to the frequency **Down** signal. Each current source (UP1 and UP1A) and current sink (DOWN and DOWNA) draws and sinks 100µA of current. The net current provided by the charge pump is converted into DC voltage by the low pass filter.

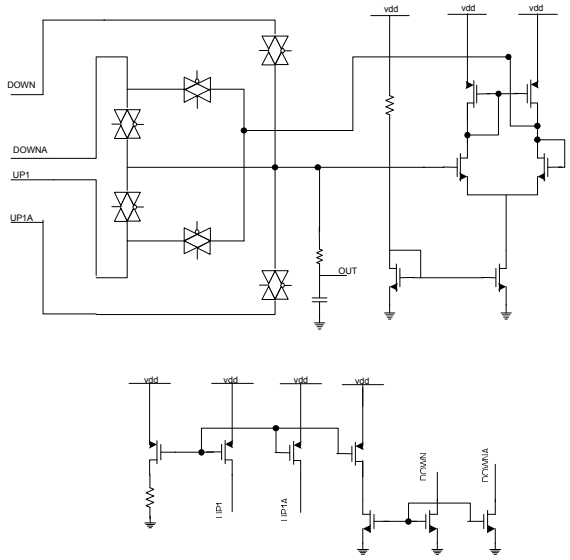

Fig. 4 Schematic representation of a charge pump circuit. © MIMOS Berhad

C. Low Pass Filter

The main function of low pass filter in this circuit is to convert current generated by charge pump into equivalent DC voltage. This circuit uses 1st order low pass filter as shown in Fig. 5 to extract the DC level and further suppress the noise level. The DC level of 1st order filter will carry phase difference which is related to soil moisture level.

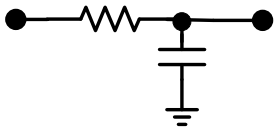

Fig. 5 Low pass filter circuit

IV. Simulation Results and Discussion

A. Simulation Results

This circuit is simulated using MIMOS' 0.35um CMOS process technology. Table II summarizes the performance of the designed FEF readout circuit in three process corners simulation; typical, worst and best case. Simulation result shows the circuit's ability to detect phase change of 0.1^0 producing output voltage difference of 0.8 mV per 0.1^0 phase difference.

TABLE II
Simulation Results for 3 Process Corners

Phase Difference	Vout		
	Worst	**Typical**	**Best**
	3.0 V	**3.0 V**	**3.6 V**
	90^0 C	**27^0 C**	**0^0 C**
36^0	**2.72000 V**	**2.44495 V**	**2.94643 V**
36.01	**2.72100 V**	**2.44503 V**	**2.94751 V**
Sensitivity	**0.0001 V**	**0.0008 V**	**0.00108 V**

Fig. 6 shows the worst case transient simulation for FEF readout circuit. Circuit's DC output range from 2.7 volt to 2.8 volt is simulated. The simulation shows that output signal is stable after 250ms.

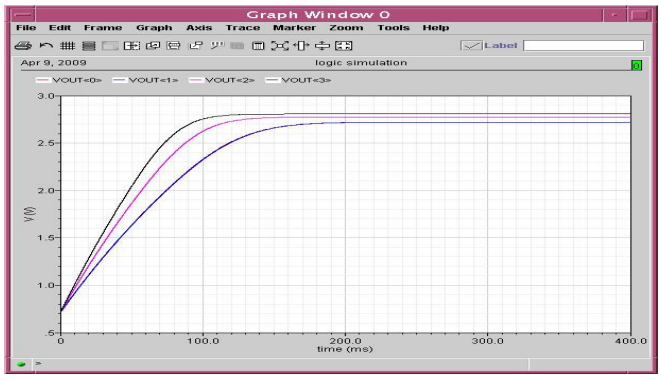

Fig. 6 Transient simulation result. © MIMOS Berhad

B. Test Results

Test results shows that the circuit has good linearity from 36– 52 degree phase difference as shown in Fig. 7. The change in phase is directly proportional to the output voltage with resolution of 0.79 mV/0.1^0. Fig. 8 shows the relationship between VWC and output voltage where output voltage is inversely proportional to the VWC. Layout of the design can be seen in Fig. 9.

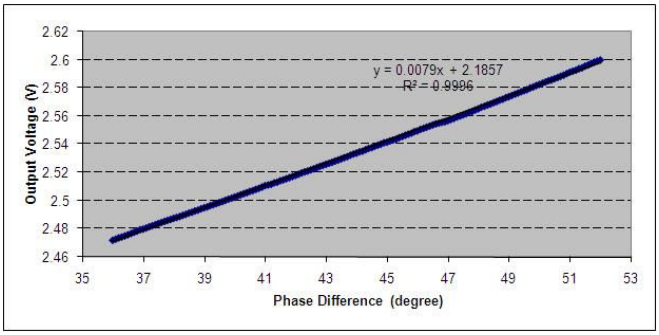

Fig. 7 Test result for output voltage vs. phase difference. © MIMOS Berhad

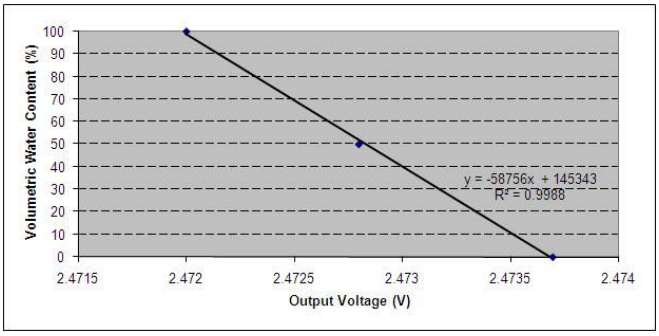

Fig. 8 Volumetric water content vs. output voltage. © MIMOS Berhad

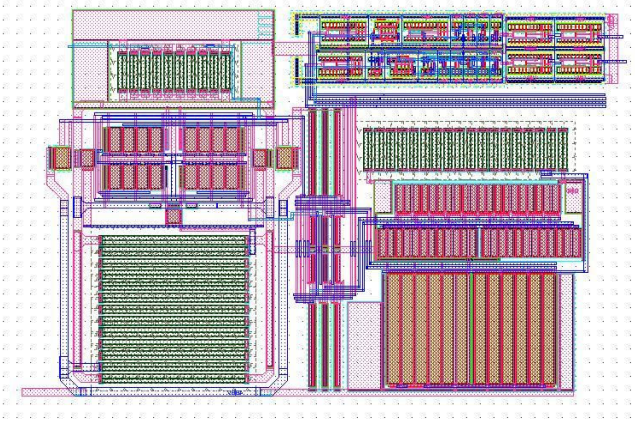

Fig. 9 Layout implementation of FEF interface circuit. © MIMOS Berhad

V. Conclusion

A readout circuit for FEF capacitive sensor based on phase differential technique has been designed and simulated using MIMOS' 0.35µm CMOS technology. In this design, type IV of phase frequency detector circuit is used together with charge pump and low pass filter to produce DC voltage proportional to phase difference. Simulation result shows a linear characteristic from 36 – 52 degree phase difference, representing 0 – 100% in soil moisture level. Sensitivity of 0.79mV/0.1^0 phase difference has been achieved, translating into resolution of 10% soil moisture level.

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