

Development of Manufacturing Simulation Model for Semiconductor Fabrication

Syahril Ridzuan Ab Rahim, Ibrahim Ahmad, Mohd Azizi Chik, Ahmad Zafir Md. Rejab, and
U. Hashim

Abstract—This research presents the development of simulation modeling for WIP management in semiconductor fabrication. Manufacturing simulation modeling is needed for productivity optimization analysis due to the complex process flows involved more than 35 percent re-entrance processing steps more than 15 times at same equipment. Furthermore, semiconductor fabrication required to produce high product mixed with total processing steps varies from 300 to 800 steps and cycle time between 30 to 70 days. Besides the complexity, expansive wafer cost that potentially impact the company profits margin once miss due date is another motivation to explore options to experiment any analysis using simulation modeling. In this paper, the simulation model is developed using existing commercial software platform AutoSched AP, with customized integration with Manufacturing Execution Systems (MES) and Advanced Productivity Family (APF) for data collections used to configure the model parameters and data source. Model parameters such as processing steps cycle time, equipment performance, handling time, efficiency of operator are collected through this customization. Once the parameters are validated, few customizations are made to ensure the prior model is executed. The accuracy for the simulation model is validated with the actual output per day for all equipments. The comparison analysis from result of the simulation model compared to actual for achieved 95 percent accuracy for 30 days. This model later was used to perform various what if analysis to understand impacts on cycle time and overall output. By using this simulation model, complex manufacturing environment like semiconductor fabrication (fab) now have alternative source of validation for any new requirements impact analysis.

Keywords—Advanced Productivity Family (APF), Complementary Metal Oxide Semiconductor (CMOS), Manufacturing Execution Systems (MES), Work In Progress (WIP).

I. INTRODUCTION

COMERCIAL semiconductor fabrication plan (fab) for CMOS process usually consists of hundreds of processing equipment, more than 35 percent of the process was re-

entrance at the same equipment [10]. The complexity encourage many literatures from practitioner perform manufacturing optimization analysis using available commercial software instead of develop software or platform what if analysis.

Yao et al. (2001) developed a simulation model using AutoSched AP to verify new preventive maintenance (PM) scheduling obtained from calculation of two layer hierarchical concept. New PM scheduling was configured in the AutoSched AP model for a week forecast to validate the opportunity to reduce PM frequency. Simulation result had shown that the research has successfully achieved 14 percent reduction of PM frequency by implementing the new PM schedule at their factory. Through this many assessments of potentials gains and benefits are easily identified used for fine-tuning before implement it in the real production environments. Gan et al.(2005) used AutoSched AP in High level Architecture (HLA) simulation model to develop a Borderless Fab model that comprise of two factories model. The integration of both models as borderless fab simulation model was used for study the opportunity of improving production performance. They also found that, the models simulate time is ten times better to straightforward application of the HLA Simulation time Infrastructure's using similar hardware configuration. Klein and Kalir (2006) used AutoSched AP to develop fab transient model to study the effect of ram-down 0.18- μm logic and ramp-up 90nm flash product at Intel's Fab-18. This study was attempted to understand the effect of one-of-a kind equipment to the overall Fab cycle time [1].

AutoSched AP is widely used in semiconductor fabrication [2]. In this paper, the AutoSched AP is customized with the integration of current factory database which known as Manufacturing Execution Systems (MES) and Advanced Productivity Family (APF). Data from MES was extracted and re-arranged using APF to match the required parameters and acceptable formats for AutoSched AP to process. Usually this stage will take the longest time spent during the development period, since it required a lot of understanding on the data definitions, validation of data collection with real situation and challenging in codes language its logical function[5]. Once the model is integrated with the right information, the simulation model now able to execute and produce required results. The results are saved in the output files.

The output files are then customized with APF codes to develop proper reports analysis which later attempt for

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analysis to use for optimization in what if analysis. This study used AutoSched AP version 10.0.1 and APF version 7.8.0 software. AutoSched AP is the commercialize software known as off-the shelf simulation packages (CSPs) for industrial practitioner [2].

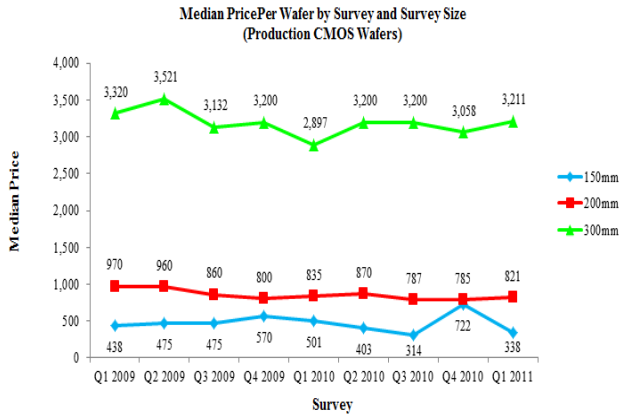


Fig. 1 Average price per wafer by quarter and wafer size (Production Wafers), GSA Wafer Fabrication Pricing Reports, April, 2011 [9]

The simulation software was integrated with existing MES systems using APF software. All of MES data is stored in the Cycle Time Database (CTDB) and MES database (MESDB). APF is used to extract data from this databases and structured the data into respective format and parameters according to AutoSched AP requirement. The information from this customized includes overall WIP details, routes and its associated wafer per hour (wph), equipment PM calendar and equipment restriction notice. The results then reproduced and categorized according to the respective categories such as trend chart for equipment utilization, daily output from the equipment or moves, forecast for WIP projection at respective area and forecast output per month.

The next discussion in this paper outlined as follows: Section II will discuss on simulation model development, include architecture for the integration simulation model with MES and APF. Section III will discuss about simulation model validation. Further analysis also performs to compare forecast in simulation model versus actual and its gap analysis. Section IV will continue discuss on the simulation result and the application towards current production environment. Last but not least, section V will conclude the research achievements and propose the future action plan to improve the simulation model to next level.

II. SIMULATION MODEL

Philips (1998) categorized AutoSched AP simulation model into two categories. First is for analytical models, for analysis of dispatching rule and planning decision. Second is the operational model, for scheduling and production control activity [3]. In this research, the simulation model is developed for operational model purposes. A simulation model in general consists of input data, AutoSched AP software, output data and the results analysis as shown in Fig.

2 below. The activities for the simulation model are controlled through the integration of Advanced Productivity Family scheduling and data analysis software (APF), Manufacturing Execution System (MES) database, cycle time database and AutoSched AP as illustrated in Fig. 3. During the simulation model run, APF first executes the commands to compile the input information for AutoSched AP. After the compilation completed, the APF launches the AutoSched AP to run for the defined simulation period. Once the AutoSched AP run is finished, APF again instructs the commands to collect the desired statistics from the AutoSched AP output and constructs the analysis report.

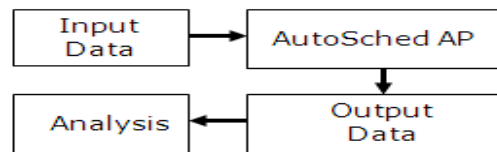


Fig. 2 Overview of simulation model

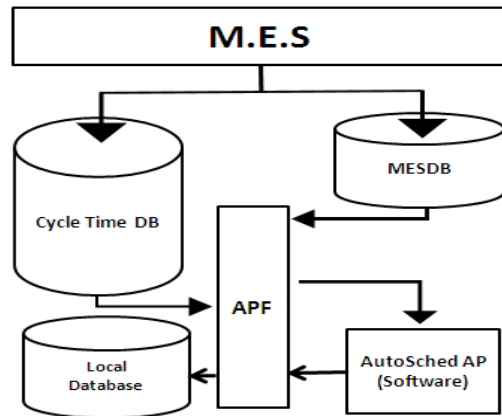


Fig. 3 Simulation model architecture

The input data consist of manual configured parameters and real-time information collected from MES and cycle time databases. The main input data are equipment configurations, equipment availability, order file, current WIP profile and route file as shown in Fig. 4.

The equipment configurations are defined in the equipment file. The simulation model includes all processing and metrology equipment, which are grouped under equipment family based on the equipments processing capability. The model also includes equipments that can perform batch processing such as for cleaning and furnace for respective deposition. Batching configurations such as minimum and maximum batching size and maximum waiting time to complete a batch are configured in this file.

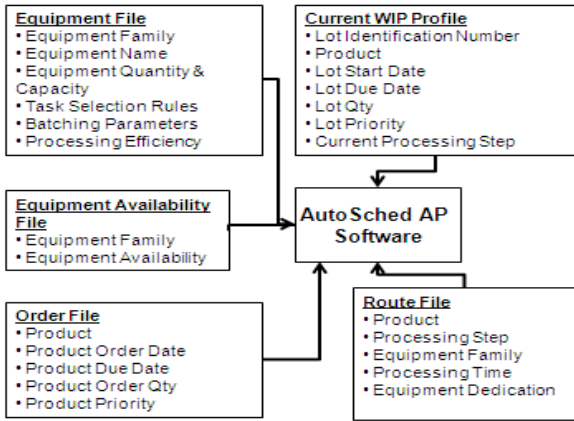


Fig. 4 Simulation model input data

In the situation when more than one lot arrive at the same equipment family, the model uses rules and ranks to determine which lot to be selected next when the equipment becomes free [4]. As an example, rule_SSU (same setup), determines the lot selection based on similar equipment setup. Examples of ranks are rank_EDD (earliest due date) and rank_LP (lowest priority), which means that the lot with the earliest due date is ranked first and the lot with the lowest priority level is ranked first, respectively. Multiple ranks can be specified, meaning that the task list is ranked according to the first ranking criteria, and the subsequent rank is used to break any tie. The equipment availability or uptime are collected based on past 6 month historical data with reference to SEMI E10 equipment states stack chart shown in Fig. 5.

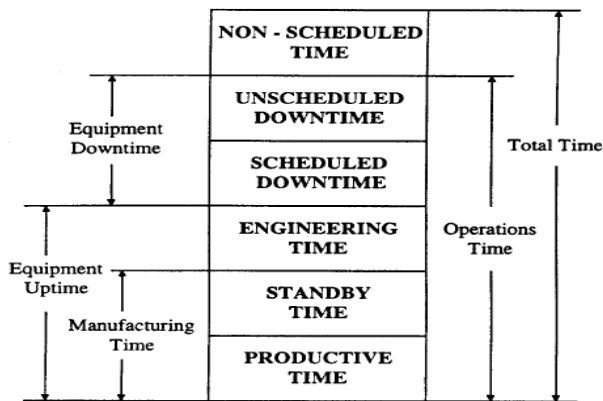


Fig. 5 SEMI E10 equipment states stack chart [11]

The order file has the information for the current and future orders to be started into the fab. The continuity of wafer starts per week is scheduled in the order file with 8-minute-interval between the lots started. Once all the input configurations are in place, the simulation model now ready for production use. The simulation model begins with the current WIP profile that is retrieved by APF from MES to show the status of the WIP. The contents of order file and WIP profile are shown in Fig. 4. A route file contains the processing information for each product such as the processing steps, processing time and

processing equipment family. A route file has more than 60 different product routes and each product route has 300 to 800 processing steps. The processing time for each step is defined based on the study of the past 6 months data. Each step is also assigned to the respective equipment family. In the situation when more than single equipment can process a step, alternate equipment family is specified. In a situation when there are different capabilities for equipment within an equipment family, the name of the equipment that can or cannot be dedicated to process a step is defined as station specification (STNSPEC) or station exception (STNEXC) respectively [8]. This situation is also called as one-of-a-kind equipment condition.

Prior the simulation model execution, these input files are compiled by APF to produce the input data for AutoSched AP. AutoSched AP then produces output files, that can be further analyzed using APF or other commercial data analysis software. Equipment output file summarizes the equipment states during simulation period such as percentage of processing, idling, or conducting preventive maintenance. There is a schedule report file that traces detailed breakdown of each processing activities that individual lot goes through during the simulation. This report is also used to calculate the quantity that is completed from the equipment. Another output is lot report that not only tracks each lot start date, completion date and quantity, but also provides the lot location at the end of the simulation period. There is also performance report that summarizes the WIP quantity at every defined period. Finally, further analysis can be conducted on the output results generated from the simulation model run, such as on short interval scheduling, forecasting WIP profile or investigating fab performance.

III. MODEL VALIDATION

Simulation model were simulate for more than 30 days. Thus, warm-up period was not required because it already considered the current WIP in the production. Results from the simulation model were compared with the actual Fab operation to validate the accuracy of the model by using APF [7]. Actual operational data were collected from MES database such as: Move, WIP Quantity, and Equipment Uptime. Total throughput or wafer moves is validated.

The accuracy equation in this analysis was based on

$$1 - (100\% \times |(Forecast - Actual) / Actual|) \quad (1)$$

the model went through continuous improvement in order to reach the desired accuracy [6]. Actions taken include ensuring the proper operation are match with actual travel times, operator availability, dispatching policies, WIP performance and revisit the cycle time data. Finally the model achieved average accuracy of more than 95 percent over 30 days of simulation period for all of the process area as illustrated in Fig. 6. This model qualified to be used for scheduling and production control activities.

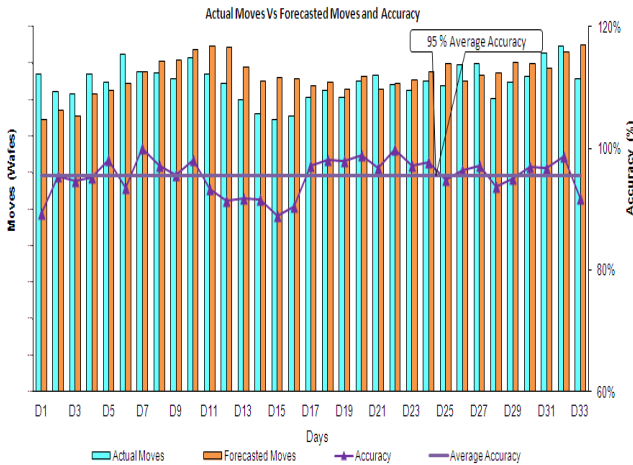


Fig. 6 Moves comparison actual versus forecast

IV. SIMULATION RESULT AND DISCUSSION

Simulation model is used to perform what if analysis in the daily manufacturing strategy. One of the what if analysis is the analysis to studies the impact of new priority request to the original quarterly output and cycle time commitments. Re-prioritization WIP analysis is needed when respective customers request to have an early delivery date compared to the original due date. This analysis usually, requires the information of the current respective WIP location in the production as shown in Fig. 7 below to understand the impact of overall output and cycle time. Respective WIP data were collected from MES and generated from APF report to perform this analysis.

DPML (day per mask layer) is defined as days take to complete one mask layer, which normally most semiconductor fabrication performs at 1.8 DPML [11], [12].

$$DPML = \text{Days} / \text{Masking layer} \quad (2)$$

For example, if the remaining mask left is 10, then based on generic 1.8 DPML, the remaining completion cycle time is 18 days. According to historical data collection, the cycle time or DPML is varies for respective location of masking layers.

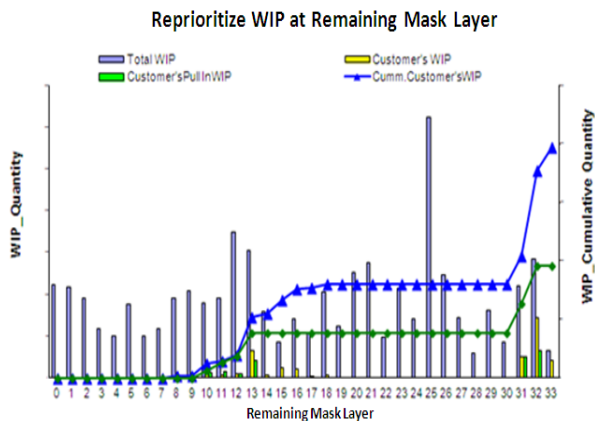


Fig. 7 Respective WIP at remaining mask layer

Through the formulation above and real data in the factories, remaining WIP is then calculated roughly to estimate the cycle time to map the proper strategy to apply for parameter changes in the simulation model. Usually for this type of analysis, the baseline analysis is based on normal parameters condition. Few parameter changes will be made either increase the priority requirements, changed in due date, PM frequency, wait time for batching, recipe dedication and transportation time. Usually up to 10 simulation trials will satisfy the decision to finalize the best strategy. The respective scenario that provides the optimal result was selected as the proposal method to be implemented in the operation as shown in Fig. 8. In this analysis, the selected strategy helps to meet the required objective, while improving overall cycle time by 10 percent and wafer output quantity by 8 percent.

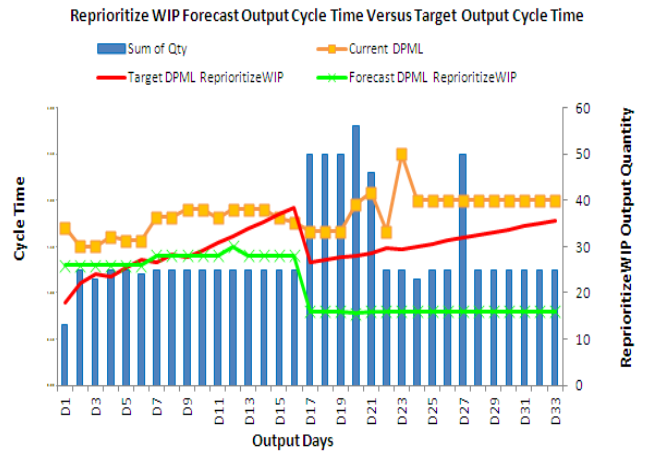


Fig. 8 Respective reprioritize WIP analysis

This example demonstrates the importance of having the right simulation model to perform several analyses regarding WIP to support decision making to convince customer related to production performance.

V. CONCLUSION

This paper demonstrates that the development of this simulation model is successfully implemented. It is needed and important since its help to provide general overview to understand the impact when new changes needed to be made. Approach used to integration of AutoSched AP with MES and APF help to reduce longer times taken to prepare the simulation model prior to perform any analysis. Results from this research, successfully make the model to be used daily in the factory to provide guidelines for strategy planning.

VI. RECOMMENDATION AND FUTURE STUDY

There are many more scenarios that the simulation model can help to perform the analysis. Implementation in the real industry cases help to improve the model and understand many features and function that available in the model.

Among the potential projects for this simulation model to perform include

1. Capacity validation analysis
2. Cycle Time and Utilization and WIP
3. Loading plan and its estimated cycle time
4. Optimum Priority Analysis
5. Optimum Dispatching Analysis
6. PM Scheduling frequency
7. Batch sizes
8. Impact when equipment is not available
9. Operators requirements
10. Cycle Time improvement
11. Process flow changes

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REFERENCES

- [1] Moti Klein and Adar Kalir, "A Full Factory transient Simulation model For The Analysis of Expected Performance in A Transition Period," in *Proc. winter simulation Conf.* Israel, 2006.
- [2] Boon Ping Gan, Peter Lendermann, Malcolm Yoke Hean Low, Stephen J. Turner, Xiaoguang Wang and Simon J.E. Taylor "Interoperating AutoSched AP Using The High Level Architecture," in *Proc. Winter Simulation Conf.* Singapore, 2005.
- [3] Tyler Philips, "AutoSched AP by AutoSimulations," in *Proc. Winter Simulation Conf.* U.S.A, 1998.
- [4] Ingy A. El-Khouly, Khaled S. El-Kilany, and Aziz E.-Sayed, "Effective Scheduling of Semiconductor Manufacturing", *World Academy of Science, Engineering and Technology*, vol. 79, 2011.
- [5] Kader Ibrahim, Mohd Azizi Chik and UdaHashim, "Variability Due to Tool Configurations That Impacts Overall Capacity in Wafer Fabrication Facility" *The 11th Asia Pacific Industrial Engineering and Management Systems Conference*, Melaka, 2010.
- [6] YudhaAndrianSaputra&StefanusEkoW., "Combination of MAPE, MedAPE, and Skewness of APE", *Industrial Engineering And Service Science (IESS) International Conferenc*, SOLO.2011.
- [7] Ben H. Thacker, Scott W. Doebbling, Francois M. Hemez, Mark C. Anderson, Jason E. Pepin and Edward A. Rodriguez, *Concepts of Model Verification and Validation*. California, CA: United States Department of Energy, 2004, pp.17-21.
- [8] Applied AutoSched AP. 2011. AutoSched AP Release Note v 10.0.1.
- [9] Global Semiconductor Alliance (GSA), Semiconductor Market Overview, April 2011.
- [10] Mohd Azizi Chik, Mohd Hazmuni bin Saidin, and Uda bin Hashim, "Industrial Engineering Roles in Semiconductor Fabrication", *APIEM 11th Conf. December* 2010.
- [11] R. C. Leachman, D. A. Hodges, "Benchmarking Semiconductor Manufacturing," *IEEE Trans. on Semiconductor Manufacturing*, TSM-9 (May 1996), pp. 158-169.
- [12] Mohd Azizi Chik, Yeo EngTeck, Mahalil Amin AbdMalek, and Mohd HafidzSaidi, "Comprehensive Sequencing Dispatching Method for Identified Bottleneck Tool – Photolithography Process", *NSM, Perlis, Malaysia*, pp.19-21. 2003.

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