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Overview of Multi-Chip Alternatives for 2.5D and 3D Integrated Circuit Packagings

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***Abstract*—**With the size of the transistor gradually approaching the physical limit, it challenges the persistence of Moore's Law due to such issues of the short channel effect and the development of the high numerical aperture (NA) lithography equipment. In the context of the ever-increasing technical requirements of portable devices and high-performance computing (HPC), relying on the law continuation to enhance the chip density will no longer support the prospects of the electronics industry. Weighing the chip's power consumption-performance-area-cost-cycle time to market (PPACC) is an updated benchmark to drive the evolution of the advanced wafer nanometer (nm). The advent of two and half- and three-dimensional (2.5 and 3D)-Very-Large-Scale Integration (VLSI) packaging based on Through Silicon Via (TSV) technology has updated the traditional die assembly methods and provided the solution. This overview investigates the up-to-date and cutting-edge packaging technologies for 2.5D and 3D integrated circuits (IC) based on the updated transistor structure and technology nodes. We conclude that multi-chip solutions for 2.5D and 3D IC packaging can prolong Moore's Law.

***Keywords*—**Moore's Law, High Numerical Aperture, Power Consumption-Performance-Area-Cost-Cycle Time to Market, PPACC, 2.5 and 3D-Very-Large-Scale Integration Packaging, Through Silicon Vi.

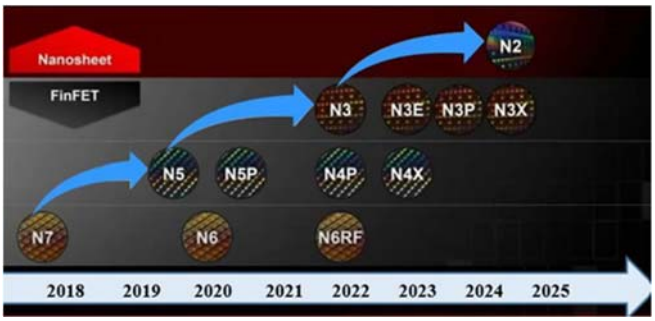
I. Background

FOLLOWING the transistor size gradually approaching the physical limit, it has challenged the continuation of Moore's Law [1]-[3], driving the demand for high NA lithography equipment and solving looming dilemmas like quantum tunneling issues [4], [5]. While the technical requirements of portable devices and HPC are growing, expecting the law's persistence to improve the chip density will no longer make headway in the semiconductor industry. The PPACC is an up-to-date criterion to drive progress in the advanced nm wafer process [6]. The emergence of stereoscopic stacking IC assembling according to TSV technology has replaced traditional die packaging approaches and granted the solution.

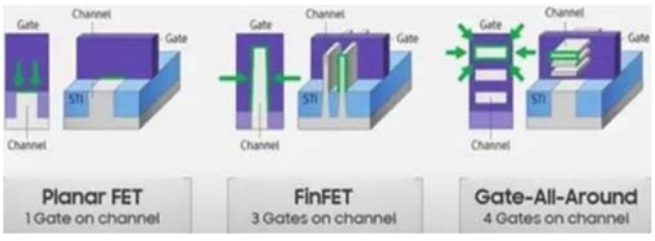
II. Technical Review

A. Evolutions of Transistor Structure and Technology Node in Wafer Process

Moore's law describes that the technical nodes of the wafer process double the chip transistor number every 18 to 24 months [1]-[3]. It has dominated the development of semiconductors. However, when the engineers reduce the transistor's gate width (electron channel length) to 20 nanometers (nm), effects such as threshold voltage drop of the control switch, reduction of the drain potential energy barrier, carrier surface scattering, electron velocity saturation, ionization, and thermionic effects will occur [7]-[9]. Consequently, some large-scale foundries, such as Intel, TSMC, and Samsung, have adopted Fin Field-effect Transistor (FinFET) and Gate-All-Around FET (GAAFET) to cope with evolving technical bottlenecks to persist in the rule. Below 3 nm, the physical limits are significantly constraining [4]. Relying on chip-scaling to continue the law is a huge challenge. PPACC trade-offs for chips is an updated criterion driving advanced wafer nanometer (nm) development. Fig. 1 shows technical development from 7 nm (N7) to 2 nm (N2) and the transistor structures of the various wafer processes. Fig. 2 illustrates the evolution of chip structure under TSMC's technology node evolution (Fig. 2 (a)), the change of transistor's body thickness to mobility (Fig. 2 (b)), the change of gate length to subthreshold swing (Fig. 2 (c)), the change of technology node and gate length to transistor number (Fig. 2 (d)), and the effect of Van set Waals (vdW) contacts inside ultra-thin body silicon on insulator (Fig. 2 (e)).



(a) Industry-leading Advanced Technology Portfolio



(b) Evolution of Transistor Structures

Fig. 1 Transistor Structure development [5]; > 20 nm: MOSFET; < 20 nm: FinFET; < 3 nm: Gate All Around Fet (GAAFET)

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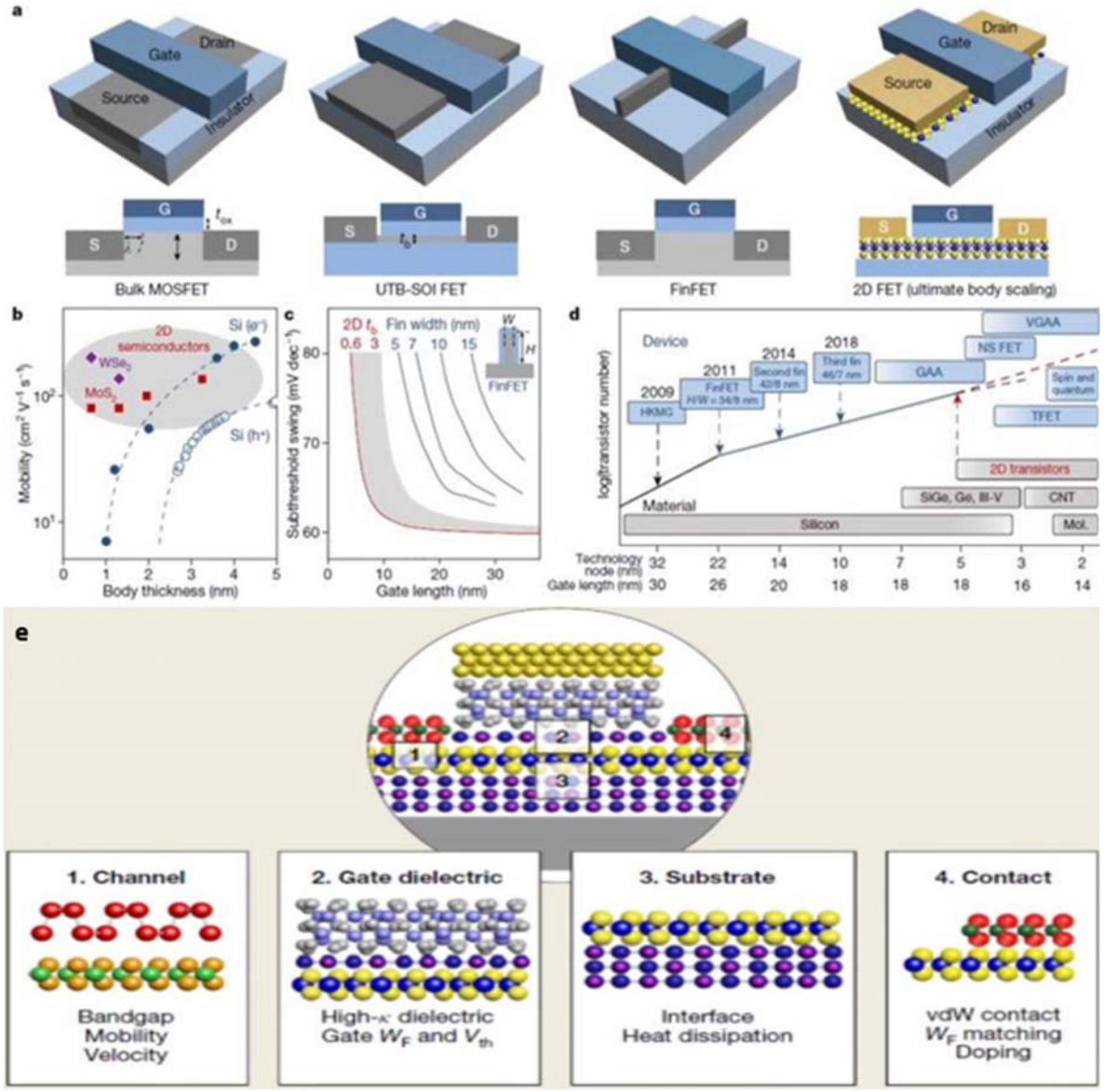


Fig. 2 TSMC's technology node evolution [5]; UTB-SOI: Ultra-thin body Silicon on Insulator; Van der Waals (vdW) Contacts

TABLE I
TSMC'S PPA CHANGES UNDER DIFFERENT PROCESSES [5]

	TSMC			
	N5 vs N7	N3 vs N5	N3E vs N5	N2 vs N3E
Power	-30%	-25-	-34%	-25-
Performance	+15%	30%	+18%	30%
Chip Density*	?	?	~1.3X	>1.1X
Volume	Q2	H2	Q2/Q3	H2
Manufacturing	2022	2022	2023	2025

Note: Chip density of the mixed chips containing 50% of logic, 30% SRAM, and 20% analog (TSMC).

Table I shows the changes in the power consumption-performance-area (PPA) of TSMC under different processes. From the comparison of N3E (Node 3E) and N5, and N2 and N3E, the chip density only increased by 30% and more than 10%, respectively (Fig. 3). It challenges foundries to continue Moore's Law. With the exponential cost increase, it defies to raise the chip density. The investment risk will be higher if manufacturers consider the wafer production yield and the increasingly rare customers' pyramid-shaped situation. It is challenging to regulate the timeframe for a leading manufacturer. In this context, in addition to gaining a better market share ahead of its rivals, it has spawned technological innovation to optimize PPA and generate state-of-the-art techniques that meet customer needs. For example, TSMC's N3 includes N3, N3E, N3P, and N3X. TSMC further divides N3E into three processes, 2-1Fin, 2-2 Fin, and 2-3 Fin, based on the same chip to satisfy customers' design flexibility (Fig. 4) and PPA requirements [5].

To echo the requirement of epoch-making technology, the wafer producers generally use two methods to endure the regulation: Introduce EUV (extreme ultraviolet lithography) and transfer circuit patterns to wafers through high-energy, short-wavelength light sources [10]. Another approach is to stack crystals vertically through "heterointegration" [11]-[13].

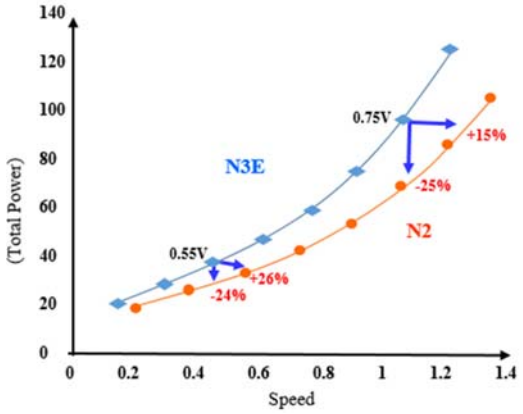


Fig. 3 Comparison of performance and Power Consumption of N2 and N3E, Cortex-A72 [5]

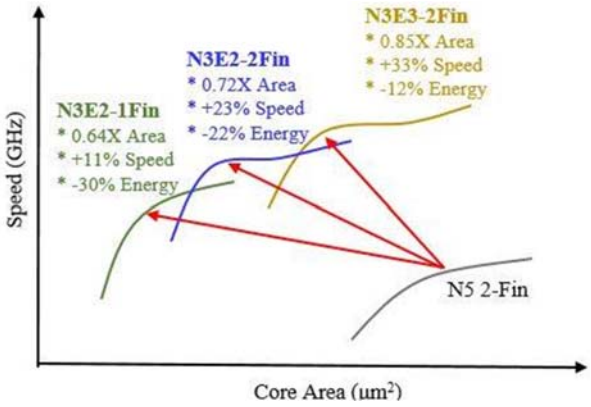
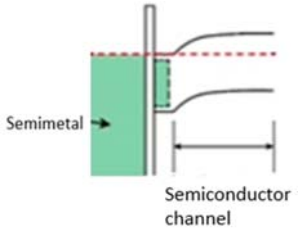


Fig. 4 From Vmax/Fmax to low-Vdd/power-efficient compute cores-all on the same die [5]

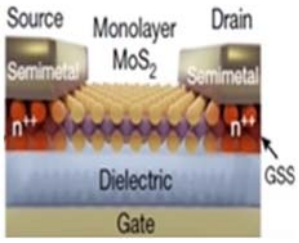
For heterogeneity, manufacturers rely on advanced packaging technology to integrate chiplets with different properties and functions and stack them in 2.5D or 3D packaging. The advantage is that it can package processors, memory, communication, sensing, and even laser chips. These heterogeneous chiplets and materials in the same IC enhance the function of the chip module, save the printed circuit board (PCB) area, and facilitates complementary properties between dissimilar materials. Under the premise that the semiconductor industry has clarified this development trend, the future wafer foundry industry is essential for integrating heterogeneous chiplets and advanced packaging, which can also improve the IC's PPA. As a high chip area reduces yield, the solutions to stack the chips help reduce them interconnect length. The overall wafer decreases delay and increases speed and performance [4]. This possible solution could be a paradigm shift in the present and future fabrication process, creating a new era of chip fabrication architecture and continuing the guideline.

With the emergence of 3D VLSI, although it provides solutions to increased speed and lessened power consumption, it also presents challenges that differ from traditional single-chip packaging. Chip assembly equipment is one of them. As any error will affect the yield of the production line and even cause the product of the entire production line to be defective, it must retain high precision, machine shock resistance, and intelligent management to ensure machine stability and product quality while maintaining high-speed operation.

As mentioned earlier, when the designer shrinks the transistor's gate length to 20 nm, effects such as threshold voltage drop of the control switch, reduction of the drain potential energy barrier, carrier surface scattering, electron velocity saturation, ionization, and thermionic effects will occur. To overcome these technical dilemmas, manufacturers introduce costly lithography equipment in hundreds of millions of US dollars, such as Deep Ultraviolet (DUV) with a wavelength of 193 nm and Extreme Ultraviolet (EUV) with a wavelength of 13.5 nm. Massachusetts Institute of Technology (MIT), TSMC, and National Taiwan University (NTU) (2021) [14] discovered that optimizing the bismuth (Bi) deposition process in two-dimensional materials and using Helium-ion beam lithography can approach the quantum limit to make the metals the transistor reaching ohmic contact (meager resistance). A stable ohmic contact with low resistance and a linear and symmetrical current-voltage characteristic curve (I-V curve) is a critical factor affecting the performance and stability of the current-voltage characteristic curve of an IC. It improves the current transmission between the source and drain and successfully narrows the device channel to nanometers (Fig. 5) [14]. In addition to DUV and EUV, other corresponding equipment and wafer tape-out prices remain high. Consequently, except for a few companies, such as Apple, Intel, and Samsung, only minimal corporations have a few product varieties, and a substantial global market share can be affordable and outsourced.



(a) Ohmic contact



(b) Degenerate part of Bi-contacted MoS2 marked in orange color due to gap-state situation (GSS)

Fig. 5 Schematic of a 2D FET with a monolayer semiconductor (MoS2) channel and semimetal (Bi) contacts [14]

Lapedus'es (2018) survey showed that the expenses of developing a 3 nm chip could be as high as US$1.5 billion (Fig.

6). However, the benefits of PPA are likely to decrease. International Business Strategies (IBS) [15] also noted that the 5 nm development cost exceeds US$ 542 million. Thus, the business and financial risks of foundries and fabless firms will increase momentously; the development of 2.5D and 3D heterogeneous stacked packaging seems essential [15].

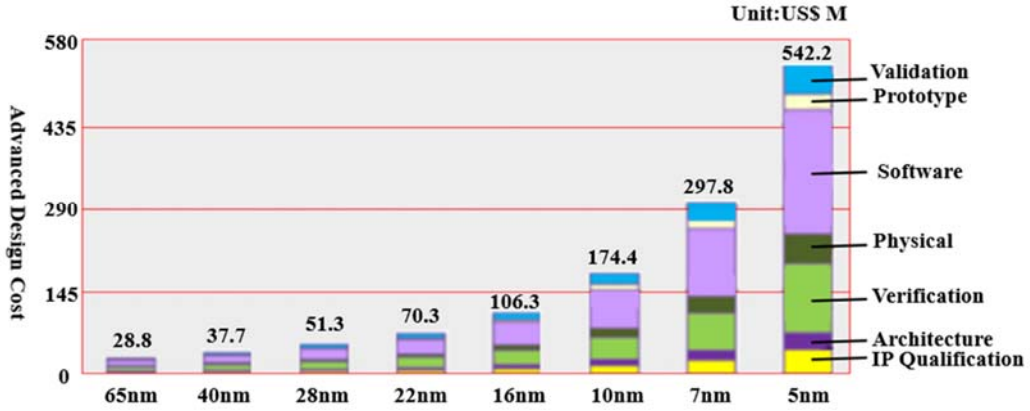


Fig. 6 IC design costs escalate [15]

B. Multi-Chip Alternatives for 2.5D and 3D Chip Assembly

Multi-chip alternatives have various structures, such as 2.5D, Embedded Multi-Die Interconnect Bridge (EMIB), Fan-out wafer-level packaging (FOWLP), Fan-Out Panel Level Packaging (FOPLP), Integrated Fan-Out (InFO) Wafer Level Packaging, Chip on Wafer on Substrate (CoWos), Small Outline IC (SOIC), System in Wafer-Level Package (SiWLP), and Embedded wafer fan-out (eWFO) to assemble the chips and formulate new architectures [16].

The 2.5D is a packaging methodology for including multiple dice inside the same package (Fig. 7) [17].

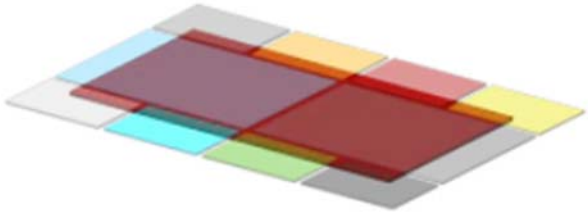


Fig. 7 Industry Standard 2.5D [17]

EMIB is an elegant and cost-effective approach to in-package high-density interconnect heterogeneous chips. The substrate fabrication process embeds a tiny bridge die with multiple routing layers (Fig. 8) [18], [19].

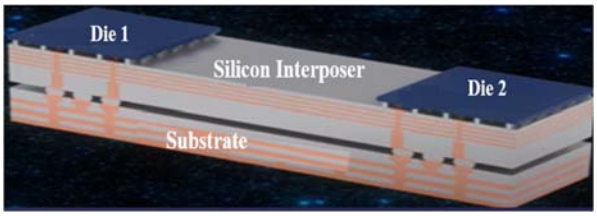


Fig. 8 EMIB [19]

FOWLP is an IC packaging technology that enhances standard wafer-level packaging (WLP) solutions (Fig. 9) [20]. In fan-out WLP, the wafer is diced first. However, the dies are precisely re-positioned on a carrier wafer or panel, with space for fan-out kept around each die. The carrier is then reconstituted by molding, making a redistribution layer (RDL) atop the entire molded area (both atop the chip and the adjacent fan-out area), and then forming solder balls [21].

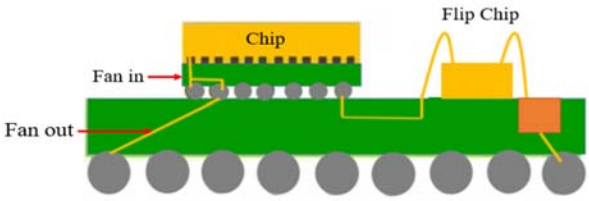


Fig. 9 FOWLP [20]

FOPLP is one of the latest packaging trends in microelectronics (Fig. 10). It has a high potential for significant package miniaturization concerning volume and thickness. The technological core of FOWLP is the formation of a reconfigured molded wafer combined with a thin film RDL to yield an SMD-compatible package [22], [23].

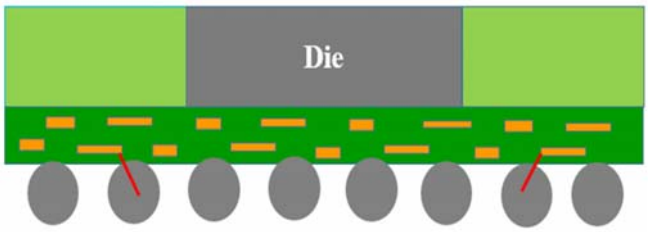


Fig. 10 FOPLP [22]

InFO is an innovative wafer-level system integration technology platform featuring a high-density RDL and TIV (Through InFO Via) for close interconnection and performance for various applications, such as mobile and HPC. Fig. 11 shows the architecture of InFO_POP architecture. There are

two different die types, a System on a Chip (SOC) and a Dynamic Random Access Memory (DRAM) in the case of InFO. Each may utilize a different feeding source, potentially with one device fed directly from the wafer and another from the Joint Electron Device Engineering Council (JEDEC) tray [24], [25].

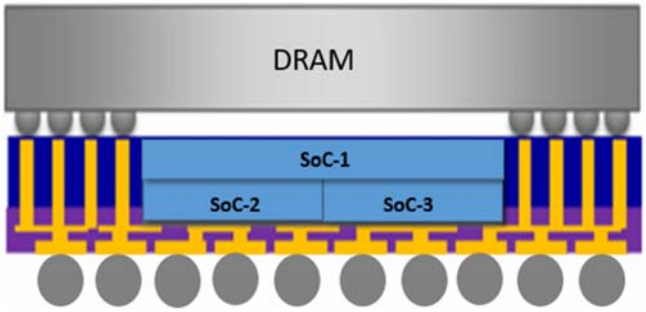


Fig. 11 InFO_POP Architecture [25]

Fig. 12 shows the architecture of CoWoS$^{\circ,R}$. It is a 2.5D wafer-level multi-chip packaging technology that incorporates multiple dies on a silicon interposer to achieve better interconnect density and performance. Individual chips are bonded through micro-bumps on a silicon interposer, forming a chip-on-wafer (CoW). Then thin CoW so that the TSV perforations are exposed, followed by Controlled Collapse of Chip Connection (C4) bumps formation and singulation. Makers can complete a CoWoS package through bonding to a package substrate [26], [27].

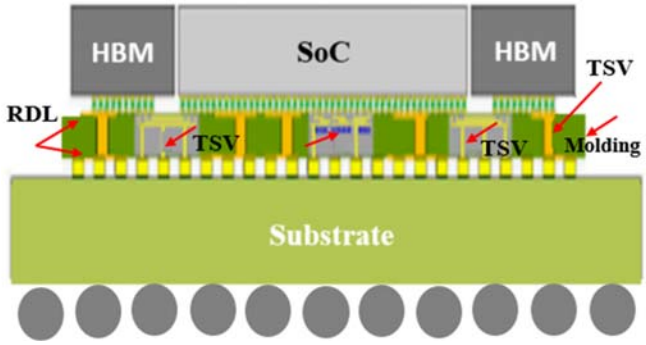


Fig. 12 CoWoS$^{\circ,R}$ Architecture [26]

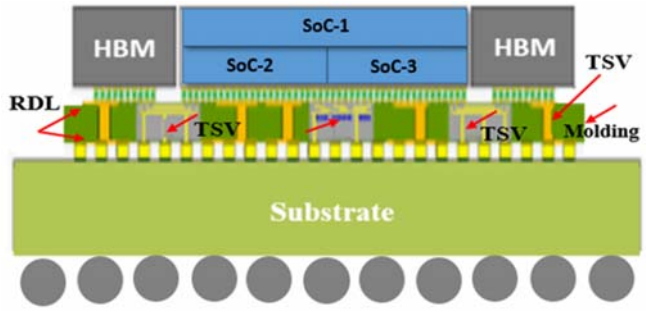


Fig. 13 CoWoS® Architecture of TSMC-SoIC [28]

Fig. 13 [28] shows that a surface-mounted integrated circuit (SoIC) package occupies an area of about 30-50% less than an equivalent dual in-line package (DIP), with a typical thickness being 70% less [29], [30].

Fig. 14 [31] illustrates the system's architecture in a wafer-level Package (SiWLP). It is fabricated using "RDL-first" technology for fan-out wafer-level packages (FO-WLPs) and provides the density of the high Chip-Input/Output (I/O), design flexibility, and package miniaturization [32], [33].

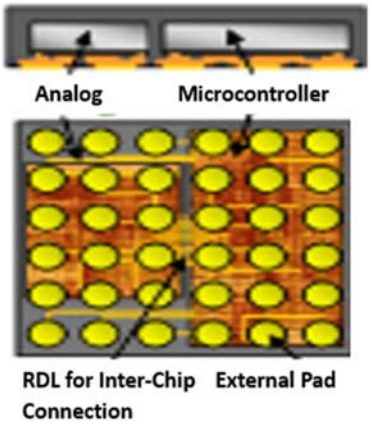


Fig. 14 SiWLP Architecture [31]

Embedding wafer and fan-out (eWFO), shown in Fig. 15 [34], is assembled in either wafer fabs using back end of line (BEOL) tools, materials, and processes or Outsourced Semiconductor Assembly and Test's (OSAT's) built-up fabs and tools [35], [36].

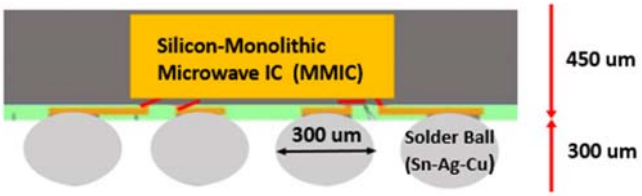


Fig. 15 Infenion's eWFO for 77 GHz Automotive radars [34]

C. Cutting-Edge Packaging Technology

Due to the high investment cost in the advanced wafer process, the short channel effect and the nonlinear Schottky contact issues are challenging to overcome. So far, only TSMC, INTEL, and Samsung can invest in foundries below 7 nm (inclusive). Intel's EMIB (2.5D) and Foveros (3D) packaging technologies are similar to TSMC [37], [38]. They are more applicable than Samsung's 3D high-bandwidth memory (HBM) stacking technology to product heterogeneity as they can widely assemble various heterogeneous chips to achieve better power consumption, performance, area, cost, and cycle time to market (PPACC) [39]. Nevertheless, Samsung encapsulates 12-layer HBM chips in a package with a thickness of only 720 µm. Researchers [40] consider it one of the most challenging technology. A common feature of the three foundries' wafer stacking technology is the extensive use of TSV technology.

1. TSMC's 3DFabric

Fig. 16 illustrates the evolution of TSMC from 2D InFO to 2.5D CoWoS and then to 3D SoIC InFO packaging. Off-chip coupling (Fig. 17) has higher interconnection and specific capacitance densities with ultra-low bonding latency for energy-efficient computing systems. It brings the merits of the large reticle size in fan-out and performance in HPC and AI networks. Fig. 18 shows that the SoIC™ bonding pitch is intrinsically exceptional to conventional 3D IC packaging [17].

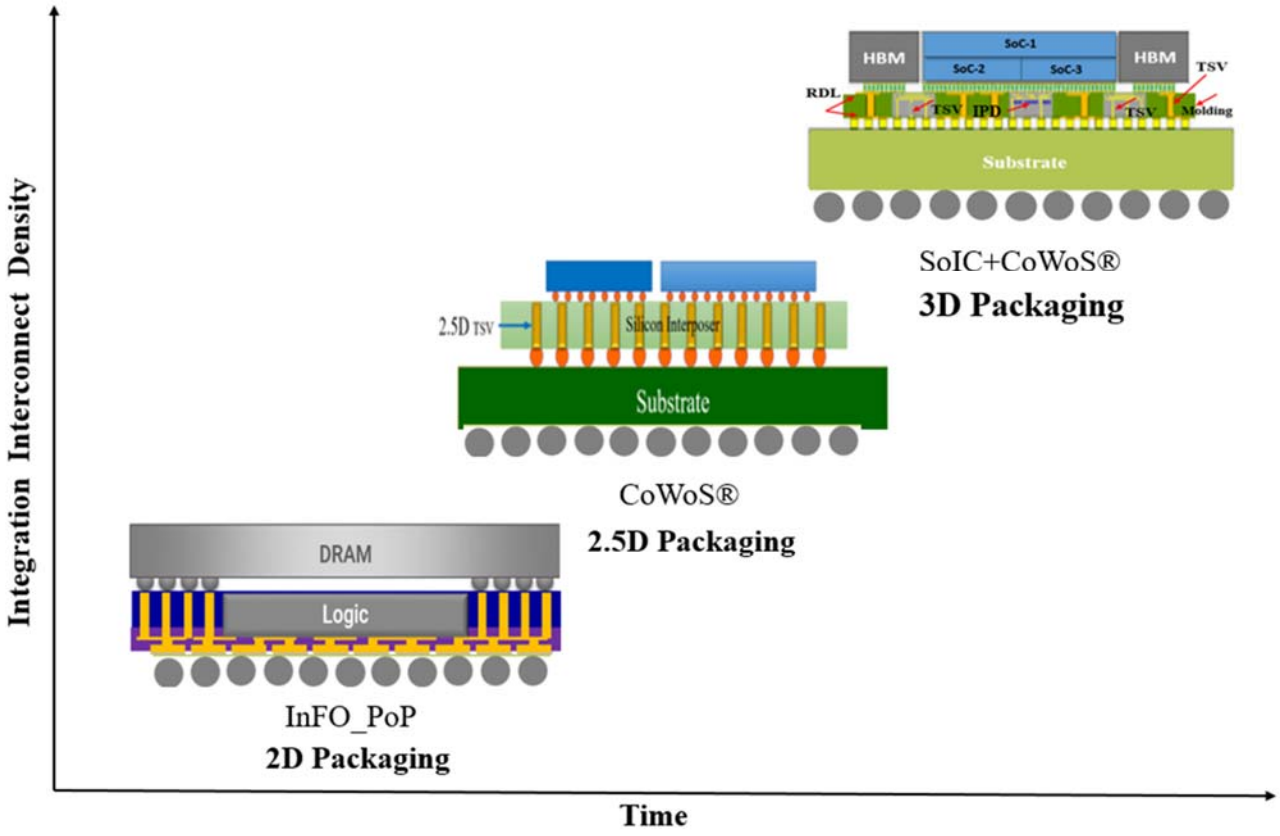


Fig. 16 TSMC 3DFabric™ Integration [17]; improve system-level performance, power, form factor, and functionality

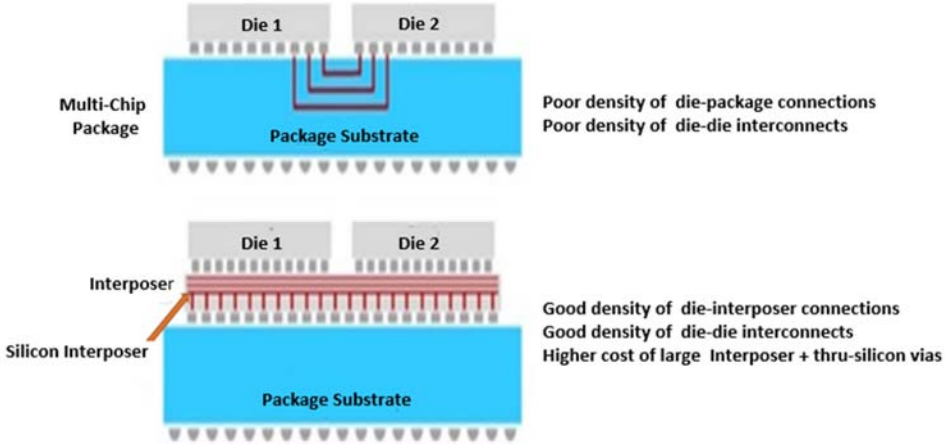


Fig. 17 Heterogeneous Integration Options (2D Multi-Chip and 2.5D CoWoS Packages) [17]

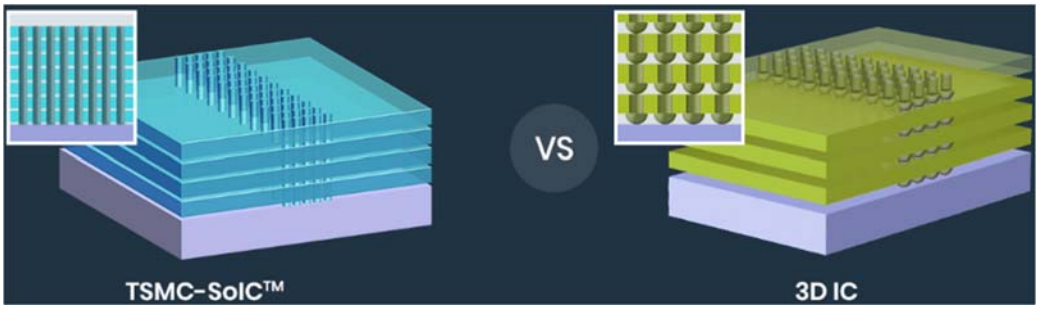


Fig. 18 Heterogeneous Integration Option (System on Integrated Chips (SoIC™) versus 3D Multi-Chip Integration) [17]

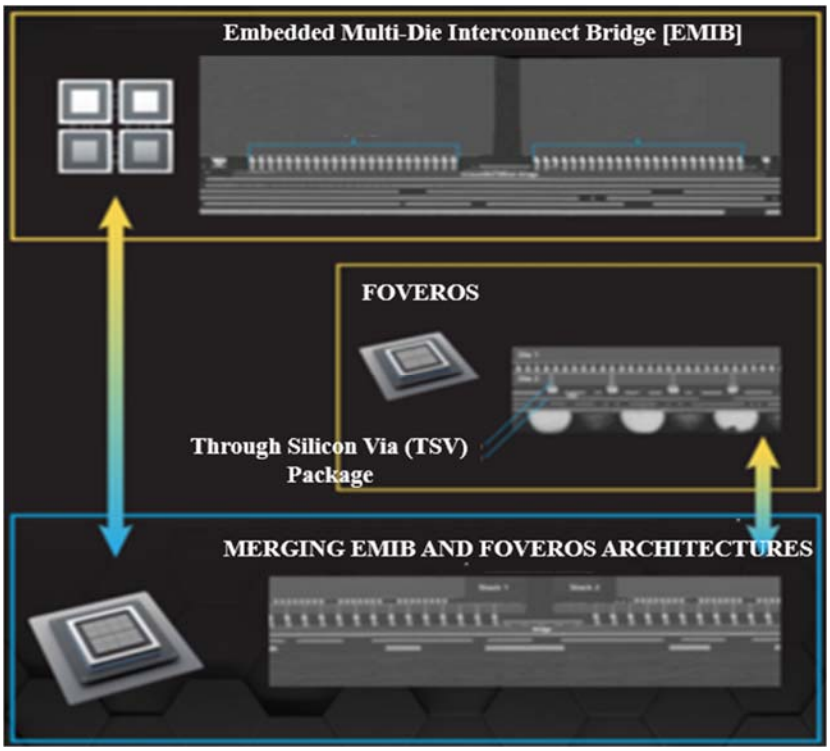
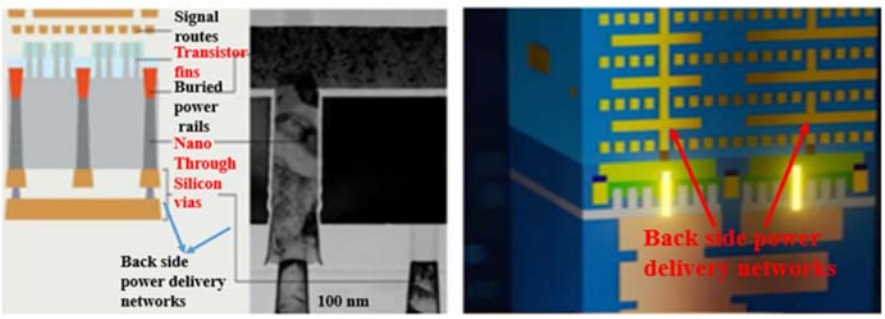


Fig. 19 Merging EMIB and Foveros Architecture [19], [37], [38]



(a) (b)

Fig. 20 (a) Fervos Profile [21]; (b) Power VIA (Intel) [40]

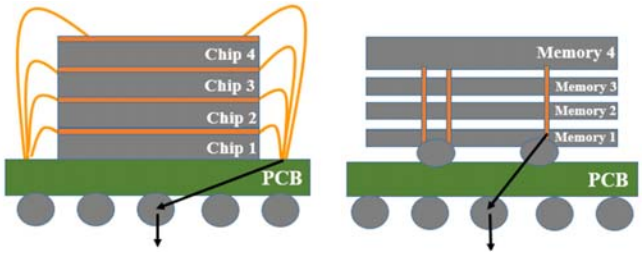
2. Intel's EMIB (2.5 D), Foveros (3D), and Power Via

The upper part of Fig. 19 demonstrates that Intel's EMIB's Silicon Interposer is significantly smaller than TSMC's CoWoS. It has the advantage of low cost. Foveros (the middle part) enables the foundry to integrate processors with computing units piled vertically, providing more excellent performance in a miniaturized package. It helps the manufacturer optimize the cost and power efficiency and allows the fine interconnect pitch. In addition, the chip's back Power Via can implement the backside power delivery and optimize

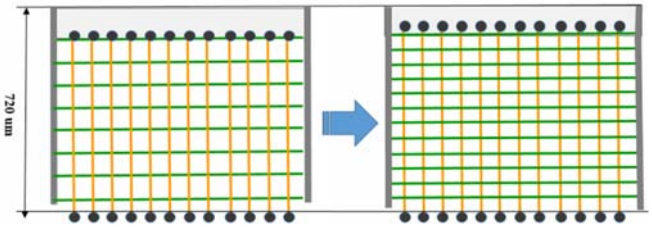
signal transmission by eliminating the requirement for power routing on the front side of the wafer (Fig. 20) [40].

3. Samsung's 12-Layer 3D TSV for High Bandwidth Memory (HBM)

Fig. 21 shows Samsung's 12-layer 24 GB HBM chips that use 3D TSV technology to increase the stacking from 8 to 12 layers. Because the 3D structure through 60,000 TSV holes is vertically interconnected, high-precision alignment is required [39]. Academic circles see this technology as one of the most challenging packaging technologies for mass-producing high-performance chips. Compared with current wire bonding technology, it can shorten the data transfer time between chips, reduce power consumption and increase speed.



(a) Conventional Wire Bonding vs. TSV Technology



(b) 8-layer vs. 12-layer cross section structure

Fig. 21 12-Layer 3D TSV technology [39]

III. Conclusions

This article comprehensively overviews the various multi-chip alternatives for 2.5D and 3D IC packaging technologies. It highlights the growing demand for higher performance and increased functionality in electronic devices, which has led to the development of advanced packaging solutions beyond traditional 2D IC packaging. It extensively surveys the multi-chip alternatives used in 2.5D and 3D IC packaging, including silicon interposer-based approaches, such as EMIB, FOWLP, FOPLP, InFO, CoWos, SOIC, SiWLP, and eWFO to assemble the chips and formulate new architectures, and describes each alternative in detail. Furthermore, we describe emerging trends and future directions in multi-chip packaging, like FOWLP, and advanced packaging technologies for artificial intelligence (AI) and 5G applications.

The information presented in this article is a valuable resource for researchers, engineers, and designers working in IC packaging, aiding them to make informed decisions when selecting the most suitable multi-chip alternative for their specific applications.

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