An Investigation into the Isolation and Bandwidth Characteristics of X-Band Chireix PA Combiners

D. P. Clayton, E. A. Ball

***Abstract*—**This paper describes an investigation into the isolation characteristics and bandwidth performance of radio frequency (RF) combiners that are used as part of Chireix power amplifier (PA) architectures, designed for use in the X-Band range of frequencies. Combiner designs investigated are the typical Chireix and Wilkinson configurations which also include simulation of the Wilkinson using manufacturer's data for the isolation resistor. Another simulation was the less common approach of using a Branchline coupler to form the combiner, as well as simulation results from adding an additional stage. This paper presents the findings of this investigation and compares the bandwidth performance and isolation characteristics to determine suitability.

***Keywords*—**Bandwidth, Chireix, couplers, outphasing, power amplifiers, Wilkinson, X-Band.

I. Introduction

THE Chireix, or outphasing, amplifier was designed with the aim of improving efficiency of the valve amplifiers used in AM kilowatt transmitters. This technique has had somewhat of a resurgence in modern times as an efficiency enhancement method for use at much higher application frequencies than its originally intended design frequencies. Modern communication systems demand for faster data rates and more bandwidth, have placed an even greater emphasis on amplifier designs to be as efficient as possible and this has allowed for older architectures like the Chireix method, first proposed by H. Chireix back in 1935 [1], to be repurposedsed. Fig. 1 shows a simplified block diagram of a Chireix system comprising a signal component separator (SCS), the two PAs and the combiner.

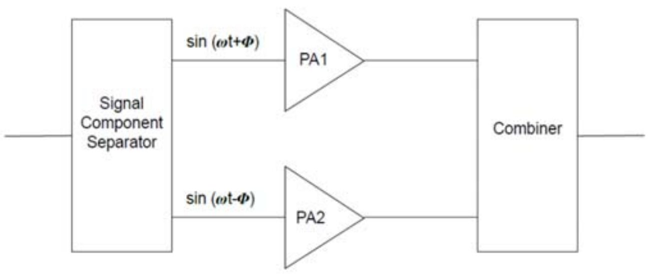

Fig. 1 Block Diagram of a Chireix System

The operation of the Chireix system starts with the generation of two constant amplitude signals that are identical except for the case that one of the signals is out of phase with the other so the amplitude modulated signal information is encoded via the difference in phase. These two signals are then fed into a separate amplifier stage each and both PAs are then operating at a fixed power level and so are themselves highly non-linear.

The combiner often becomes the focus for research due to it having an impact on parameters such as bandwidth, linearity and efficiency and so designs are often based around improving one or more of these parameters in some way. This paper details an investigation into the bandwidth performance and isolation characteristics of a Wilkinson combiner compared with a Chireix combiner, followed by an idea of using a Branchline coupler as a combiner, all designed for use in the X-Band range of frequencies of 8 GHz to 12 GHz.

The paper is organized as follows: Section II details the typical combiner configurations that are commonly used. Section III discusses the layout and the simulation results of a Wilkinson combiner; Section IV presents the design details and simulation results of a Branchline coupler followed by the addition of a second stage to the coupler to show the effect on bandwidth along with the simulation results of this. Lastly, Section V provides the conclusion to the paper.

II. Typical Combiner Configurations

An approach, documented in a number of research papers, to the combiner stage of the Chireix architecture is to typically use either a non-isolated design [2], as originally proposed by H. Chireix, or an isolated design using a common layout such as a Wilkinson combiner [3]. Fig. 2 shows the Chireix combiner while Fig. 3 shows the Wilkinson combiner layout.

The non-isolated method is to use quarter-wavelength transmission lines and then apply lumped reactive compensating components at the inputs to remove the imaginary part of the phase varying impedance at specific outphasing angles and so improve efficiency [4]. For higher frequency designs these lumped components can be transformed into open and short circuit stubs and this method was used in [5], however, it was found that the compensating stubs negatively impacted the linearity of the design and so required the application of linearization techniques, which highlights that there are drawbacks to this method.

The Wilkinson combiner is effective for maintaining a good isolation between the two input ports and this means that the two input PAs cannot interact via the combiner circuit, hence

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the term isolated, so the overall individual PA behavior can be more accurately controlled. The drawback to this layout is that the resistor that is vital to the isolation is also a source of loss in the system and so harms the overall efficiency although there is interesting research on recovering this energy, normally lost by the resistor as heat, and feeding it back to the supply as shown in [6]. At high frequencies there is also the potential issue of the resistor component parasitic that could be detrimental to correct circuit operation, making the implementation of this resistor into higher frequency designs potentially more problematic. Despite this issue of size for high frequency implementation, it was decided that the Wilkinson would be a better choice for further investigation due to the linearity drawbacks of the Chireix combiner mentioned in [5].

III. Simulation of an X-Band Wilkinson Combiner

The Wilkinson combiner was designed for an operating frequency of 9 GHz using quarter-wavelength microstrip transmission lines utilizing the Keysight Advanced Design System (ADS) software package. The characteristic impedance for the circuit was taken as 50 Ω and so the quarter wavelength line impedances and isolation resistor values were calculated using equations found in [7].

The substrate used was a Rogers Corporation RO4003C, with a dielectric permittivity (εr) of 3.55, a substrate thickness of 0.5 mm, a copper conductor thickness of 17 µm and a dissipation factor (tan δ) of 0.0027. Fig. 4 shows the circuit, including the substrate information that was used when calculating the dimensions of the transmission lines, as well as the results of the S-Parameter simulation.

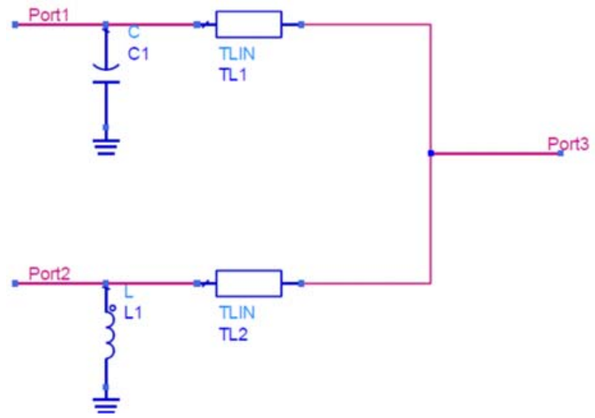

Fig. 2 Chireix Combiner with Compensating Components

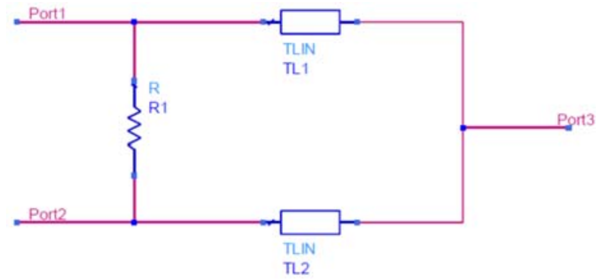

Fig. 3 Wilkinson Combiner with Isolation Resistor

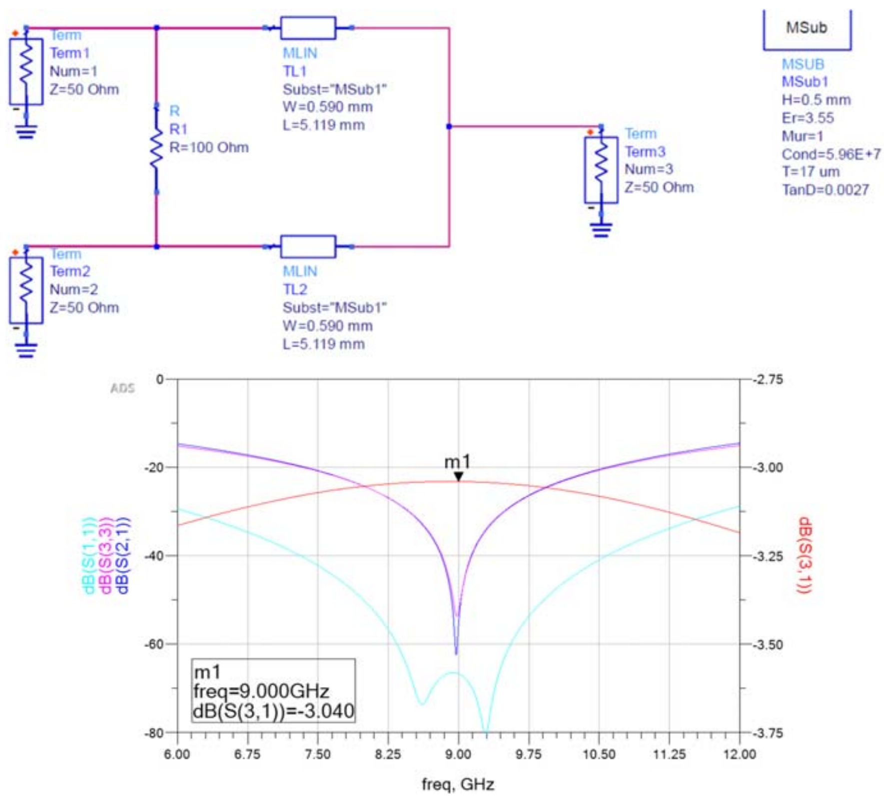

Fig. 4 Wilkinson Combiner Layout and S-Parameter Simulation Results

The S-Parameter simulation shows the 3 dB power split at the design frequency and a good isolation figure (S(2,1)) between the two inputs of greater than 40 dB. Cripps noted in [8] that removal of this isolation resistor causes dramatic changes in circuit behavior. Because of this, the next simulation involved removing this isolation resistor in order to determine what effect this had on the overall performance of the circuit and another S-Parameter simulation was conducted. Fig. 5 shows the results of this simulation and it can be seen that the isolation between the two input ports is negatively impacted and therefore shows the isolation resistor is vital to the correct operation of the Wilkinson combiner.

Another simulation of the Wilkinson combiner was then considered but instead of using the idealized resistor used within the ADS software, the resistor was modeled on a Vishay FC Series 0402 chip resistor with its lumped internal capacitance and inductance, taken from the datasheet. The reason for this was to try and recreate a circuit with resultant simulation data that would show as close as possible what the physical combiner would give if manufactured. This resulted in the same 100 Ω resistor being used but also required a 0.00189 nH inductor in series and a 0.0262 pf capacitor placed in parallel as shown in the circuit layout, Fig. 6, with the respective simulation data presented in Fig. 7.

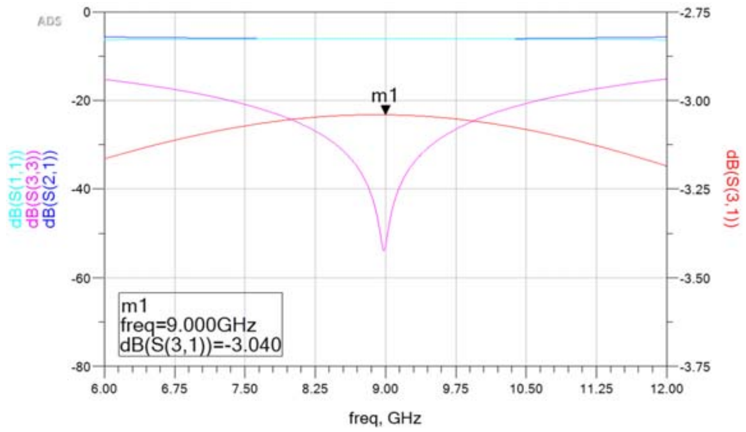

Fig. 5 S-Parameter Simulation of Wilkinson Combiner with Isolating Resistor Removed

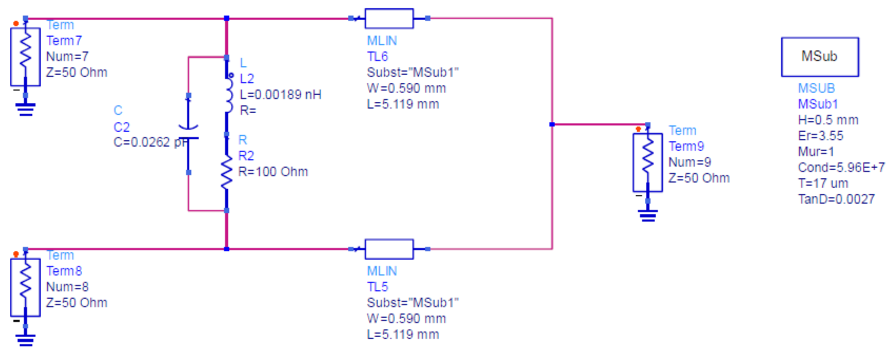

Fig. 6 Wilkinson with Lumped Internal Components of Resistor

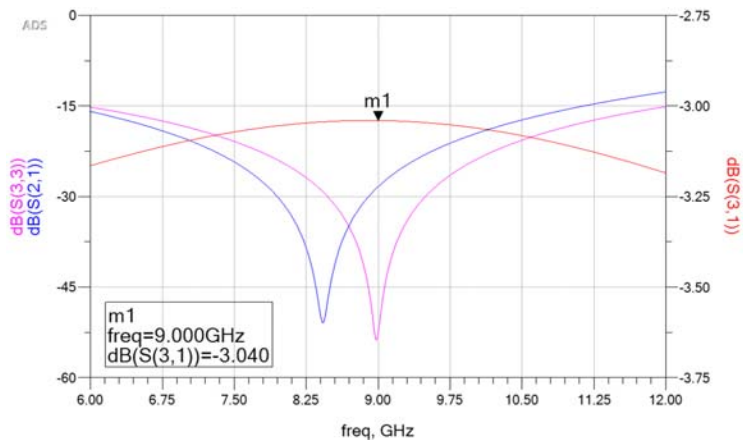

Fig. 7 Simulation Results of the Wilkinson with Lumped Internal Components of Resistor

As can be seen from the simulation data, the isolation figure, S(2,1), is no longer tuned to exactly 9 GHz due to the effect of the capacitive and inductive elements of the resistor but it is still low enough at 9 GHz, at almost -50 dB, to still be considered a good figure of merit.

IV. Simulation of an X-Band Branchline Coupler

An interesting concept is the use of a coupler to form the combiner stage as shown in [9], [10] in order to determine if there is an overall improvement in bandwidth of the system compared against other combiner configurations. Because a coupler also manipulates the phase of the input signals passing through it, any potential Chireix combiner that would utilize the Branchline coupler design would have to consider that one of the input signals to the coupler would already be out of phase.

A single stage Branchline coupler, designed around a center frequency of 9 GHz, is shown in Fig. 8, using Port 1 and Port 2 as the two input ports, with Port 3 as the output port and with Port 4 as the isolated port. As with the Wilkinson design, the transmission lines are all a quarter-wavelength long at the design frequency with the series line impedances set to 50 Ω and the Branchline impedances calculated to be 35.4 Ω using equations taken from [7]. The substrate parameters were identical to those in the simulation of the Wilkinson combiner as detailed in the previous section.

An S-Parameter simulation of the circuit detailed in Fig. 9 was performed, showing an approximate 3 dB power split, the same as the Wilkinson design, as well as markers to determine the 1 dB bandwidth of the coupler, in this case showing a bandwidth of 2300 MHz.

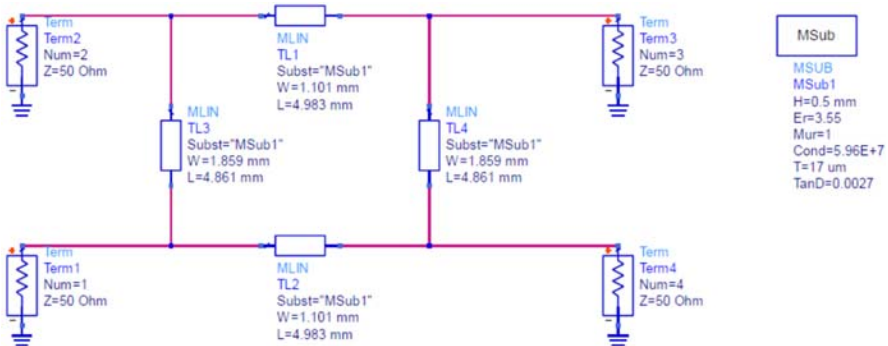

Fig. 8 X-Band Branchline Coupler Layout

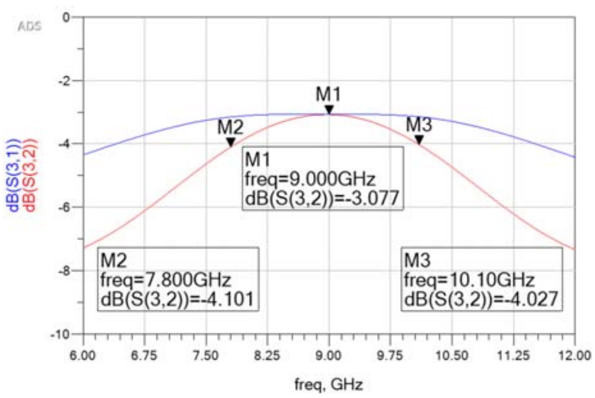

Fig. 9 Bandwidth Simulation Results of the X-Band Branchline Coupler

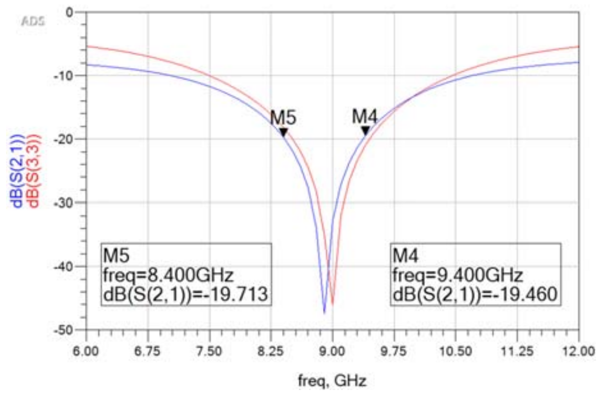

Fig. 10 Isolation Measurements of Branchline Coupler

The isolation characteristics of the Branchline were then measured, as shown in Fig. 10, in order to compare this against the Wilkinson combiner with the idealized resistor of Section III.

Much like the Wilkinson combiner, the Branchline coupler shows a very good level of isolation bandwidth of 1 GHz at a level of approximately -20 dB for the S(2,1) parameter.

The next process of the investigation was to incorporate an additional stage to the coupler circuit in order to determine how much improvement on bandwidth this enables. To do this, two identical circuits were combined together and the tune feature of ADS was used to determine the ideal impedance values for each line. For simplicity's sake, the series impedances were kept at 50 Ω to provide a better match at the inputs and outputs, the outermost branch lines were tuned to 110 Ω and the central line tuned to 65 Ω, all shown in Fig. 11.

An increase in overall bandwidth was achieved with the two-stage coupler, as identified in Fig. 12, showing an approximate bandwidth of 3300 MHz compared with the single stage coupler bandwidth of 2300 MHz giving an overall bandwidth increase of 1 GHz.

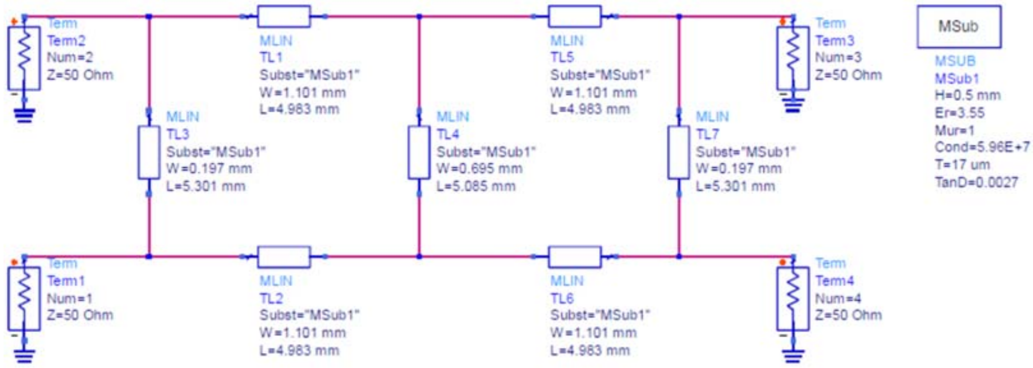

Fig. 11 Layout of Branchline Coupler with Additional 2nd Stage

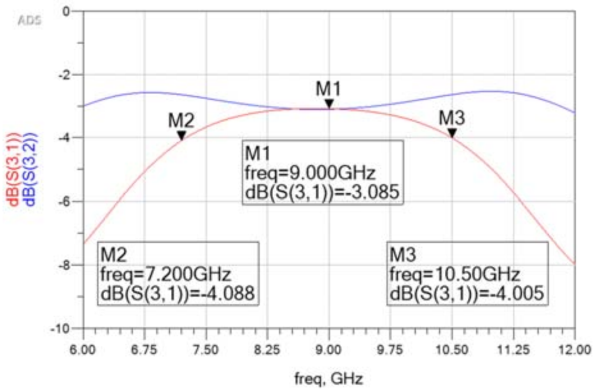

Fig. 12 Bandwidth Simulation Results of the X-Band 2 Stage Branchline Coupler

As with the single stage Branchline coupler, isolation measurements were made for the two-stage design to determine what impact the additional stage could have. Again, the isolation figure is good at approximately -38 dB, although it is not as good as the single stage design, it is well above the accepted level for this type of parameter. The simulation results for this are given in Fig. 13.

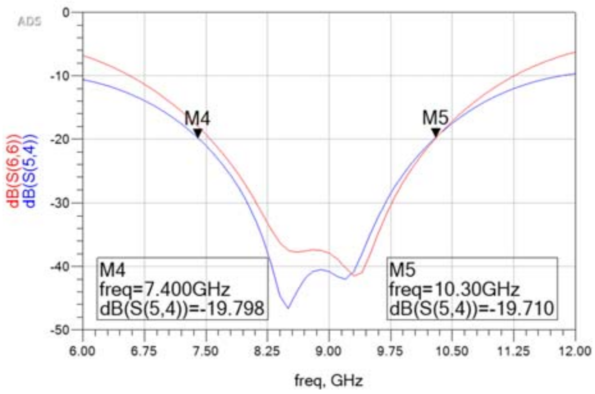

Fig. 13 Isolation Measurements of the 2 Stage Branchline Coupler

V. CONCLUSION

The investigation shows that while a Wilkinson combiner is a straightforward design, the resistor is fundamental to its correct operation and to provide the high level of isolation. For higher frequencies this resistor would be more difficult to implement due to capacitive and inductive parasitic and so the isolation would be negatively impacted. The Branchline coupler used as a combiner shows promise due to providing good insertion loss and isolation bandwidth figures without requiring a passive component and that also by merely adding an additional stage, increases these parameters without much complexity. The only downside to the addition of further stages would be the increased circuit size.

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