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Comparative Study of Al_2O_3 and HfO_2 as Gate Dielectric on AlGaN/GaN MOSHEMTs

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***Abstract*—**We have made a comparative study on the influence of Al_2O_3 and HfO_2 grown using Atomic Layer Deposition (ALD) technique as dielectric in the AlGaN/GaN metal oxide semiconductor high-electron mobility transistor (MOS-HEMT) structure. Five samples consisting of 20 nm and 10 nm each of A_2lO_3 and HfO_2 respectively and a Schottky gate HEMT, were fabricated and measured. The threshold voltage shifts towards negative by 0.1 V and 1.8 V for 10 nm thick HfO_2 and 10 nm thick Al_2O_3 gate dielectric layers, respectively. The negative shift for the 20 nm HfO_2 and 20 nm Al_2O_3 were 1.2 V and 4.9 V, respectively. Higher g_m/I_{DS} (transconductance to drain current) ratio was also obtained in HfO_2 than Al_2O_3. With both materials as dielectric, a significant reduction in the gate leakage current in the order of 10^4 was obtained compared to the sample without the dielectric material.

***Keywords*—**AlGaN/GaN HEMTs, Al_2O_3, HfO_2, MOSHEMTs.

I. INTRODUCTION

OWING to their material properties of wider bandgap (> 3eV), high critical electric filed (> 3 MV/cm), high electron velocity (> 2.5 x 10^7 cm/s) and a reasonably high thermal conductivity (130 W/cm), gallium nitride (GaN) is believed to be the potential replacement of silicon in future power electronic applications. In AlGaN/GaN heterojunction, a high concentration (> 10^{13} cm^{-3}) of high electron mobility (up to 2000 cm^2/s) 2-dimentional electrons gas (2DEG) can be achieved without any intentional doping. The 2DEG makes the basis of high electron mobility transistors (HEMTs), which have gained a commercial acceptance and are widely used in the optoelectronic applications such as light emitting diodes, photodetectors, and in the radio frequency (RF) and power technologies. Despite these tremendous achievements, two fundamental challenges still persist; current collapse which limits the power output, and (Schottky) gate leakage, which limit the on-state voltage swing, have been of greater concern in pushing their application spaces in high power RF and high temperature applications. The current collapse phenomenon is the decrease in the drain current when large alternating signal is applied to the gate [1]-[3]. The lag of threshold voltage is the other fundamental issue affecting the performance of GaN HEMTs. Presence of surface traps in the hetero-epitaxially grown HEMT devices, are believed to be the main cause of these problems. To address these issues, dielectric materials such as SiO_2 [4]-[6], Si_3N_4 [6]-[8], Al_2O_3 [8]-[11], Hf_2O [12]-[14] etc., are widely used for passivation and gate insulation in AlGaN/GaN MOS-HEMTs. Significant progresses have been achieved in minimizing Schottky gate leakage and current collapse through this technique. However, using these high permittivity materials sometimes compromises the threshold voltage shifts and the device's transconductance, which are very much desirable in high power RF and high temperature applications. With many reported works in literature [5]-[11], [15]-[18] on the performance of various dielectric materials, it is obvious that making comparative study requires consideration of many factors such as material quality, thickness of the insulator, device processing technique, surface treatment, dielectric deposition technique, and the type of the dielectric material itself.

In this work, we compared the influence of the Al_2O_3 and HfO_2 of different thicknesses as insulating oxides deposited using ALD on AlGaN/GaN MOS-HEMT.

II. DEVICE STRUCTURE AND FABRICATION

In this study, an experiment was carried out using five different AlGaN/GaN HEMT samples to make a comparative investigation on the performance of the device using different thicknesses of Al_2O_3 and HfO_2 as insulation oxides in the metal semiconductor structure. The epitaxial layers were grown using metal organic chemical vapor deposition (MOCVD) by the University of Cambridge, United Kingdom, and consisted of 2 nm undoped GaN cap layer, 21 nm AlGaN barrier layer, 1 nm AlN exclusion layer, 200 nm GaN channel layer, 800 nm GaN buffer layer, 1.7 μm graded AlGaN buffer layer and 250 nm nucleation layer, on 4-inch silicon wafer. The device structure is illustrated in Fig. 1. A two-level gate wrap-around transistor design with gate length, L_G = 3 μm, gate-to source spacing, L_{GS} = 3 μm, and gate-to-drain spacing, L_{GD} = 5 μm was used to minimize the device processing time and steps, eliminating the need for mesa isolation as shown in Fig. 2. The five samples were designated S1 to S5 as follows: S1- a Schottky gate HEMT without dielectric, S2- MOS-HEMT with 10 nm thick Al_2O_3, S3- MOS-HEMT with 10 nm HfO_2, S4-MOS-HEMT using 20 nm thick Al_2O_3, and S5- MOS-HEMT with 20 nm thick HfO_2.

Device fabrication begun with depositing a metal stack of Ohmic contacts by the evaporation of Ti/Al/Ni/Au (30/180/40/100 nm), then annealing in the N_2 atmosphere at 800 °C for 30 secs using rapid thermal annealing (RTA) technique. This was followed by a blanket deposition of 10 nm of Al_2O_3 for S2, 10 nm of HfO_2 for S3, 20 nm of Al_2O_3 for S4, and 20 nm of HfO_2 for S5 using ALD. The Schottky gate contact was metallized by the evaporation of Ni/Au (20/400 nm), followed by a lift-off

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process. Dielectric layers (Al_2O_3 and HfO_2) were removed from Ohmic regions for measurement purposes. Al_2O_3 was removed from the ohmic regions of S2 and S4 using inductively coupled plasma (ICP) 180. The recipe was: BCl_3, ICP = 600 W, and RF = 25 W for 60 secs for S2 and 90 secs for S4. HfO_2 was removed from the Ohmic regions of S3 and S5 using PlasmaPro System 100 ICP 300 Cobra. The recipe was: ICP = 1250 W, RF = 25 W, 3 mTorr, 10 sccm BCl3, 10 sccm Cl2, 20 oC, He = 10 Torr for 40 secs for sample S3 and 60 secs for S5.

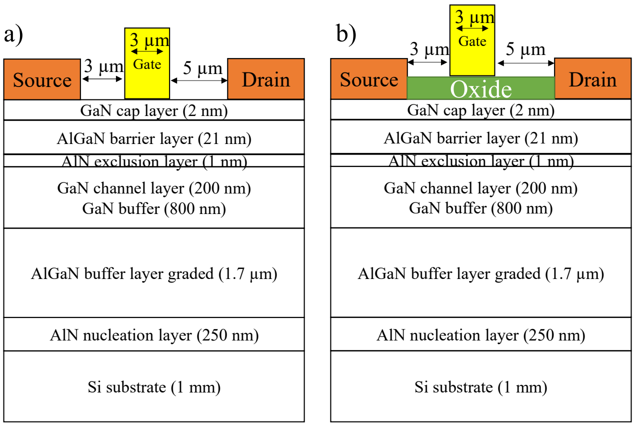

Fig. 1 Cross-section schematic diagram of fabricated devices: (a) AlGaN/GaN HEMT structure, (b) AlGaN/GaN MOSHEMT structure employing Al_2O_3/HfO_2 as gate dielectric

Fig. 2 Top-view fabricated layout of a wrap-around gate device

III. RESULTS AND DISCUSSIONS

The DC characteristics of the gate wraparound transistor samples were measured using Keysight B1500A Semiconductor Device Analyzer. The transfer characteristics of the five samples were measured by sweeping the gate voltage from -10 V to +1 V at the step of 1 V and the drain voltages from 0 V to +10 V. The measured output, transfer, and gate leakage current characteristics of the fabricated devices are shown in Figs. 3, 4, and 5, respectively. For ease of comparison, various transistor parameters are deduced from the measurements and given in Tables I and II. As can be seen in Table I, there is significant decrease in the gate leakage current in samples S2 to S5 in comparison with S1. Moreover, with different thicknesses of the dielectric in the MOSHEMT structures S2 to S5, the leakage current remains the same regardless of the insulation material, likewise much higher drain currents were obtained in samples S2 to S5 compared to S1. Drain current is observed to be increasing with the increasing dielectric thicknesses in all samples as obtained in Table I. This could be attributed to the influence of the dielectric on the AlGaN surface enhancing the density of the 2DEG. It had been reported in literature that surface states have a significant effect in the sheet carrier density of the 2DEG and applying a dielectric layer on the AlGaN barrier layer, reduces the effect by eliminating the negative carrier charges [19]-[21]. However, some literatures suggested that increase in the 2DEG density is due to the strain effect of dielectric on the AlGaN barrier layer, which causes an increase in the piezoelectric polarization field between the atoms [22]. The higher drain currents obtained in the Al_2O_3 than HfO_2, may be related to the relative influence of HfO_2 on the channel carrier mobility [23], [24]. This study also employs g_m/I_{DS} principle, which is the measure of the efficiency of a device, to further compare the device's performances. The greater the g_m/I_{DS} value, the greater the transconductance obtained at a constant current [25]. The variation in the g_m/I_{DS} ratio with the thickness of gate dielectric can be observed in both materials. The results in Table II illustrate that lower ratio of g_m/I_{DS} was obtained in samples with thicker dielectric. Moreover, samples with HfO_2 have higher g_m/I_{DS} ratio than samples with Al_2O_3 dielectrics. This could be due to the increasing drain current in the samples with thicker dielectric layer, and the increase in the current is more in the Al_2O_3 dielectric, making the samples with HfO_2 be more efficient. Changes in the threshold voltages were also observed in respect with the differences in the thickness and the type of dielectric material used. Each value of the threshold voltage was extracted at I_{DS} = 1 mA/mm. In Table I, the threshold voltage shifts towards negative, with increasing thickness, and the increase is more in Al_2O_3 compared to HfO_2 materials. In theory, threshold voltage is in inverse proportion to the gate capacitance. Increasing thickness of the dielectric eventually results in decreasing gate capacitance, while using material with higher permittivity results in higher gate capacitance. Moreover, higher thresholds in the Al_2O_3 layer are due to its lower permittivity compared to HfO_2.

CV measurements were carried out for all the samples to analyze the quality of the dielectric layers. Double sweep CV measurement at 1 MHz frequency is used to see the hysteresis of the dielectric layers. It was swept from -10 to 0 V in forward measurement, and then swept backward to initial negative voltage (-10) to complete hysteresis curve as shown in Fig. 6. The hysteresis curve shows a good result for all samples. The hysteresis occurs due to the existence of interface traps between the GaN surface and the dielectric layers. Also, change in hysteresis (Δhysteresis) was obtained by measuring flat band voltages between the forward and backward C-V sweeps. Δhysteresises were 5 mV, 20 mV, 16 mV, 13 mV, and 32 mV for S1, S2, S3, S4 and S5, respectively, as shown in Table II.

TABLE I
DEVICE CHARACTERIZATIONS OF DIFFERENT DIELECTRICS (AL_2O_3 AND HFO_2) WITH 10 NM AND 20 NM THICKNESS

	Drain Current at V_{GS} = 1V (mA/mm)	Transconductance (mS/mm)	Gate Leakage Current (A/mm)	Threshold Voltage (V)
HEMT	980	225	~1E-4	-4.3
10 nm HfO_2	1300	276	~1E-8	-4.4
10 nm Al_2O_3	1443	292	~1E-8	-6.1
20 nm HfO_2	1561	287	~1E-8	-5.6
20 nm Al_2O_3	1910	274	~1E-8	-9.2

HEMT is used for comparison to MOSHEMTs.

TABLE II
OBTAINED PARAMETERS OF MEASURED DEVICES S1, S2, S3, S4, AND S5

	g_m/I_{DS} (S/A)	$\frac{I_{Dielectric}}{I_{HEMT}}$	Δhysteresis (mV)
HEMT	0.231	N/A	5
10 nm HfO_2	0.212	1.327	20
10 nm Al_2O_3	0.202	1.472	16
20 nm HfO_2	0.184	1.593	13
20 nm Al_2O_3	0.143	1.949	32

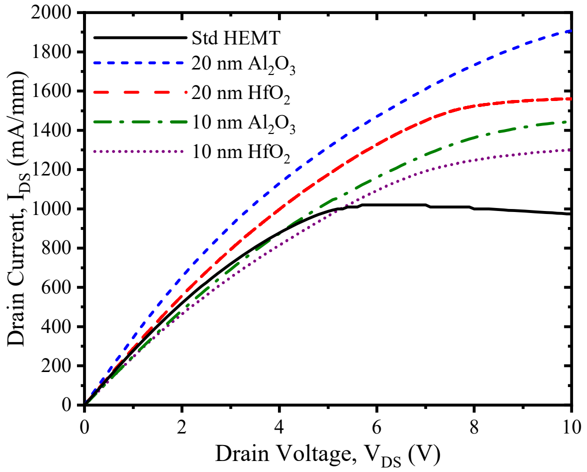

Fig. 3 Measured output characteristics at gate-to-source voltage, V_G = 1 V, for all fabricated devices

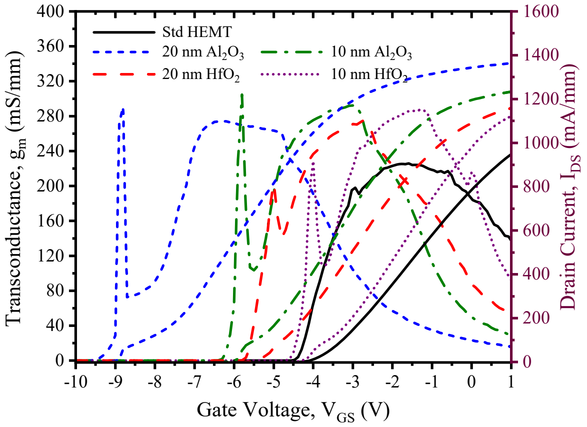

Fig. 4 Measured transfer characteristics at a drain-to-source voltage, V_{DS} = 5 V, for all fabricated devices

IV. CONCLUSIONS

In this study, the influence of HfO_2 and Al_2O_3 as gate dielectrics in MOSHEMTs have been experimentally investigated and compared. Based on the experimental results, a significant reduction in the leakage current has been recorded in the samples insulated with the high-k dielectrics (Al_2O_3 and HfO_2) than that without dielectric. Insulating the gate with HfO_2 has shown higher g_m/I_{DS} ratio than Al_2O_3. The drain current is found to be higher with increasing thickness of the dielectric layer, and much higher in Al_2O_3 than in HfO_2. The threshold voltage shifts towards negative with increasing layer thickness and much more in Al_2O_3 than HfO_2 of the same thickness. The results indicate that HfO_2 could be the dielectric of choice for high frequency applications.

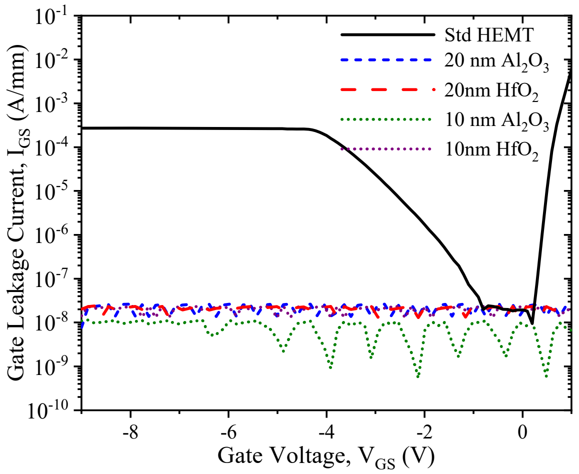

Fig. 5 Measured gate leakage current characteristics at drain-to-source voltage, V_{DS} = 0 V for all fabricated devices

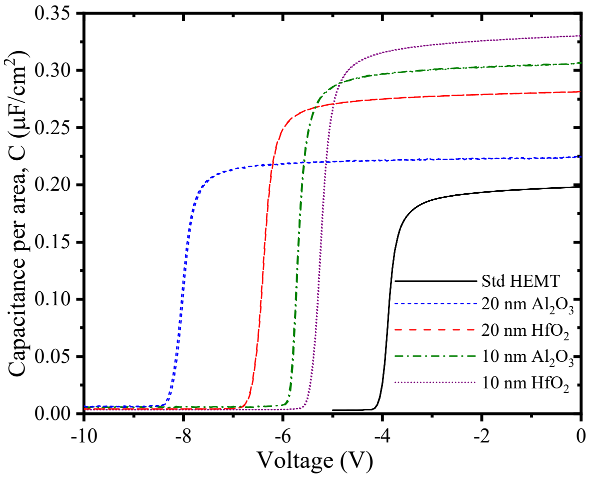

Fig. 6 Double sweep CV measurements for fabricated devices at 1 MHz frequency

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