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Void-Free Bonding of Si/Ti/Ni Power Integrated Circuit Chips with Direct Bonding Copper Alumina Substrates through Ag_3Sn Intermetallic Interlayer

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***Abstract*—**Ti/Ni/Ag/Sn-metallized Si chips were bonded to Ni/Pd/Au-surface finished DBC (Direct Bonding Copper) alumina substrate through the formation of an Ag_3Sn intermetallic interlayer by solid–liquid interdiffusion bonding method. The results indicated that the holes and gaps at the bonding interface could be effectively prevented. The intermetallic phases at the bonding interface between the Si/Ti/Ni/Ag/Sn wafer and the DBC substrate were identified as Ag_3Sn, Ni_3Sn_4, and Ni_3Sn_2. The average bonding strength was about 19.75 MPa, and the maximum bonding strength reached 35.24 MPa.

***Keywords*—**BGBM, Backside Grinding and Backside Metallization, SLID bonding, Solid–liquid Interdiffusion Bonding, Si/Ti/Ni/Sn, Si/Ti/Ni/Ag/Sn, intermetallic compound.

I. Introduction

THE power module is a power semiconductor component, such as a MOSFET (Metal-Oxide-Semiconductor Field-Effect Transistor), IGBT (Insulated Gate Bipolar Transistors), BJT (Bipolar Transistor), Thyristor (Silicon Controlled Rectifier, SCR), GTO (Gate Turn-Off thyristor), JET (Junction Gate Field-Effect Transistor) or a module with diodes in the same package. By welding or sintering, power semiconductors are fixed on substrates such as DBC substrates, which provide thermal conduction, electrical conduction, and signal transmission. Most power modules include multiple interconnected dies to form specific circuits; in electric vehicle applications, the efficiency of power components and modules directly affects the vehicle's performance, such as driving distance. Therefore, improving the efficiency while reducing the volume and weight of electric vehicle powertrains will potentially save a lot of energy [1], [2].

At present, the technical development trend of power modules is to reduce the cost, increase the power density, improve the reliability and reduce the impacts of stray components. Among them, a common topic of power module optimization is the path from the heat source (bare die) to the heat sink. Since the new generation of power transistors requires better heat transfer with a greater power density, the negative impact of elevated temperatures on the performance and reliability of semiconductor dies is well understood and documented [3]-[5]. The thermal management challenges caused by the adoption of high-power modules should be addressed in future power module packaging. Solid–liquid interdiffusion (SLID) bonding is a bonding packaging technology applied in the fields of semiconductors and power components because it provides features such as good bonding strength, low thermal resistance at the bonding interface, and high-temperature resistance of the bonding point.

The use of advanced processes and materials at the interface of the package layer between the chip and the DBC substrate will help to reduce the thermal resistance of the package. For example, the wafer may be a BGBM (Backside Grinding & Backside Metallization) process wafer. The processing method is first to grind the backside of the wafer to make the surface of the back side flat to achieve a specific surface roughness and wafer thickness, and then to apply the metallization layer. This is a reliable method for high-temperature semiconductor component die bonding due to its advantages of a thin wafer attachment layer, excellent ohmic contact, good heat dissipation, and electrical conductivity [6], [7]. Backside Metallization (BSM) wafers are particularly suitable for SLID bonding processes. Typically, a BSM layer consists of several thin metal films adhered in layers, such as diffusion barriers, solder layers, and protective oxide layers [6], [7].

Die bonding is one of the main steps in power integrated circuit (IC) packaging. To meet the needs of high-temperature applications, special attention should be paid to the temperature resistance, bonding strength, reliability, electrical conductivity, and thermal resistance after bonding of the chip and substrates. The current conventional method is to use soldering and Ag sintering. However, the application of soldering to products is often limited by the low melting point of solder, which is not suitable for high-power components used in high temperature applications. The other is Ag sintering technology, which offers many advantages, such as high thermal conductivity and enhanced reliability of thermal and power cycling [8], [9]. The high melting point (961 °C) of the interface after sintering is suitable for components and products used in high-temperature applications, but because the bonding temperature is higher and the voids exceed 10% of the volume, the conductivity and reliability can easily be affected.

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Therefore, SLID bonding technology, which can be applied to low-temperature bonding and high-temperature applications, has attracted attention. According to the principle of phase equilibrium, a substance with a low melting point can diffuse through the solid state of another substance with a low or high melting point reaction (solid interdiffusion reaction) or a solid–liquid diffusion reaction (SLID reaction) to form intermetallic compounds (IMCs) with high melting points. This phenomenon can be used in bonding to achieve "low-temperature bonding and high-temperature application" because the rate of solid–liquid diffusion reaction is much higher than that of solid-state diffusion reaction. It can better meet the actual production needs of the industry and reduce the cost, and it has good bonding strength and bonding interface thermal resistance. The need for low-temperature bonding and high-temperature resistance at the bonding point drives the continuous development of packaging and bonding technologies in the field of semiconductors and power components. SLID uses at least two metals, a low melting point metal (solder) and a high melting point metal, which are capable of forming intermetallic phases. Additionally, the thickness of the solder must be in the micrometer range to cure in a reasonable bonding time, so SLID bonding is more suitable for flat and thinner electronic packages [10]. The IMCs mentioned above are alloy phases composed of different types of atoms in long-range ordered arrangement and have relatively certain stoichiometry ratios. They have a high melting point and high-temperature resistance, and the common and representative IMCs used in the field of bonding include Ag-Sn, Ni-Sn, and Cu-Sn systems. Ni/Sn/Ni and Cu/Sn/Cu are bonded using SLID technology. The NixSny and CuxSny IMCs thus formed are in a scallop form, which will lead to the generation of a large number of holes, so although they are widely used in 3D IC [11]-[14] and heat-resistant bonding in high-power module assemblies [15]-[17], they still entail some structural or process defects. In this study, two BSM wafers of Si/Ti/Ni/Sn and Si/Ti/Ni/Ag/Sn were respectively bonded on Au/Pd/Ni/Cu/Al_2O_3 DBC substrates by SLID technology. The bonding parameters were varied in the experiment. The diffusion phenomenon at the bonding interface was observed by SEM/EDX and the bonding strength was measured to evaluate the bonding performance. The BSM chip of Si/Ti/Ni/Ag/Sn was realized via void-free bonding of Si/Ti/Ni power IC wafers to DBC alumina substrates with an IMC layer of Ag_3Sn.

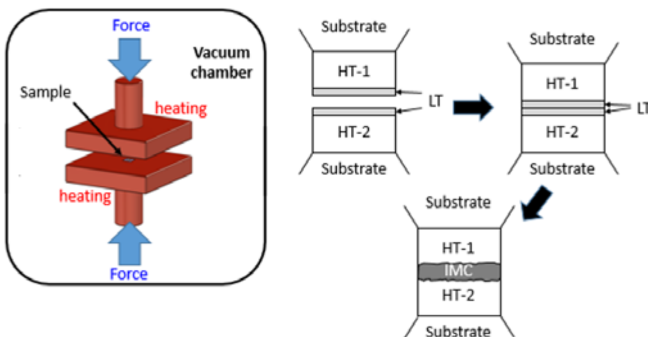

Fig. 1 Schematic diagram of the diffusion welding process

II. Experimental

In this study, the DBC was cut to a size of 3 mm x 3 mm, and the BSM wafers were cut to a size of around 6 mm x 6 mm. BSM wafers of two different structures, namely, Si/Ti/Ni/Sn and Si/Ti/Ni/Ag/Sn, were bonded on Au/Pd/Ni/Cu/Al_2O_3 DBC substrate under different bonding parameters. Tests with the different experimental parameters were performed in a vacuum environment. The bonding conditions were 250 °C for durations of 30 min, 60 min, 90 min, and 120 min. And the experiments' bonding temperatures were 275 °C, 300 °C, 350 °C, and 400 °C respectively for 30 min. Bonding was performed with pressure of 10 MPa on the bonded sample. Fig. 2 is a schematic diagram of diffusion soldering of the Si/Ti/Ni/Sn and Au/Pd/Ni/Cu/Al_2O_3 structure, and Fig. 3 presents a schematic diagram of diffusion soldering of the Si/Ti/Ni/Ag/Sn and Au/Pd/Ni/Cu/Al_2O_3 structure.

After the SLID bonding was completed, the samples were embedded in resin for sample preparation of the cross-section, and metallographic grinding and polishing were performed with sandpaper of different grits and 1.0 lm Al_2O_3 polishing powder. The morphology of the bonding interface and the formation of IMCs were then observed by scanning electron microscopy (SEM). The thickness of the IMC growth was measured from SEM images, and the growth kinetics of the IMCs s were further evaluated. Energy dispersive X-ray spectroscopy (EDX) was used to analyze the chemical composition of the intermetallic phase. To confirm successful bonding and to quantify the bond strength, bond samples were tested with a DAGE 4000 bond tester at a shear rate of 3×10^{-5}m/s.

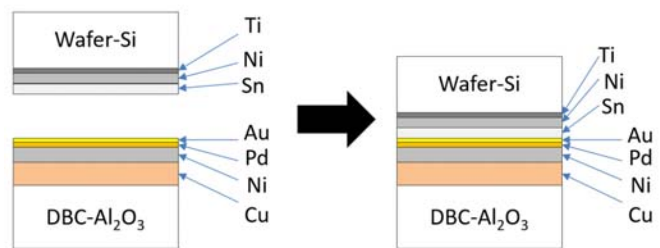

Fig. 2 Schematic diagram of diffusion soldering of Si/Ti/Ni/Sn and Au/Pd/Ni/Cu/Al_2O_3 with Sn interlayer

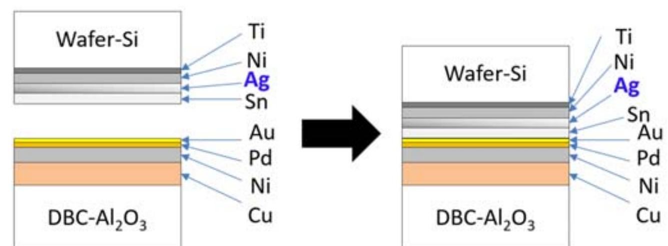

Fig. 3 Schematic diagram of diffusion soldering of Si/Ti/Ni/Ag/Sn and Au/Pd/Ni/Cu/Al_2O_3 with a Sn interlayer

III. Results and Discussion

Fig. 4 (a) shows the morphologies of the diffusion-bonded junctions of Ti/Ni/Sn back-gold structures under different bonding conditions. The bonding was performed at 250 °C for

30 minutes, and many gaps and voids were detected at the bonding interface. When the bonding time was increased to 60 minutes, 90 minutes, and 120 minutes, as shown in Fig. 4 (b)-(d), the gaps and voids increased, and as the bonding time increased, the intermediate layer of the IMC thickened. This thickening occurred because the Ni layer of the back metal layer at the bottom of the Si wafer diffused downward due to the solid solution effect, and the Ni layer of the DBC diffused upward.

The Au (0.1 μm) and Pd layers of the DBC substrate were thin, and both films were depleted throughout the diffusion soldering process due to the solid solution effect, so the two metal layers were not observed at the bonding interface.

In terms of strength, as shown in Fig. 5, between 5.19 MPa and 12.16 MPa, prolonging the bonding time did not effectively reduce the holes and gaps, nor did it improve the overall bonding strength, which was limited. The Au (0.1 μm) and Pd layers of the DBC substrate were so thin that both films were depleted by the diffusion soldering process due to the solid solution effect. As a result, these two metal layers were not observed at the bonding interface. The DBC substrate had a thicker surface than that of the Si wafer (3 kÅ), a much larger Ni barrier (45 kÅ), and Sn thickened by DBC metallization diffusion and further reaction with Ni, which was the material source required for the thickening of the interlayer.

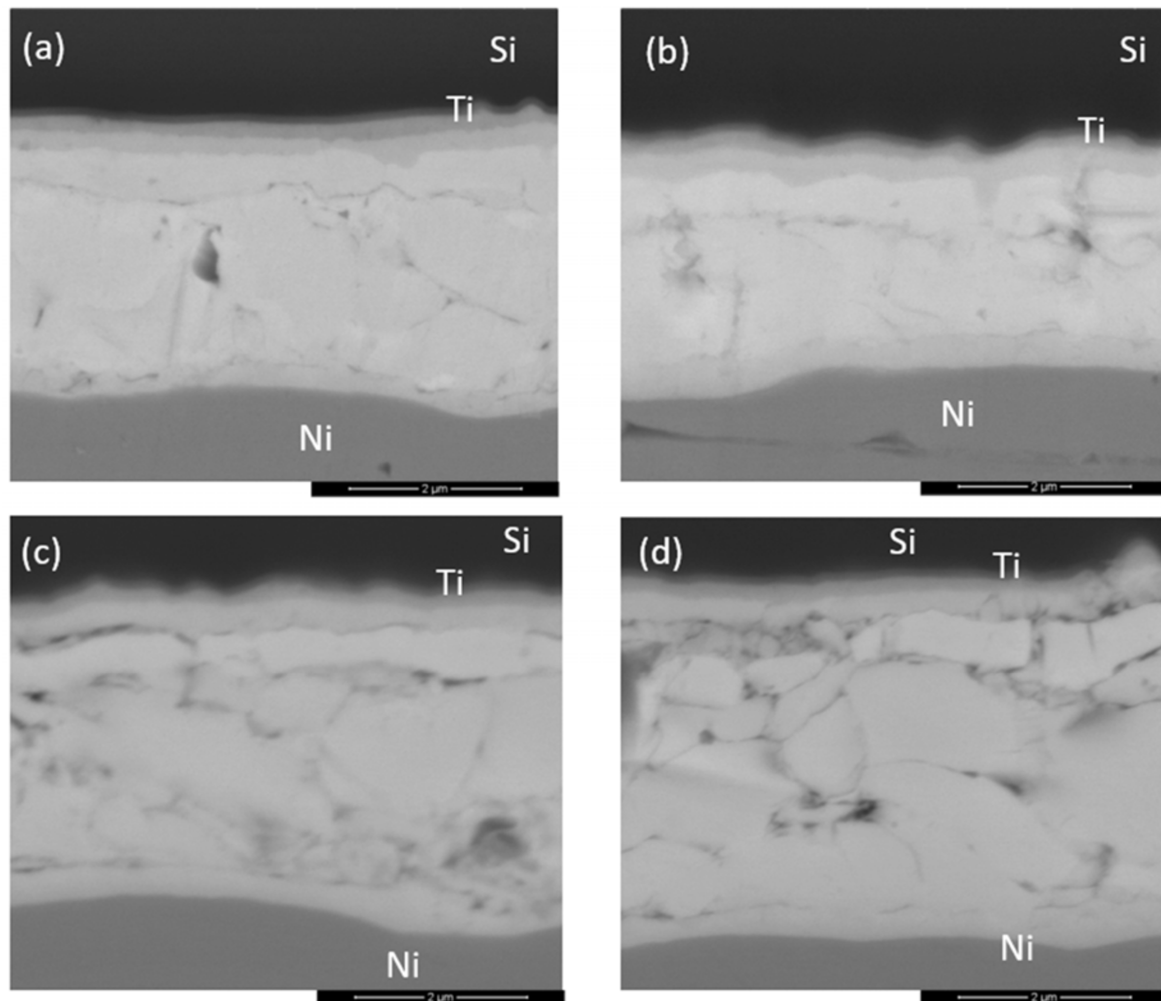

Fig. 4 Morphology of the IMCs s at the bonding interfaces of the wafer Si/Ti/Ni/Sn and DBC Cu/Ni/Pd/Au diffusion bonded at 250 °C for (a) 30 min, (b) 60 min, (c) 90 min, (d) 120 min

In an attempt to reduce the holes and gaps, the bonding temperature was increased at a fixed bonding time of 30 min. The morphology of the Ti/Ni/Sn back-gold structure at different bonding temperatures indicated that the voids were reduced, but a larger gap was detected at the bonding interface. When the bonding temperature was increased to 300 °C, 350 °C, and 400 °C, gaps still existed in the bonding layer. When the bonding temperature was raised to 300 °C and 350 °C, local Ni_3Sn_4 IMCs were generated in the intermediate layer. When the bonding temperature was 400 °C, the intermediate layer tended to become thinner due to the solid solution effect. As shown in Fig. 5, the average bonding strength ranged from 6.15 MPa to 18.03 MPa. The bonding strength was improved slightly by increasing the bonding temperature, but the holes and gaps in the intermediate layer could not be effectively eliminated.

To prevent the formation of voids due to solid–liquid diffusion bonding, intermetallic formation, and diffusion, a back metal layer design of Si/Ti/Ni/Ag/Sn was used in this

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study, as Ag-Sn SLID bonding was expected to produce Ag_3Sn intercalation. Ductile metal compounds with mechanical properties similar to those of pure silver are suitable as stress buffer layers for bonding interfaces. Although the cost of the silver itself may increase the price, this metal still has considerable value for products with high gross profit margins and high-reliability requirements, such as power modules and 3D ICs, because the BGBM metal layer can be much thinner than a similar layer of traditional filling materials. The bonding method has the advantages of thinner thickness and fewer pores.

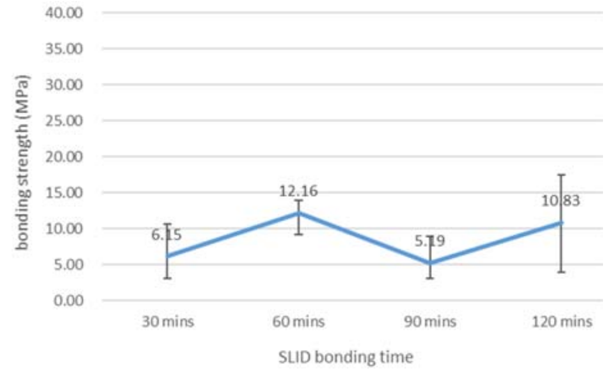

Fig. 5 Average bonding strengths of the wafer Si/Ti/Ni/Sn and DBC Cu/Ni/Pd/Au bonded at 250 °C for various durations

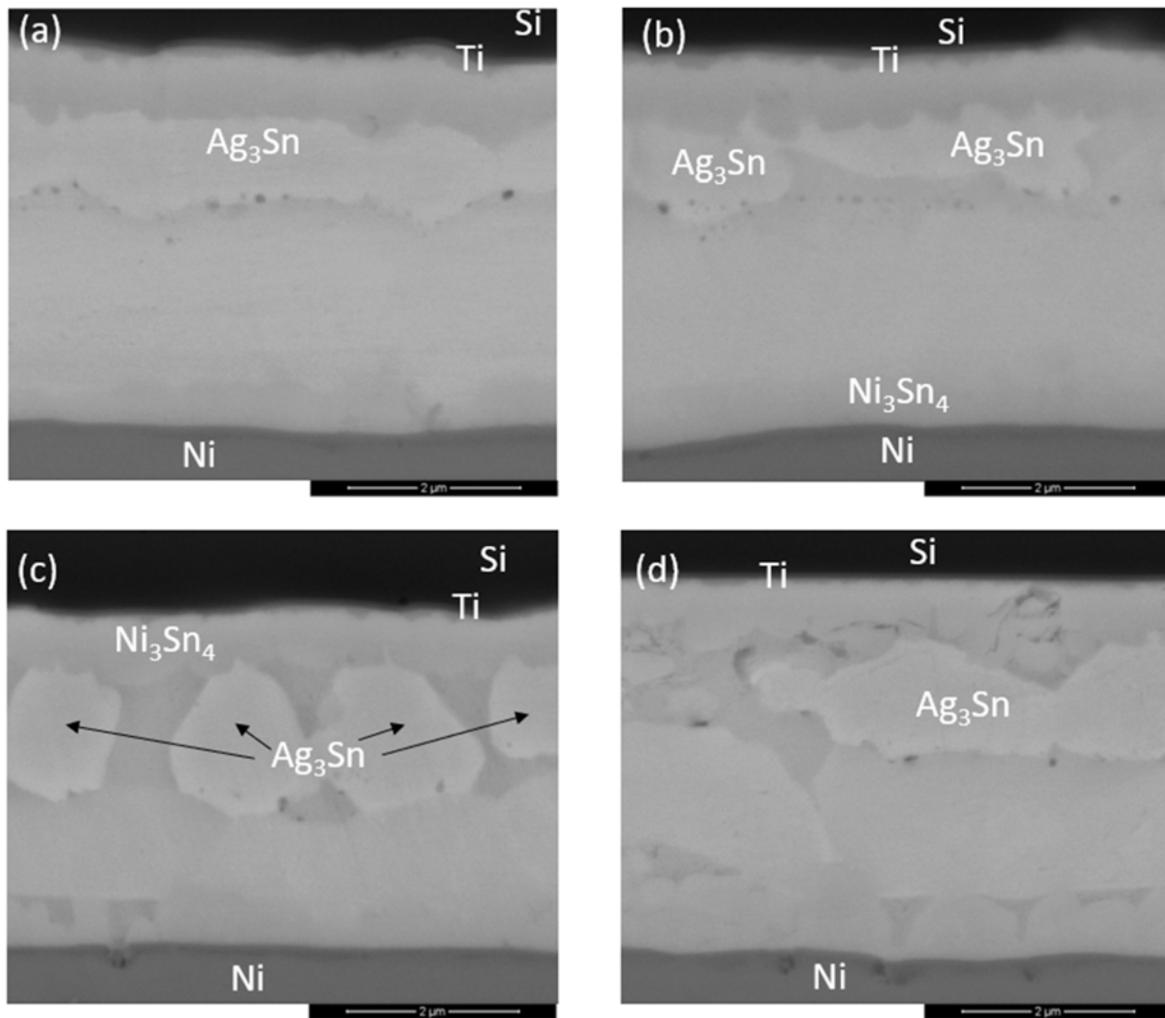

Fig. 6 Morphology of the IMCs s at the bonding interfaces of the Si/Ti/Ni/Ag/Sn wafer and DBC Cu/Ni/Pd/Au diffusion bonded at 250 °C for (a) 30 min, (b) 60 min, (c) 90 min, (d) 120 min

Fig. 6 (a) shows the morphologies of samples bonded at 250 °C for 30 minutes. The formation of IMCs indicates that the reaction mechanism was the interdiffusion of solid solutions. Due to the addition of the silver layer, the formation of holes and voids was prevented. A uniform Ag_3Sn IMC with a thickness of about 0.8 um was observed in the intermediate layer. The Ag layer was completely depleted and reacted with the Sn layer to form Ag_3Sn.

When the bonding time was increased to 60 minutes, as shown in Fig. 6 (b), the Ni layer of the DBC substrate diffused to the upper Sn layer to form Ni_3Sn_4. When the bonding time was increased to 90 minutes, as shown in Fig. 6 (c), the IMCs

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of Ag_3Sn formed a bulk, and part of the Sn diffused toward the Ni layer of the Si wafer to form the intermetallic layer of Ni_3Sn_4.

When the bonding time was increased to 120 minutes, as shown in Fig. 6 (d), the distribution of Ag_3Sn IMCs became uneven. However, even if the bonding time was prolonged, no gaps or voids formed. As shown in Fig. 7, the average bonding strength ranged from 12.98 MPa to 17.32 MPa. The bonding strength was higher than that of the Ti/Ni/Sn control group because the Ag layer filled in the holes and gaps in the intermetallic layer.

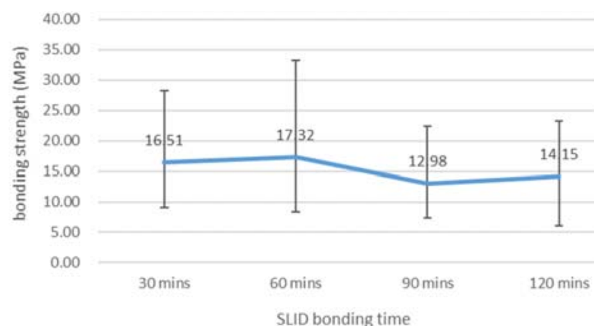

Fig. 7 Average bonding strengths of the Si/Ti/Ni/Ag/Sn wafer and DBC Cu/Ni/Pd/Au bonded at 250 °C for various durations

To improve the bonding strength so as to increase the parameters of the bonding temperature, Ti/Ni/Ag/Sn BSM structures were DBC SLID bonded at different bonding temperatures, and the morphologies were examined. No holes or voids were found in the bonded intermediate layer. After bonding at 275 °C for 30 min, some of the Sn reacted upward with Ni in the Si wafer to form IMCs of Ni_3Sn_2, and another portion of the Sn diffused downward and reacted with the Ni layer of the DBC substrate to form the IMCs of Ni_3Sn_4. At a bonding temperature of 300 °C, the intermediate layer of Ag_3Sn IMCs formed a local block phenomenon. When the bonding temperature was increased to 350 °C and 400 °C, the IMCs of Ag_3Sn gradually formed a uniform intermetallic reaction layer. When the time was prolonged, the upper and lower layers gradually diffused to form the intermetallic layer of Ni_3Sn_4. The melting points of Ag_3Sn, Ni_3Sn_2 and Ni_3Sn_4 are much higher than 790 °C, so the effect of "low bonding temperature and high-temperature application" was achieved. The average bonding strengths ranged from 13.12 MPa to 19.75 MPa. The increment of the overall average bonding strength was due to the increase in bonding temperature. Using backside metallized Ti/Ni/Ag/Sn and SLID bonding to prevent void formation can increase both the path of heat conduction and the electrical conductivity. These bonding structures and techniques are a good design option.

IV. Conclusion

In each SLID bonding combination of Si/Ti/Ni/Sn wafer and Au/Pd/Ni/Cu/Al_2O_3 DBC substrate, many gaps and holes were observed at the bonding interface. In addition, the IMC in the intermediate layer of the bonding interface thickened. This thickening could not be effectively avoided even if the bonding temperature was increased and would have adverse effects on the thermal conductivity, resistivity, and long-term reliability. The optimized BSM was performed with a silver addition to fill the gaps and holes in the interlayer. In the SLID bonding combination of Si/Ti/Ni/Ag/Sn wafer and Au/Pd/Ni/Cu/Al_2O_3 DBC substrate, almost no gaps or holes were observed. In addition, the interlayer of the bond contained ductile Ag_3Sn IMCs, whose mechanical properties are quite similar to those of pure silver, making them suitable for use as a stress buffer layer for the bonding interface. IMCs in the form of Ni_3Sn_4 and Ni_3Sn_2 also formed at the bonding interface. The overall average bonding strength reached 16.51 MPa. When the bonding temperature was increased to 275–400 °C, the average bonding strength was slightly improved to 13.12–19.75 MPa. The research results show that the optimized BSM wafer with SLID bonding technology has great potential for application in the power component and semiconductor industries. Since the melting point of the IMCs formed by low-temperature bonding is much higher than the application temperature, the purpose of high-temperature application is achieved.

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