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A Soft Error Rates Evaluation Method of Combinational Logic Circuit Based on Linear Energy Transfers

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Abstract—Communication stability is the primary concern of communication satellites. Communication satellites are easily affected by particle radiation to generate single event effects (SEE), which leads to soft errors (SE) of combinational logic circuit. The existing research on soft error rates (SER) of combined logic circuit is mostly based on the assumption that the logic gates being bombarded have the same pulse width. However, in the actual radiation environment, the pulse widths of the logic gates being bombarded are different due to different linear energy transfers (LET). In order to improve the accuracy of SER evaluation model, this paper proposes a soft error rates evaluation method based on LET. In this paper, we analyze the influence of LET on the pulse width of combinational logic and establish the pulse width model based on LET. Based on this model, the error rate of test circuit ISCAS'85 is calculated. Experimental results show that this model can be used for SER evaluation.

Keywords—Communication satellite, pulse width, soft error rates, linear energy transfer, LET.

I. Introduction

THE reduction in process size will lead to the increase of communication satellites sensitivity to radiation particles [1], [2]. The injection of particles into the node of an electronic device will result in the accumulation of charge at the node and the generation of single event transients (SET). SETs propagating in combinational logic circuit may be stored by timing element, resulting in circuit output error and affecting the normal operation of the circuit. This error is called soft errors and soft error rates (SER) represent the vulnerability of a circuit to SETs [3]. It is of great significance to establish an accurate SER evaluation model for the anti-radiation research of the combinational logic circuit.

Many scholars have done a lot of research on SER evaluation [4]-[8]. Liu et al. proposed a Monte Carlo model to analyze the reliability of transient pulse on combinational logic circuits [9]. Three masking effects, logical masking, electrical masking, and latch window masking were considered in this model. Paliaroutis et al. established a soft error evaluation model based on layout information and considered the influence of temperature on the pulse widths of SETs [10]. Anglada et al. introduced an innovative way which combined signal probabilities with technology characterization to calculate the SER [11]. Farjaminezhad et al. proposed a shape prediction method for transient faults based on recursive neural network (RNN) [12]. This method could be used to estimate the influence of single or multiple transient faults propagating in a combined circuit. Cai et al. presented a methodology of multi-transient fault simulation based on probability distribution, in which the logical output results were subject to Bernoulli distribution [13].

The probability of a soft error caused by SETs depends on the SET pulse widths [14]. A larger SET pulse width is more easily propagated in the combinational logic circuit and stored by triggers [15]. The existing research on SER of combined logic circuit is mostly based on the assumption that the logic gates being bombarded have the same pulse width. Whereas, in the actual radiation environment, the pulse widths of the logic gates being bombarded are different due to different LETs. In this paper, a SER evaluation model based on LET was proposed. We analyzed the effect of LET on the SET pulse width, studied the modeling of SET pulse width, and finally obtained the soft error rates of combinational logic circuits by circuit level simulation.

The structure of this paper is as follows: Section II introduces the affection of LET on SET pulse widths, Section III proposes the SER evaluation model based on LET. Section IV displays the effects of LET on the SER and verifies the validity of the model.

II. The Affection of LET on SET Pulse Widths

In this paper, the effect of LET on SET pulse widths was analyzed with the basic gate (inverters, NOR gates, and NAND gates) as the research object. This paper took an inverter as an example to present the simulation process. A device-circuit level hybrid simulation model of the basic gates was built on TCAD platform, which had been calibrated with reference to the 40 nm process, as shown in Fig. 1. The NMOS bombarded by particles was the device model, and the rest was the SPICE model. Table I shows the structure and doping parameters of the NMOS.

The heavy ion radiation environment was simulated on the established 3D model. The simulation location was set as the drain center of the NMOS, the direction was vertical incident, the incident particle was heavy ion, and the value of LET ranged from 0.01 pc/μm to 0.05 pc/μm. Fig. 2 reflects the change of SET voltage pulse of inverters. It can be seen from the figure that the width of SET voltage pulse window

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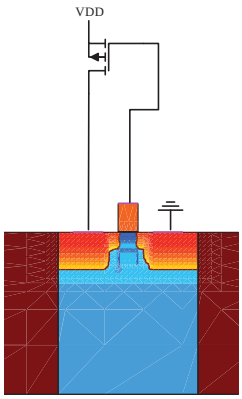

Fig. 1 The structure of inverters

TABLE I
THE STRUCTURE AND DOPING PARAMETERS OF THE NMOS

Parameter	Value
The length of the channel(nm)	55
Gate oxide layer thickness(nm)	1.25
Source and drain doping concentration(cm-3)	1.00e21
VT doping concentration(cm-3)	1.29e19
Substrate doping concentration(cm-3)	6.00e16

increases with the increase of LET. The reason was as follows: With the increase of LET, the concentration of electron hole pair generated by particle incident increased, and the drain needed a longer diffusion time to recover to the initial state. SET pulse width was defined as FWHR (the full width of half rail). The value of FHWR was calculated according to the following expression.

$$FWHR = T_1 - T_2 \tag{1}$$

where T_1 is the time to recover to half of voltage amplitude, T_2 is the time to drop to half of voltage amplitude.

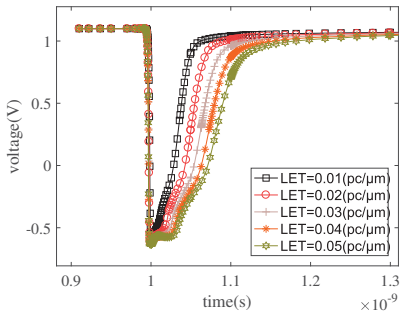

Fig. 2 The change of SET voltage pulse of inverters

According to (1), the SET pulse width of the basic gates was obtained. As shown in Fig. 3, similar to the inverters, the NOR gates, and NAND gates also conform to the phenomenon that the pulse width increases as the LET increases. It can also be seen that the SET pulse widths of NAND gates and NOR gates are larger than that of inverters.

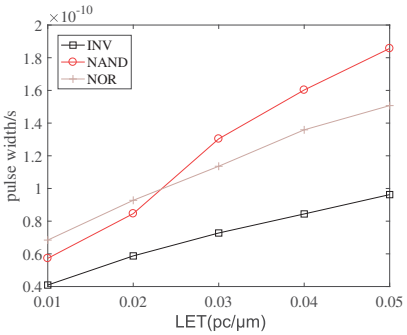

Fig. 3 SET voltage pulse of base gates

III. A SER EVALUATION MODEL BASED ON LET

Based on the above research on the influence of LET on SET pulse widths, this section proposed a LET-based soft error rates evaluation model, which took into account logical masking, electrical masking, latching masking and the random injection of SET pulse. SET pulse widths of the basic gates were modeled by the Polyfit function in the MATLAB. The pulse widths of the basic gates were obtained as follows:

$$y_1 = 9.34e{-}10 \cdot x + 4.61e{-}11 \tag{2}$$

$$y_2 = -6.74e{-}10 \cdot x^2 + 1.80e{-}9 \cdot x + 5.95e{-}11 \tag{3}$$

$$y_3 = \begin{cases} -2.07e{-}9 \cdot x^2 + 3.19e{-}9 \cdot x + 3.65e{-}11 & x < 0.4 \\ 1.01e{-}9 \quad 0.4 \le x \le 0.6 \end{cases} \tag{4}$$

where y_1 is the pulse width of inverters, y_2 is the pulse width of NOR gates, y_3 is the pulse width of NAND gates, x is the value of LET.

Fig. 4 shows the structure diagram of the soft error rates evaluation model, including the following parts.

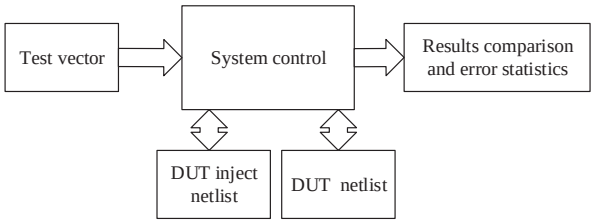

Fig. 4 The structure diagram of the proposed model

1) System control: This part mainly included test vector address generation, SET pulse width generation, injection time control and injection position control. The pseudocode is shown in Table II.
2) DUT inject netlist: This was the netlist file for the circuit under test. The DC synthesis tool was used to synthesize the circuit under test into gate level netlists containing only inverters, NAND gates and NOR gates. The pulse injection model, derived from the Pulse model, was inserted into each of the base gates in the netlist.

3) DUT netlist: Unlike DUT inject netlist, this netlist did not insert the pulse injection model and was used to compare with the output of DUT inject netlists.
4) Test vector: Traversal of all inputs would greatly increase the simulation time. In order to save time, random vector was used as the input of the netlist.
5) Results comparison and error statistics: This part compares the output results of DUT Inject netlists and DUT Netlists by XOR operation. If the value was 0, there was no error. Otherwise, the error count was increased by 1.

TABLE II
THE PSEUDOCODE OF SYSTEM CONTROL

```
    Algorithm : system ctrol
1   Setting the number of test vector
2   Setting the injection time
3   Setting the injection location
4   Setting the number of LET
5   For netlist in the list of netlist
6     For LET in the list of LET
7     set the pulse-width-inv as the pulse-width of inverters by (2)
8     set the pulse-width-nor as the pulse-width of NOR gates by (3)
9     set the pulse-width-nand as the pulse-width of NAND gates by (4)
10      For injection location in the list of injection location
11        For a random input vector in the input vector
12          For injection time in the list of injection time
13          Simulate the target netlist
14          output-inject <- the output of DUT inject netlist
15          output-unject <- the output of DUT netlist
16          if (output-unject!=output-inject)
17            counter-error ++
18            END
19          END
20        END
21      END
22    END
23  END
```

IV. ANALYSIS OF RESULTS

A. Analysis of SET Pulse Width Model

The SET pulse width model was established by fitting the SET pulse widths simulated by TCAD. The value of LET used for SET pulse width modeling ranged from 0.01 pc/μm to 0.6 pc/μm. MSE and regression coefficient (R^2) were taken as metrics of the model accuracy.

$$R^2 = 1 - \frac{\sum_{i=1}^{n} (y_i - \hat{y}_i)^2}{\sum_{i=1}^{n} (y_i - \bar{y})^2} \tag{5}$$

$$MSE = \frac{1}{n} \sum_{i=1}^{n} (y_i - \hat{y}_i)^2 \tag{6}$$

where n is the number of data; y_i is the factual data and $\hat{y}_i$ is the predicted data.

The closer regression coefficient is to 1, the smaller MSE is, indicating that the fitting effect is better. Fig. 5 shows the comparison between TCAD simulation results and this model. From Table III and Fig. 5, it could be found that both were quite close and could be used for subsequent research.

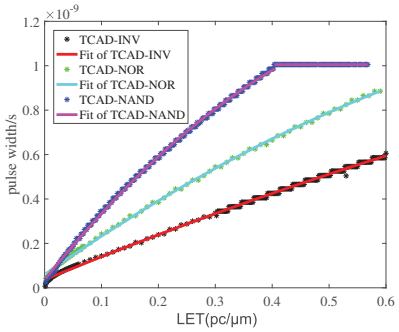

Fig. 5 The comparison between TCAD and this model

TABLE III
MODEL INDICATORS

base gates	R^2	MSE
inverters	0.99715	8.39e-23
NAND gates	0.99936	3.02e-20
NOR gates	0.99924	5.79e-23

B. Analysis of SER Model

Using the LET-based SER evaluation model proposed above, this paper analyzed the soft error rates under different LET of part of circuits belonging to the ISCAS'85 benchmark set. The SMIC 40 nm process library was designated as the comprehensive target library in this paper. The number of test vectors was 150 and the value of LET ranged from 0.1 pc/μm to 0.5 pc/μm. The operating environment of this model was as follows: CPU was Intel Core i5-8500, GPU was NVIDIA GeForce GTX 1060 5GB.

Fig. 6 presents the soft error rates of the ISCAS'85 Benchmark circuits. As LET increased, the probability of circuit error increased. This phenomenon was related to the SET pulse widths. As LET increased, SET pulse widths increased, and the probability of pulse propagating in combination logic and being locked by timing unit also increased. The probability of a SET pulse being stored increased, and so did the probability of an output error.

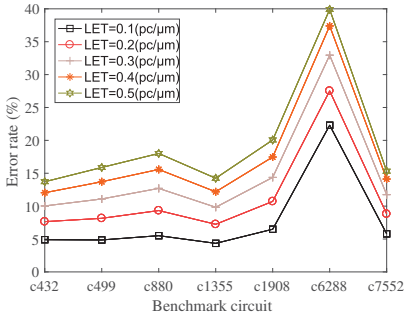

Fig. 6 The error rates of the ISCAS'85 benchmark circuits

The validity of the model was demonstrated by comparing with [9]. The circuit reliability analysis data in [9] when pulse width was 200 ps were compared with the error rates in this model when LET was 0.1 pc/μm. We set the LET value of

this model to 0.1 pc/μm, which meant that the pulse width of inverters was 140 ps, the pulse width of NOR gates was 233 ps, and the pulse width of NAND gates was 335 ps. Fig. 7 shows the data comparison between this model and [9]. As can be seen from Fig. 7, the trend of data in this model is almost the same as that in [9]. It should be noted that, in general, various algorithms to study the soft error rates would carry out different simplified processing, and this model adopted the 40 nm process, while the comparison model adopted the 65 nm process. Different process technologies would also cause deviations in the results.

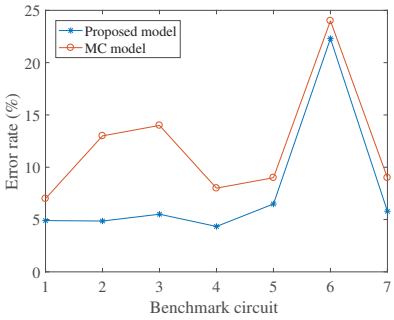

Fig. 7 The error rates of the proposed model and [9]

The model was set as two cases of the same and different pulse widths of the basic gates. By comparing the error rates in these two cases, the research significance of the model was further proved. In the first case, the basic gate used the same pulse width of 140 ps; in the second case, we set the LET value as 0.1 pc/μm, and the pulse widths corresponding to the basic gates were 140 ps, 233 ps and 335 ps respectively. As we can see from Fig. 8, in the first case, the soft error rates may be underestimated, resulting in an inaccurate assessment of the soft error rates. Similarly, the soft error rates may be exaggerated when the same pulse width was 335 ps.

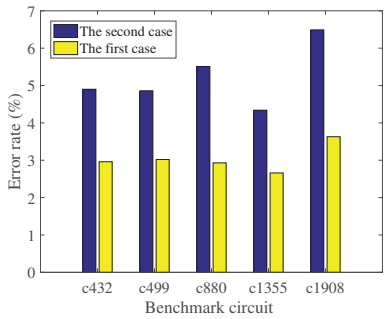

Fig. 8 The error rates in case one and the error rates in case two

V. Conclusion

In this work, a SER evaluation method of combinational logic circuit based on LET was proposed to predict SER under different LETs. Compared with the model using the same pulse width, the SER prediction was more accurate. If the influence of LET on the pulse widths of the basic gates was not considered, the soft error rates assessment would be inaccurate. This model can be applied to the study of satellite radiation resistance.

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References

[1] Lwin, Ne Kyaw Zwa and Sivaramakrishnan, "Single-Event-Transient Resilient Memory for DSP in Space Applications," 2018 IEEE 23rd International Conference on Digital Signal Processing (DSP), pp. 1-5 Nov. 2018.

[2] T. Li, H. Liu and H. Yang, "Design and Characterization of SEU Hardened Circuits for SRAM-Based FPGA," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 27, no. 6, pp. 1276-1283, June 2019, doi: 10.1109/TVLSI.2019.2892838.

[3] M. R. Rohanipoor, B. Ghavami and M. Raji, "Improving Combinational Circuit Reliability Against Multiple Event Transients via a Partition and Restructuring Approach," in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 39, no. 5, pp. 1059-1072, May 2020, doi: 10.1109/TCAD.2019.2907922.

[4] T. Uemura et al., "Investigation of alpha-induced single event transient (SET) in 10 nm FinFET logic circuit," 2018 IEEE International Reliability Physics Symposium (IRPS), 2018, pp. P-SE.1-1-P-SE.1-4, doi: 10.1109/IRPS.2018.8353689.

[5] N. Pande, S. Kumar, L. R. Everson and C. H. Kim, "Understanding the Key Parameter Dependences Influencing the Soft-Error Susceptibility of Standard Combinational Logic," in IEEE Transactions on Nuclear Science, vol. 67, no. 1, pp. 116-125, Jan. 2020, doi: 10.1109/TNS.2019.2959922.

[6] S. A. Olowogemo, A. Yiwere, B. -T. Lin, H. Qiu, W. H. Robinson and D. B. Limbrick, "Electrical Masking Improvement with Standard Logic Cell Synthesis Using 45 nm Technology Node," 2020 IEEE 63rd International Midwest Symposium on Circuits and Systems (MWSCAS), 2020, pp. 619-622, doi: 10.1109/MWSCAS48704.2020.9184651.

[7] M. R. Rohanipoor, B. Ghavami and M. Raji, "Improving Combinational Circuit Reliability Against Multiple Event Transients via a Partition and Restructuring Approach," in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 39, no. 5, pp. 1059-1072, May 2020, doi: 10.1109/TCAD.2019.2907922.

[8] Z. Zhang et al., "Extrapolation Method of On-Orbit Soft Error Rates of EDAC SRAM Devices From Accelerator-Based Tests," in IEEE Transactions on

Nuclear Science, vol. 65, no. 11, pp. 2802-2807, Nov. 2018, doi: 10.1109/TNS.2018.2875051.

[9] B. Liu and L. Cai, "Monte Carlo Reliability Model for Single-Event Transient on Combinational Circuits," in IEEE Transactions on Nuclear Science, vol. 64, no. 12, pp. 2933-2937, Dec. 2017, doi: 10.1109/TNS.2017.2772267.

[10] G. Ioannis Paliaroutis, P. Tsoumanis, N. Evmorfopoulos, G. Dimitriou and G. I. Stamoulis, "A Placement-Aware Soft Error Rate Estimation of Combinational Circuits for Multiple Transient Faults in CMOS Technology," 2018 IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT), 2018, pp. 1-6, doi: 10.1109/DFT.2018.8602855.

[11] M. Anglada, R. Canal, J. L. Aragón and A. González, "Fast and Accurate SER Estimation for Large Combinational Blocks in Early Stages of the Design," in IEEE Transactions on Sustainable Computing, vol. 6, no. 3, pp. 427-440, 1 July-Sept. 2021, doi: 10.1109/TSUSC.2018.2886640.

[12] Farjaminezhad R , Safari S , Moghadam A . "Recurrent Neural Networks Models for Analyzing Single and Multiple Transient Faults in Combinational Circuits." Microelectronics Journal, 2021(7553):104993.

[13] Cai S , He B and Wang W. "Soft Error Reliability Evaluation of Nanoscale Logic Circuits in the Presence of Multiple Transient Faults". Journal of Electronic Testing, vol. 36, 2020.

[14] B. Narasimham et al., "On-Chip Characterization of Single-Event Transient Pulsewidths," in IEEE Transactions on Device and Materials Reliability, vol. 6, no. 4, pp. 542-549, Dec. 2006, doi: 10.1109/TDMR.2006.885589

[15] H. Pahlevanzadeh and Q. Yu, "Systematic analyses for latching probability of single-event transients," Fifteenth International Symposium on Quality Electronic Design, 2014, pp. 442-449, doi: 10.1109/ISQED.2014.6783358.