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Artificial Neurons Based on Memristors for Spiking Neural Networks

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***Abstract*—**Neuromorphic computing based on spiking neural networks (SNNs) has emerged as a promising avenue for building the next generation of intelligent computing systems. Owing to their high-density integration, low power, and outstanding nonlinearity, memristors have attracted emerging attention on achieving SNNs. However, fabricating a low-power and robust memristor-based spiking neuron without extra electrical components is still a challenge for brain-inspired systems. In this work, we demonstrate a TiO_2-based threshold switching (TS) memristor to emulate a leaky integrate-and-fire (LIF) neuron without auxiliary circuits, used to realize single layer fully connected (FC) SNNs. Moreover, our TiO_2-based resistive switching (RS) memristors realize spiking-time-dependent-plasticity (STDP), originating from the Ag diffusion-based filamentary mechanism. This work demonstrates that TiO_2-based memristors may provide an efficient method to construct hardware neuromorphic computing systems.

***Keywords*—**Leaky integrate-and-fire, memristor, spiking neural networks, spiking-time-dependent-plasticity.

I. Introduction

INSPIRED by the human brain's highly parallel data processing capability, artificial neural networks (ANNs) have been developed to run large-scale neuromorphic and deep learning algorithms. On the embedded system or Internet of Things (IoT) edge computing side, such as autonomous driving, smart sensors, and wearable devices, artificial neural networks have severe design constraints due to their poor performance, high power consumption, and large area. SNNs, often regarded as third-generation brain-inspired neural networks (Maass, 1997) [1], that enable event-driven, sparse and irregular input encoding, can be highly power-efficient and have competitive capabilities to deal with low latency and low power consumption tasks. Memristor is one of the most promising candidates for achieving SNNs due to its high-density integration, low-power, and outstanding nonlinearity [1]-[3]. Some recent researches have proved that the memristor can be able to implement SNNs [5], such as the memristor used to comply with SNNs structure in the "Tianjic" chip reported in 2019 [6] and the "TrueNorth", similarity. Therefore, the memristor has been considered to have the potential to implement SNNs in hardware.

In our work, we fabricate a low-power (1.4 μW) artificial neuron based on a single memristor ($Ag/TiO_2/Pt$). It has the RS and TS modes, by using different compliance currents (I_{cc}) at 7 μA and 1 mA, respectively [7]-[10]. In addition, the resultant device exhibited excellent electrical performance, such as low and concentrated switching voltage (~0.25 V), large switching window (> 10^4), and good retention properties (~4000 s). Our memristors also show remarkable analog behavior after cycling operation, demonstrating brain-inspired emulation ability. Additionally, the single device implements STDP learning rules under non-volatility and LIF neuron simulation under volatility, and we design a LIF model that can be used for SNNs with a network scale of 784×10 single-layer FC. In the handwritten digit recognition set Mixed National Institute of Standards and Technology (MNIST) database test, the accuracy rate can reach 91.57%. Finally, the emulations of the synaptic and neuron functions have been successfully implemented by $Ag/TiO_2/Pt$ memristors, revealing the great potential in developing low-power brain-inspired computing [11]-[19].

II. Experiments

The devices in this work consist of a 100 nm Ag/80 nm TiO_2/80 nm Pt structure in a crossbar array (Fig. 1 (a)).

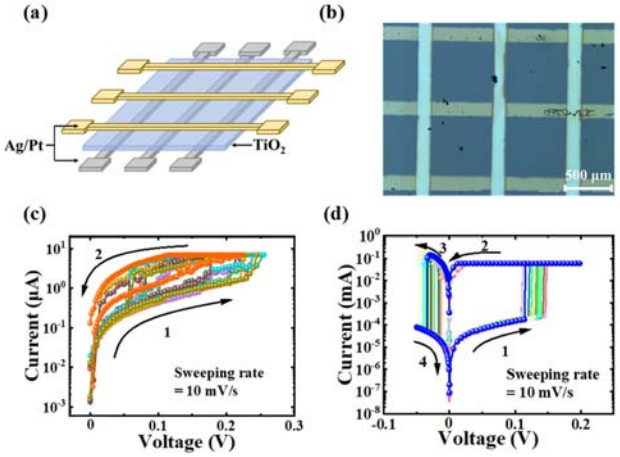

Fig. 1 (a) The structure diagram of the $Ag/TiO_2/Pt$ device; (b) The metallographic microscopy crossbar array image; (c) TS behaviors of devices with low I_{cc} of 7 μA; (d) The device showed RS behaviors with a high I_{cc} of 1 mA

As for the fabrication, first, an 80 nm-thick Pt layer was deposited on the SiO_2/Si substrate through the reticle as the bottom electrodes (BEs). Then, an 80 nm-thick TiO_2 layer serving as a resistive layer was sputtered from the SiO_2 target with an Ar gas with a flow rate of 10 sccm and a pressure of 1

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morr. Finally, 100 nm-thick Ag was sputtered and patterned for the top electrodes (TEs). The radio frequency power was fixed at 100 W, 100 W, and 50 W and under a background vacuum of 4.5×10^{-5} Pa. The optical image of the vertical structure Ag/TiO_2/Pt is shown in Fig. 1 (b). Electrical characteristics of our devices were measured by a four-probe system Cascade Summit 11,000 and Keithley 4200A-SCS semiconductor characterization analyzer.

III. Results and Discussion

Fig. 1 (c) shows the volatile TS behavior in our device under direct current (DC) voltage sweeping with a low I_{cc} (7 μA). When the positive voltage applied on the device, the current increases rapidly at the threshold voltage (0.25 V) and then the device switches to the high conductance state (HCS). With the voltage decreasing below a certain value (0.1 V), the HCS returns back to the initial low conductance state (LCS). The volatiles TS behavior may be ascribed to the spontaneous fracture of Ag conductive filaments (CFs).

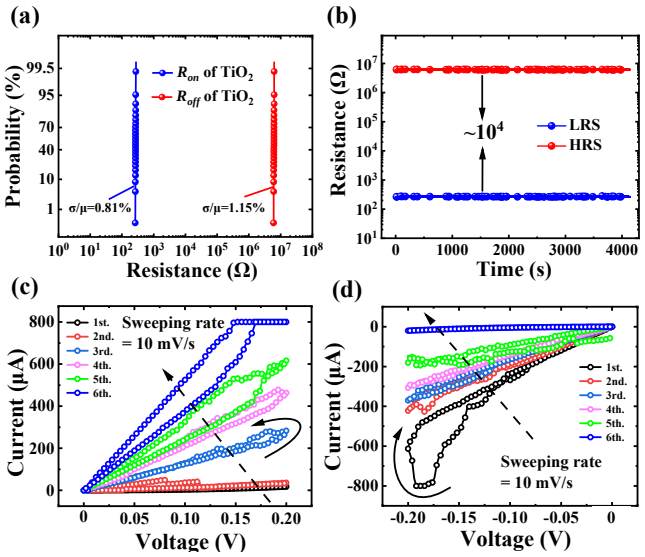

Fig. 2 (a) Cumulative probability distribution of ON and OFF resistance states during 100 cycles; (b) Retention of the Ag/TiO_2/Pt devices; (c) Memristive current under six consecutive voltage sweeps from 0 V to 0.2V (Voltage sweeping rate = 10 mV/s); (d) Six consecutive voltage sweeps from 0 V to -0.25 V with a 10 mV/s sweeping rate

The DC *I-V* characteristics in Fig. 1 (d) exhibit repeatable bipolar switching between the high resistance state (HRS) and low resistance state (LRS) of the Ag/TiO_2/Pt device under a compliance current of 1 mA. Under a large voltage and high I_{cc} (1 mA), the responded current of the device straightly increases at 0.12 V (denoted as the current jump process in the inset of Fig. 1 (d)). A sweeping voltage (0 V to 0.2 V to 0 V to -0.1 V to 0 V) was applied to the device, which exhibited non-volatile RS behaviors. Similarly, in the positive bias voltage, the device gradually changed from HRS to LRS under a sweeping voltage from 0 V to 0.2 V, named the process of "SET". Subsequently, by applying a negative voltage sweeping from 0 V to -0.1 V, the resistive state of the device returns to the HRS from the LRS, called the process of "RESET".

Drawing the cumulative probability plot is an appropriate method to study resistance state changes, which demonstrates extremely valuable information to distinguish HRS and LRS. A cumulative probability plot of the resistance of the OFF-State (R_{off}) and ON-State (R_{on}) is shown in Fig. 2 (a). According to the cumulative probability distribution, the coefficient of variation (CV) of R_{on} is 0.81% and R_{off} is 1.15% in devices respectively. Moreover, the devices can be switched between HRS and LRS keeping enough resistance ratio between them. As illustrated in Fig. 2(b), the R_{off}/R_{on}-states and the memory window of the devices can last about 4000 s, which demonstrates that the device has good non-volatility. As shown in Figs. 2 (c) and (d), when six consecutive positive/negative voltage sweeps are applied on the Ag/TiO_2/Pt device, the conductance of the device increases/decreases continuously.

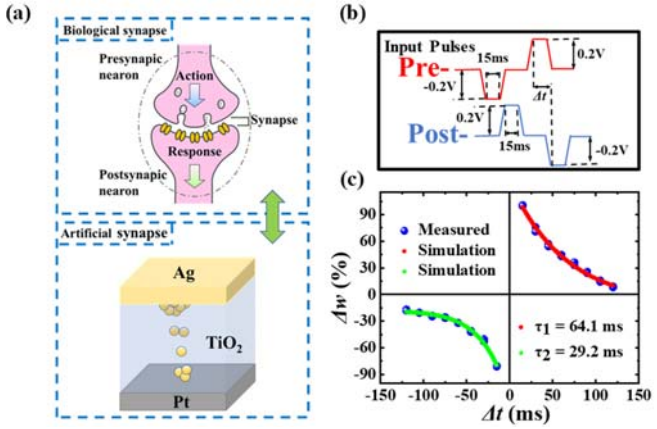

Fig. 3 (a) Schematic illustration of a biological synapse and the structure of Ag/TiO_2/Pt synaptic device, (b) Pulse shapes in the conductance modulation measurement, (c) Implementation of STDP in the Ag/TiO_2/Pt

Fig. 3 (a) shows the schematics illustration of a biological synapse and the structure of the Ag/TiO_2/Pt synaptic device. When a positive bias is applied on the Ag electrode, the Ag atoms are oxidized to Ag cations which inject into the insulating layer under the electrical field, resulting in the increase of device conductance. This process can be used to emulate the influx of Ca^{2+} in bio-synapse, which enhances the synapse weight by releasing more neurotransmitters [20]. The TEs and BEs of the device were used to emulate the presynaptic and postsynaptic of the neurons, respectively. The conductance of the device was modulated by changing the interval of pulses arriving at the TEs and BEs. The triangle-like pulse sequence shown in Fig. 3 (b) was applied to both the TEs and the BEs. The interval between the presynaptic and postsynaptic pulses was taken as Δt. If the two pulses arrive at the same time, it is recorded as $\Delta t = 0$. If the presynaptic pulse arrives earlier than the postsynaptic pulse, it is recorded as $\Delta t > 0$. Conversely, when the presynaptic pulse arrives later than the postsynaptic, it is recorded as $\Delta t < 0$. The absolute value of the voltage across the device when $\Delta t < 0$ is the same as that of $\Delta t > 0$,

but has the opposite sign. The change in conductance is regarded as the change in synaptic weight Δw, according to the exponential equation proposed:

$$\Delta w = \begin{cases} W_+ e^{\left(-\frac{|\Delta t|}{\tau_1}\right)}, if \Delta t > 0 \\ W_- e^{\left(-\frac{|\Delta t|}{\tau_2}\right)}, if \Delta t < 0 \end{cases} \quad (1)$$

where, W_+ and W_- represent the initial weight, τ_1 and τ_2 are the membrane time constant [21].

The W_+ and W_- obtained by fitting the experimental data are 138.61 and 103.46, respectively. The time constants τ_1 and τ_2 are 64.1 ms and 29.2 ms, respectively.

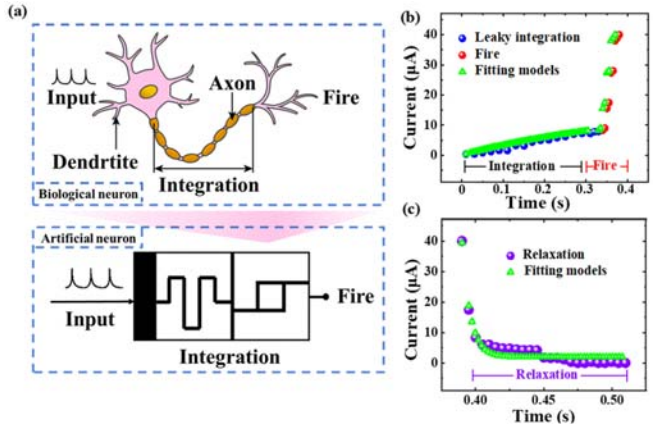

Fig. 4 (a) Schematics of a biological neuron receiving input from other neurons through interconnected synapses, (b) Plot of response conductivity and fitting models (green triangles) of the integration (blue balls), firing (red balls) function of the device, (c) The experimental conductivity of the relaxation (purple balls) function and fitting models (green triangles)

The LIF neuron model as a well-studied model of neuron works effectively in spiking and event-based networks and is quite fast to simulate, and particularly attractive for large-scale network simulations. Fig. 4 (a) shows a schematic diagram of our memristors as an artificial neuron. The LIF model is described by the neuron membrane potential:

$$\tau \frac{du}{dt} = -[u(t) - u_{rest}] + RI(t) \quad (2)$$

where, $u(t)$ represents the membrane potential at time t, R is the membrane resistance and u_{rest} is the reset value [22].

Equation (2) describes a simple parallel resistor-capacitor circuit where the leakage term is due to the resistor and the integration of $I(t)$ is due to the capacitor. The total input current, $I(t)$, is generated by the activity of pre-synaptic neurons. When $t > 0$, assuming $I(t) > 0$, the initial value is the u_{rest}, and the solution of (3) is:

$$u(t) = -u_{rest} + RI_0 \left[1 - e^{\left(-\frac{t}{\tau}\right)}\right] \quad (3)$$

As shown in Figs. 4 (b) and (c), the small spherical image realizes the three processes of integration, firing, and leakage of LIF neurons respectively. The resulting constant u_{rest} is 0.43 mV and τ is 9.41 ms. In this work, one single TiO_2-based memristor was in terms of controlling the emulation of the LIF neuron accurately. The function of a LIF neuron has been experimentally emulated by a single TiO_2-based memristor without any auxiliary circuits, which may provide a low-cost candidate for the implementation of artificial neurons in a neuromorphic system [23].

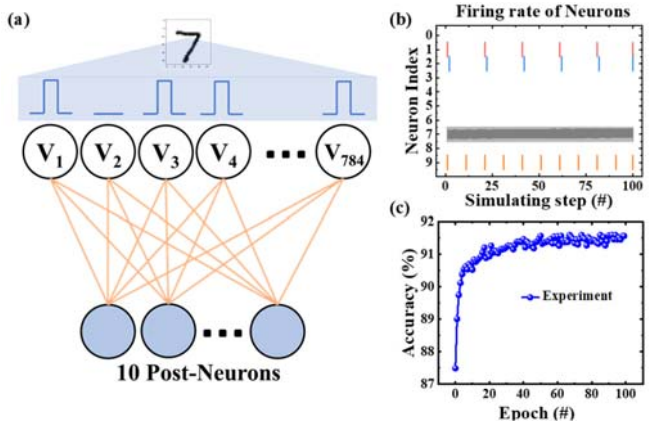

Fig. 5 (a) Schematic layout of the two-layer SNN for MNIST digit recognition, (b) The Pulses and Firing rate of the output layer, (c) The recognition accuracy of 91.57%

As shown in Fig. 5 (a), the FC network consists of an input layer and a supervised learning layer. In the input layer, there are 784 neurons, which represent the 28 × 28 pixels of each image of characters from the MNIST, and each neuron is connected to the 10 neurons in the supervised learning layer through 784 memristor LIF neurons. The 10 output neurons in the supervised learning layer represent the numbers 0-9, respectively. During the training process, the MNIST digit is transferred into a Poisson-distributed spike train, with firing rate proportional to the intensity of the corresponding pixels, and the fitted LIF model is used as the activation function. Simultaneously, the gradient surrogate function was chosen to implement error backpropagation. Fig. 5 (b) shows the pulse firing rate after the integration of 10 neurons, and the number 7 with the highest firing rate is selected as the accurate answer. After testing our SNNs on the MNIST dataset for 100 epochs, the accuracy obtained is shown in Fig. 5 (c), which is up to 91.57%.

IV. Conclusion

In summary, we fabricated an Ag/TiO_2/Pt memristor with volatile and non-volatile properties for biomimetic synapses and the construction of LIF bio-inspired neurons. By fitting non-volatile memristor and LIF model to artificial neurons, the leakage, spatiotemporal integration, and discharge functions in biological neurons are successfully simulated and a simple FC two-layer (784 × 10) supervised SNNs implemented for a recognition accuracy of 91.57%. This work shows the capability of memristors for pattern recognition applications in

SNNs.

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