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A Low Power and High-Speed Conditional-Precharge Sense Amplifier Based Flip-Flop Using Single Ended Latch

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***Abstract*—Paper presents a low power, high speed, sense-amplifier based flip-flop (SAFF). The flip-flop's power consumption and delay are greatly reduced by employing a new conditionally precharge sense-amplifier stage and a single-ended latch stage. Glitch-free and contention-free latch operation is achieved by using a conditional cut-off strategy. The design uses fewer transistors, has a lower clock load, and has a simple structure, all of which contribute to a near-zero setup time. When compared to previous flip-flop structures proposed for similar input/output conditions, this design's performance and overall PDP have improved. The post layout simulation of the circuit uses 2.91µW of power and has a delay of 65.82 ps. Overall, the power-delay product has seen some enhancements. Cadence Virtuoso Designing tool with CMOS 90nm technology are used for all designs.**

***Keywords*—high-speed, low-power, flip-flop, sense-amplifier**

I. Introduction

Digital circuits are characterized by their extreme responsiveness and ultra-low power consumption. Flip-flops' delay and power directly affect the performance and power of digital systems as basic storage elements. Flip-flops account for a major amount of the digital system's power consumption, as explained in [1]. Furthermore, the flip-flop's setup-time and CK-to-Q delay directly affects the system's maximum clock frequency.

In digital systems, optimizing the delay and power of flip-flops may have a direct effect on performance and power consumption. The master–slave flip-flop is the most common type of flip-flop in digital systems (MSFF).Since the SAFF was first introduced in [2], it has been hailed as one of the fastest flip-flops ever devised. A sense-amplifier (SA) stage and a slave latch make up the SAFF. It is possible for the SA stage to capture data immediately following the rising edge of CK, and the output of the SA stage can be maintained during the positive half cycle of CK. As a result, the The pulse-triggered flip-flop no longer has a size issue.The single-ended latch that follows the differential master sensing stage eliminates most of the drawbacks of existing flip-flop architectures.

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As part of the investigation, a variety of SAFF designs were examined.The conventional SAFF [3], M-SAFF [4], Stroll's SAFF [5], Kim's SAFF[6], Lin's SAFF [7], and Jeong's SAFF [8] are all compared in this paper. The master sensing stage amplifies weak signals and transmits them to the slave latch in the form of a small rail. All that is needed is SR (set/reset) NAND logic for these latch structures. SAFF is well-suited for low VDD applications, as previously mentioned. A new SAFF structure is introduced in this paper to address all of the problems caused by previous flip-flop designs.

Herein, a SAFF with high speed and low power consumption is proposed. Power consumption during pre-charging is reduced by using a new sense-amplifier with a lower pre-charge load. For fast, low-power and glitch-free operation a single-ended latch is employed.

II. overview of previous SAFF architectures

Figure 1 depicts the conventional SAFF [3] using a SA and a NAND2-based set-reset (S-R) latch. This is how the SAFF works: Latch maintain the output data while precharging the SN and RN voltages to VDD. At the rising edge of CK, the pre-charge transistors MP1 and MP4 are turned off and MN5 is turned on. According to the input data, the SN and RN pre-charge nodes are discharged to zero while the other remains VDD. Latch captures and stores the new data from SA stage. MN6 always-on transistor maintains the SA output when CK is high.The S-R latch's unbalanced delay and the pre-charge operation's large power are the main issues with the SAFF. The always-on transistor also reduces the SAFF's designed to sustain low supply voltages.

Modified SAFF (MSAFF) design, as illustrated in Fig. 2, is comparable to Nikolic [4]'s master stage, which increases the circuit's speed performance at the cost of increasing devices and gradually increasing the power consumption. A SAFF latch was proposed by Kim et al. in [6] using two N-C2MOS circuits and two pairs of inverters. Using a single-ended latch, Lin et al. improved the latch in [6] to a significant reduction in power consumption [7]. Figure 4 shows the latch schematic in Lin's SAFF. Due to the lack of logic between SN and the output Q, the delay of this type of SAFF is significantly than that of a conventional SAFF. When output Q and the next data input are both high, however, there is a large glitch that will increase SAFF's power consumption. Back-to-back inverters will also increase power consumption. To reduce the number

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of glitches in outputs, Strollo implemented the stacked n-mos transistor at the discharging path [5] in his later redesign of the slave latch depicted in Figure 3. In addition, the stacked transistor causes a severe current contention problem at low VDD. For low VDD applications, a SAFF-TCD (SAFF-TCD) technique was used, which generated a detection signal at the master stage of the sense-amplifier to notify the slave latch that completed the transition, and this TCD signal was connected to the discharging pull-down path, increasing operational yield and overcoming issues of current contention. It will take longer for Jeong's SAFF[8] to propagate data because of its transition completion detecting method.

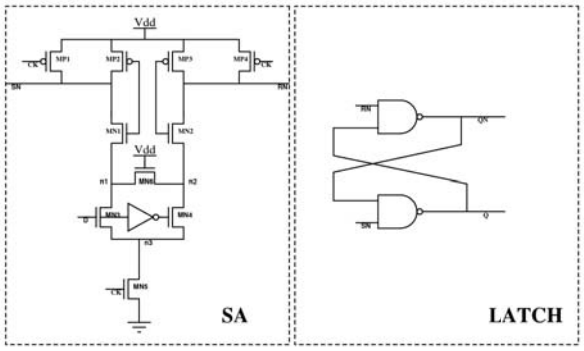


Fig. 1. Conventional SAFF circuit

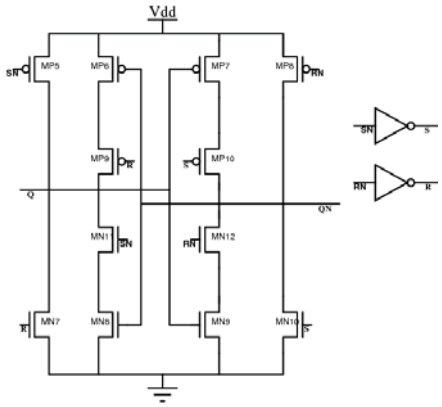


Fig. 2. Modified Nikolic's SAFF latch circuit

III. Design Of the Proposed SAFF

The schematic diagram of the flip flop is presented in Figure 6. it consists of two stages, namely the sensing stage(SA) and the latch stage(LATCH). In the precharge phase as presented in SA stage, when D is low, SN will be set to high, and if D goes high, then RN will be set to high. This state is similar to the conditional precharging technique, applied to the sensing stage of the designed SAFF, to avoid redundant transitions in arriving data input due to critical paths internal nodes. Here, two input controlled PMOS transistors, MP1 and MP2, are embedded on the precharging path of sensing stage

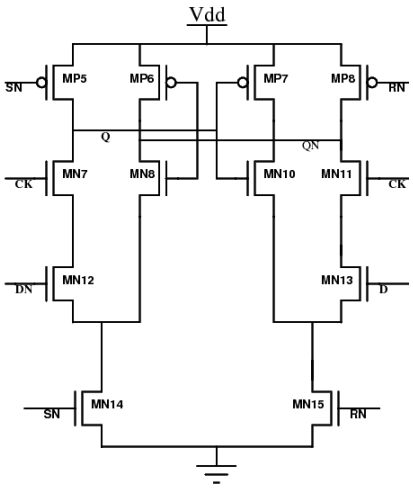


Fig. 3. Strollo's SAFF latch circuit

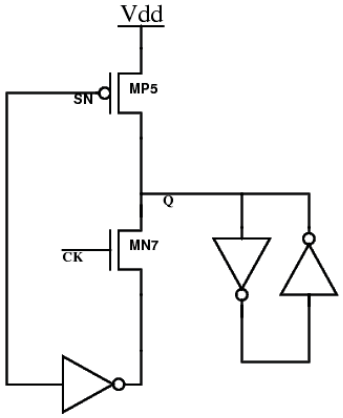


Fig. 4. Lin's SAFF latch circuit

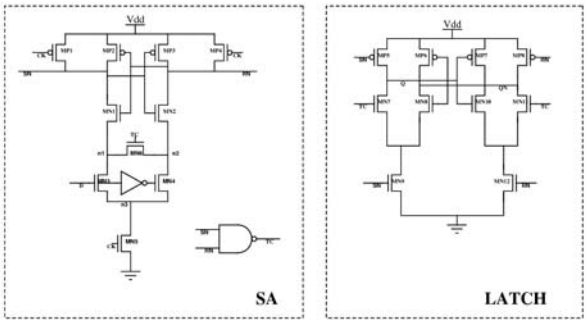


Fig. 5. Jeong's SAFF circuit

output SN and RN, respectively. When D is logic high and CK is high, the SN can only be discharged using MN3. The RN is automatically discharged as soon as the DN and clock become high state for their next cycle. Since the precharging

activity is controlled conditionally, the critical path for the pull-down of SN and RN is simplified, consisting of only one signal transistor. This helps reduce discharge time. Due to this, the resulting sensing stage exhibits features of low-power and high-speed.

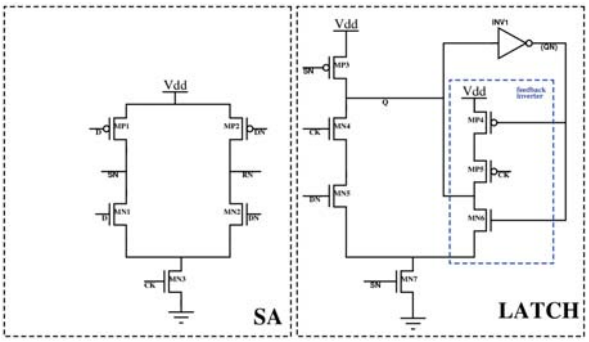


Fig. 6. Proposed SAFF circuit

The proposed SAFF includes a redesigned single-ended latch. Fast and energy-efficient operation can be achieved by combining Strollo's and Lin's latches. The latch depicted in Figure 6 uses a similar first stage to Strollo's latch to ensure glitch-free performance. The error in Lin's latch exhibited in Figure 7 has been completely removed, as demonstrated in Figure 8. This is mainly due to the insertion of MN4. When D is high, DN is low, and MN5 completely blocks the pull-down path. As a result, the issue has been fixed. As a result of the current dispute, the two inverters that store data have been modified. MN7 disables the feedback inverter when output Q changes from low to high, indicating that SN voltage is low. Additionally, MP5 is turned off for the transition from high to low output Q. Thus, the feedback inverter's influence on the output transition is fully erased. The RN generation in the SA stage could use smaller transistors because the latch has nothing to do with it, allowing for less overall power consumption in the SA stage. To create a complementary output QN, the latch's 1 inverter INV1 can be used, and the delay between the two outputs is the same as MSFF, an inverter delay.

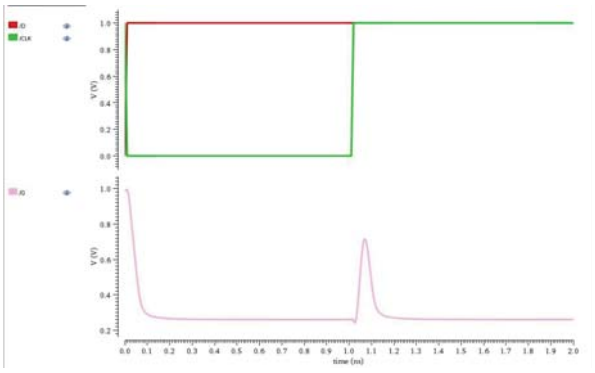


Fig. 7. Glitches in Lin's SAFF

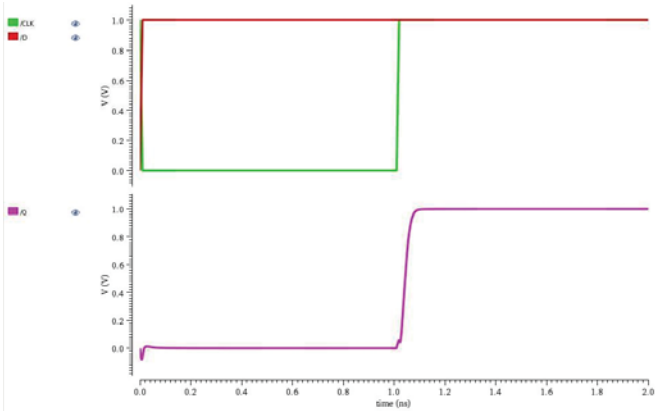


Fig. 8. Glitch-free operation in the proposed SAFF

IV. Simulation Results and Discussion

A. Pre-Layout Simulation Results

For the purpose of comparing their performance, all flip-flops were tested with a 500 MHz clock signal and a 1 V power supply voltage. The output connection provides a load capacitance of 3 fF, which can be used to check the design's capability. When a circuit is capable of withstanding a specific degree of strain, it is critical to understand what the device's output will be.

High-to-low transition: The information that's been provided While CK rises, D completes high-to-low conversion; at the same time, DN is the inverse of D and completes low-to-high conversion. D and DN are used as input values for SN and RN, which are pre-charged during the negative half cycle of CK. When the clock and the DN are in a high state, the RN will shift its condition from high to low. The output Q is discharged to low through MN3, MN4, and MN6 while the SN remains high. MP5 controls the feedback inverter until QN has completed low-to-high conversion (Q finishes high-to-low conversion). It is possible for the feedback inverter to keep Q low after the QN turns high because of MN6 and MN7 Figure 9 illustrates the high-to-low and low-to-high procedures.

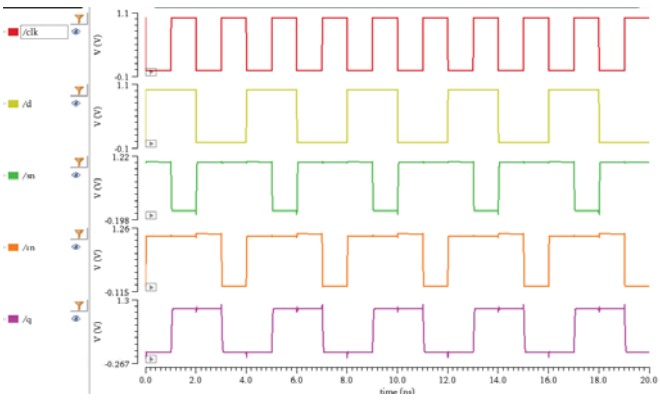


Fig. 9. Transient waveform of the proposed SAFF

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Low-to-high transition: The information that's been provided D converts from low to high before CK's rising edge, and DN converts from high to low. Pre-charging of SN and RN occurs during the negative half cycle of CK and is predicated on D and DN input value. When both the clock and D are high, the SN will go from high to low. Then the Q is charged through MP3 to an even higher level. Contention-free functioning is possible due to the fact that MN6 is disabled when SN is low. Maintaining output Q during the half-cycle of CK is done by MP3. During the CK's negative cycle, SN is pre-charged to high levels and MP3 is turned off, allowing MP4 and MP5 to maintain output Q.

Flip-flop input data toggling rates at a typical corner clock frequency of 500 MHz were applied to these flip-flops in order to study power consumption. The proposed SAFF has a significant power benefit over earlier SAFFs at all toggling rates, as demonstrated in figure 10 when the SA stage and single-ended latch are utilized. Nikolic's SAFF and Jeong's SAFF have far more power than the conventional SAFF. To put it another way, Nikolic's SAFF and Jeong's SAFF each had logic (inverters) that flips at a clock frequency. After the glitch, the ongoing controversy over SAFF power use has affected Lin's SAFF's power consumption. Even though Lin's SAFF has a single-ended latch, it has more power than the conventional SAFF. Pre-charge logic is not included in the proposed SAFF design (SN and RN). The previous slave latch's glitch and present contention have been fixed. Because of this, the SA stage's pre-charge power is significantly reduced. It's because of this large power consumption advantage that the suggested SAFF can attain.

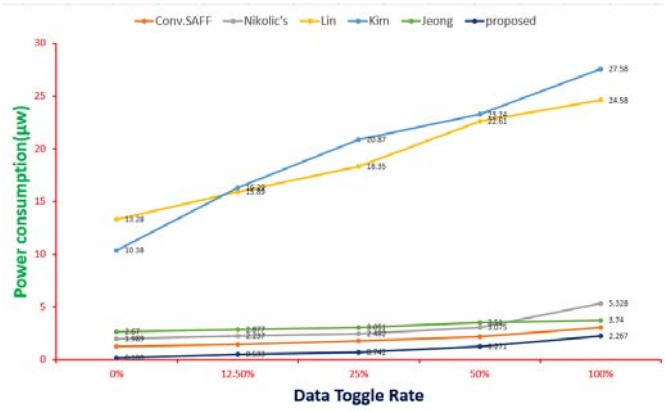


Fig. 10. power consumption (µW) at different input data toggle rates at the speed of 500 MHZ.

Figure 11 depicts the flip-flops' CK-to-Q delay. The CK-to-Q delay of the SAFF is the lowest among all flip-flops in the PVT corners. The fundamental cause for this is that the signal moves from the SA stage to the output Q with little logic. At the rising edge of CK, the SA stage can also more quickly collect data input. SAFF's delay is large since it relies on Q and QN in the SR latch. Although the dependency of Q and QN in the conventional SAFF has been eliminated, Nikolic's SAFF and Jeong's SAFF have a slightly larger delay than the conventional SAFF. The complexity of the latches is mainly responsible for the increase in delay. Due to the shorter distances between CK and Q, all SAFFs show speed advantages.

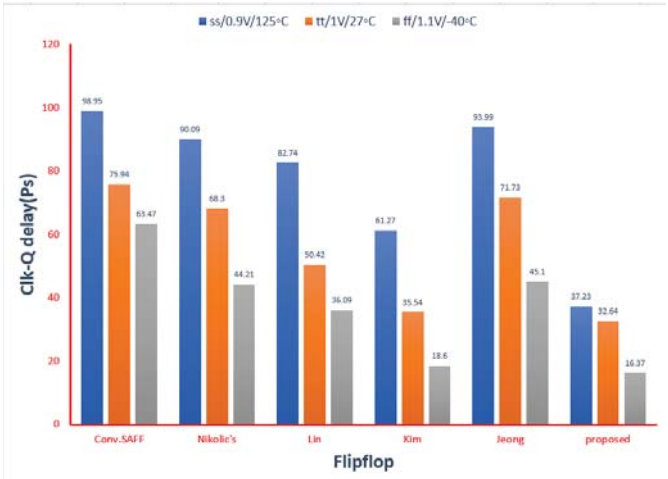


Fig. 11. CK-to-Q delay (ps) of the flip-flops across PVT corners

Figure 12. depicts the proposed SAFF's CK-to-Q delay evaluation as well as the Jeong SAFF and conventional SAFF. With a supply voltage range of 0.4V to 1.4V, the proposed SAFF has a delay advantage over the Jeong SAFF and the conventional SAFF. With 1.4V of supply voltage, there was a slight increase in delay.

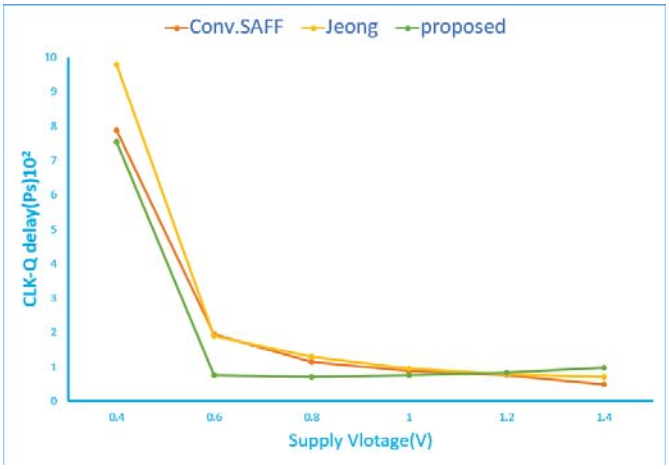


Fig. 12. CK-to-Q delay of the proposed flip-flop's at different supply voltages ranging from 0.4 V to 1.4 V

Flip-flops are evaluated using the power-delay-product (PDP) as a comprehensive performance index.Figure 13 depicts the normalized PDP under various input data toggle rates.The proposed SAFF has the lowest PDP under each toggle rate because of its smaller delay and power consumption than other flip-flops.

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Fig. 13. PDP at different Data Toggle Rate

B. Post-Layout simulation results

pre and Post layout simulation results for our proposed flipflop were compared in this section.

According to the following equations, the normalized power and normalized delay are determined.

$$NormalizedPower = Power/VDD^2. \quad (1)$$

$$NormalizedDelay = Delay/Process^2. \quad (2)$$

TABLE I
COMPARISION OF PRE AND POST LAYOUT SIMULATION RESULTS FOR OUR PROPOSED FLIPFLOP

tt/1V	Pre-layout	post-Layout
Frequency(MHz)	500	
Power(µW)	2.67	2.91
delay(Ps)	32.64	65.82
PDP(pJ)	87.14	191.53
Normalized Power	2.67	2.91
Normalized Delay	0.402	0.812

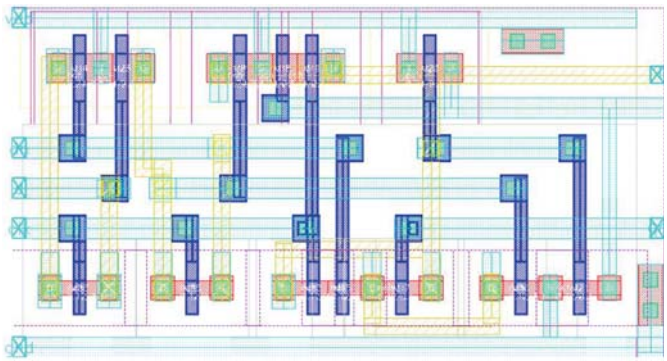


Fig. 14. Layout of the proposed flip-flop

V. CONCLUSION

This paper proposes a low-power, high-speed SAFF. A new design for the SA stage has been proposed in an effort to reduce the SAFF's pre-charge power.. There's also talk of a single-ended latch that's free of glitches and contention. The SAFF's delay and power are greatly improved with the use of the single-ended latch and the new SA stage. To reduce latency, the design outperforms earlier flip-flops because of the loading effect. The power consumption was 2.91µW and the delay was 65.82 ps, respectively, according to the results. In cadence virtuoso, all circuits were designed with the same input conditions. Because there are fewer components in the circuit, it is less expensive and takes up less space.

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