World Academy of Science, Engineering and Technology
International Journal of Electrical and Computer Engineering
Vol:14, No:11, 2020

Design and Characterization of a CMOS Process Sensor Utilizing V_{th} Extractor Circuit

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***Abstract*—**This paper presents the design and characterization of a low power Complementary Metal Oxide Semiconductor (CMOS) process sensor. The design is targeted for implementation using Silterra's 180 nm CMOS process technology. The proposed process sensor employs a voltage threshold (V_{th}) extractor architecture for detection of variations in the fabrication process. The process sensor generates output voltages in the range of 401 mV (fast-fast corner) to 443 mV (slow-slow corner) at nominal condition. The power dissipation for this process sensor is 6.3 µW with a supply voltage of 1.8V with a silicon area of 190 µm X 60 µm. The preliminary result of this process sensor that was fabricated indicates a close resemblance between test and simulated results.

***Keywords*—**CMOS Process sensor, Process, Voltage and Temperature (PVT) sensor, threshold extractor circuit, V_{th} extractor circuit.

I. Introduction

OVER the past few decades, silicon integrated circuit (IC) technology has evolved rapidly. This evolution allows more complex circuits consisting of millions of transistors, diodes, resistors, and capacitors to be integrated into a chip. Integration also provided other benefits such as batch manufacturing, where thousands of ICs were fabricated onto a single semiconductor wafer.

In spite of the manufacturing benefits, process variation during the manufacturing process can have an impact on the electrical parameters of the IC, thereby leading to variations in its performance. This process variation may cause greater yield degradation, increased cost, and longer time to market. Accurately knowing the process corner can help chip designers understand and improve chip behavior, therefore, any work that is related to this topic is essential. There are many methods reported for the detection of process variation. Some of them are presented and discussed thoroughly in these reference papers [1]-[5].

In this paper, the implementation of a low power and low complexity CMOS process sensor is presented. This paper is divided into three additional sections. The circuit and physical layout implementation are described in Section II. Section III analyses the simulation and measurement results. Finally, the conclusions are drawn in Section IV.

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II. Design Implementation

In this work, we propose a voltage threshold (V_{th}) extractor architecture for the detection of CMOS process variation. The V_{th} extractor is a circuit that automatically extracts the threshold voltage of the MOSFET transistor and uses this value as its output voltage. The Vth is one of the key device parameters in CMOS technology and is very sensitive to process variation. For simplicity, we use the saturation current equation for a MOSFET as shown in (1). It is sufficient to illustrate the impact of the main variation sources on key transistor parameters.

$$I_D \approx \frac{W}{L}\mu C_{OX}(V_{GS} - V_t)^2 \quad (1)$$

Table I shows the MOSFET parameters and relevant process steps that directly influence each of those parameters.

TABLE I
MOSFET Parameters and Their Relevant Process Steps

Device Parameter	Relevant Process Step
Threshold Voltage (Vth)	Ion implantation, gate oxidation, annealing, etching, lithography
Carrier Mobility (µ)	Ion implantation, diffusion annealing and stress
Gate Oxide Capacitance (Cox)	Gate oxide formation
Transistor Dimension (W, L)	Etching and lithography

A. Circuit Implementation

The implemented circuit topology for Vth extractor is shown in Fig. 1. It consists of three parts: self-bias circuit, differential amplifier and power down circuit. The devices sizes are shown in Table II. This architecture was first proposed by [6] and was improved and simplified by [7].

TABLE II
Device Parameters

Device	W/L (µm)	Multiplier,m
MP1	3/40	2
MN1	6/36	8
MP2,MP3	6/12	2
MN2,MN5,MN6	6/36	1
MN3,MN4	6/36	2

When EN signal is high (connected to positive power supply VDDA), transistors MP1 and MN1 provide a bias voltage V1 to the gate transistor of MN2. The voltage V1 also applied to the terminal of a differential amplifier, which is the gate of transistor MN6. Transistors MN2, MP2, MP3, MN3 and MN4 generate voltage V2 and it is applied to another terminal of a differential amplifier, the gate of transistor MN5.

MN5 and MN6 are set to be identical in terms of transistor dimensions.

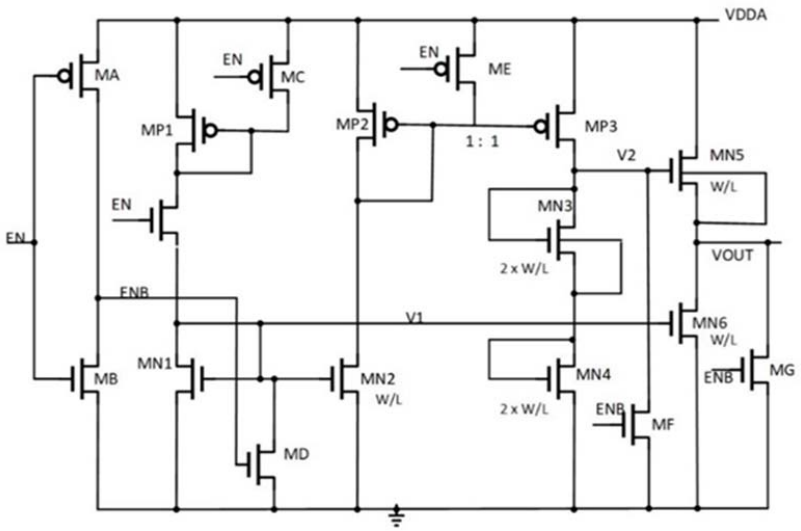

Fig. 1 Circuit of Vth Extractor as CMOS process sensor

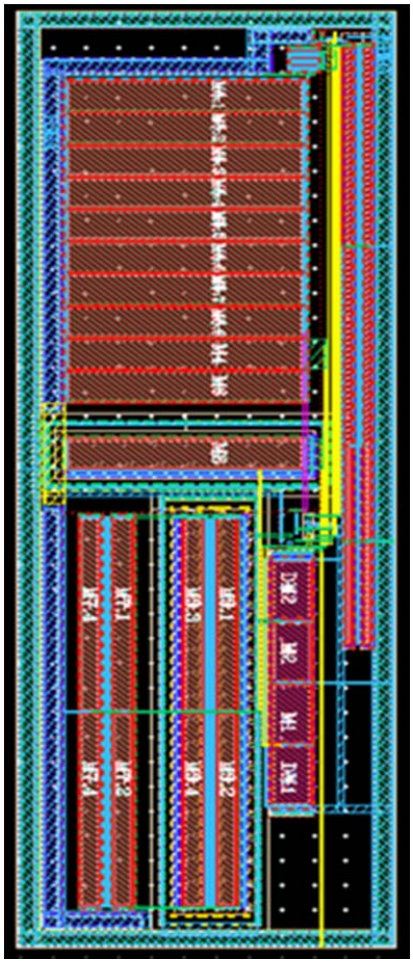

Fig. 2 (a) Physical layout of V_{th} extractor circuit

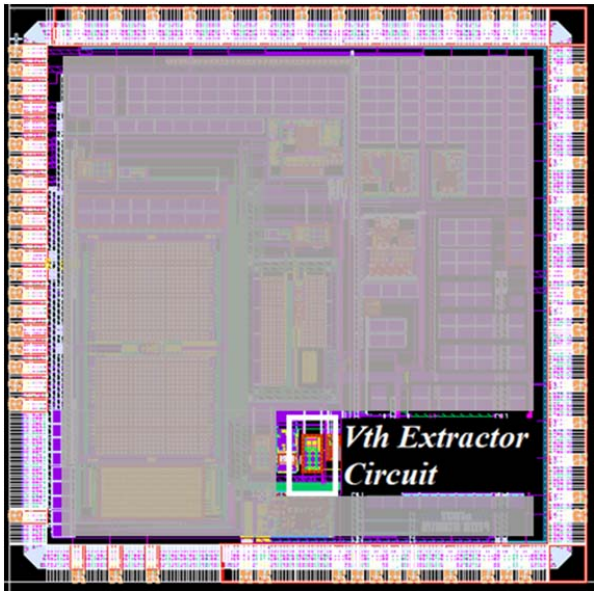

Fig. 2 (b) Placement of V_{th} extractor circuit in the test chip

By assuming both transistors are in the saturation region, the VGS for these transistors can be simplified as

$$V_{GS(MN5)} = V2 - V_{OUT} \quad (2)$$

$$V_{GS(MN6)} = V1 \quad (3)$$

Since the drain current, $I_{D,}$ for both transistors MN5 and MN6 are similar, they must also have similar V_{GS}. Therefore, from (2) and (3):

$$V_{OUT} = V2 - V1 \quad (4)$$

Quoting from [7],

$$V_{OUT} = V_{th(MN6)} \quad (5)$$

V1 needs to be maintained small, $V1 < 2V_{th}$ to ensure the transistor of MN6 is always in the saturation region. To achieve this, the sizing (W/L) of MN2 is designed to be large, while (W/L) MP1 is small. Transistors MN3 and MN4 are implemented using separated wells because of the body-bulk connection. Transistors MA, MB, MC, MD, ME, MF, and MG were added to power down the circuit.

B. Physical Layout Implementation

To better match transistors, a layout technique called common centroid was used. Common-centroid layout is the act of evenly spacing devices that are interdigitated and have the same central point. Using this technique, sheet resistant variation as a function of the devices position is minimized thus making the devices more closely matched. These devices were placed as close together as design rules would allow minimizing sheet resistant gradients. Guard rings were also used generously around all devices to minimize cross coupling noise. The complete physical layout for this V_{th} extractor circuit is shown in Fig. 2 (a). It occupies 190 µm x60 µm silicon area without I/O pads. Fig. 2 (b) shows the location of the V_{th} extractor circuit inside the test-chip.

III. Results and Analysis

A. Simulation Results

The Vth extractor circuit was simulated using the BSIM3V3 model for Silterra 180 nm CMOS process. For accurate simulation, all parasitic resistance and capacitance that were extracted from the top layout of the test-chip need to be included. Wire bond package information was also added. Fig. 3 illustrates the simulation setup for this circuit. Wire bond model includes the 697 mΩ series resistor, 2 nH inductor and 235 fF capacitor. The output load capacitor is set to 25 pF to model the oscilloscope probe loading.

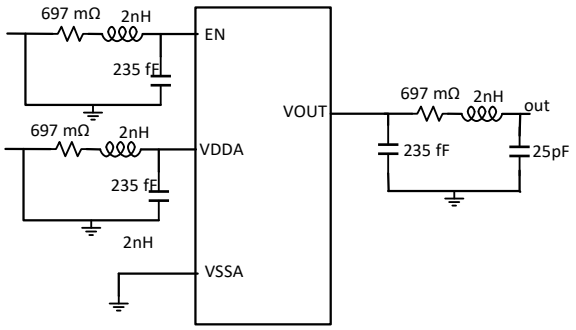

Fig. 3 Simulation configuration for V_{th} extractor circuit

Table III shows the simulation results for the output voltage of the V_{th} extractor circuit at three different corners; fast-fast (*ff*), typical-typical (*tt*) and slow-slow (*ss*). Another two corners fast-slow (*fs*) and slow-fast (*sf*) are excluded since this circuit only extracts the threshold voltage of NMOS-type transistors. The V_{OUT} for these *fs* and *sf* corners should be close to *ff* and *ss* corners, respectively. Table III shows close comparison between the threshold voltages of the NMOS transistor that were extracted from the model parameters. The difference between these two values is about 0.5% (for three different corners).

TABLE III
VTH FROM MODEL PARAMETER VS. GENERATED VOUT OF VTH EXTRACTOR CIRCUIT

Process	Model (V)	Simulated Vout(V)
ff	0.396	0.401
tt	0.421	0.423
ss	0.445	0.443

Monte Carlo simulations were used to determine the process and transistor mismatch effects on the V_{th} extractor circuit output voltage. This analysis was performed for all process corners with three different supply voltages and at three temperature conditions; cold (-40 °C), room (27 °C) and hot (125 °C). Fig. 4 shows the Monte Carlo simulation results for typical conditions with output voltage variation by ~6 mV ($\pm 3\,\sigma$) across 500 runs. The mean value for V_{OUT} is 0.423 V. Table IV summarizes the results obtained for V_{OUT} for all MOSFET corners; fast-fast (*ff*), typical-typical (*tt*) and slow-slow (*ss*). The output voltage is unique for each process corner and does not overlap with other corners, thus this circuit can be used to detect the test chip process corner.

TABLE IV
EXTRACTED LAYOUT SIMULATION RESULTS FOR VTH EXTRACTOR

Process	Mean (V)	3σ Min (V)	3σ Max (V)
ff	0.401	0.399	0.405
tt	0.423	0.420	0.426
ss	0.443	0.441	0.446

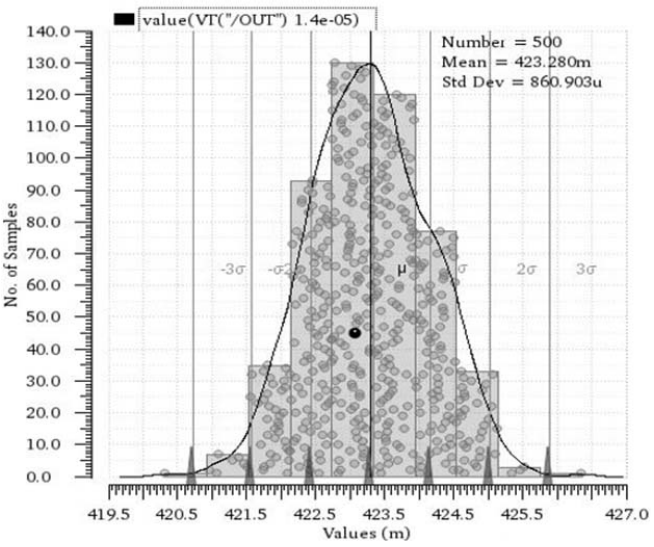

Fig. 4 Monte Carlo simulation result at typical condition

B. Measurement Results

The test-chip has been fabricated under Silterra's MPW program and packaged in a 56 pin QFN. A test board has been developed to characterize all the IPs in this test chip, including the V_{th} extractor circuit. Using a temperature chamber to test

the circuit, the output voltages of the V_{th} extractor circuit were measured from all ten packaged chips in 10 °C increments from -40 °C to 90 °C. These measurement results were compared with Table III to identify which process corner the chips belong to. The comparison between measurement and simulation results was tabulated in Figs. 5 (a)-(c). The gray area represents the output voltage range for the specific process corners. These three graphs show that six out of 10 tested chips lie on the *tt* process corner while the rest belongs on the *ss* process corner. This result correlates with measurement result of another IP (ring oscillator) that was designed and fabricated together in this test-chip. As can be seen from Table V, the measurement results of the ring oscillator is further proof that chip number 1, 2, 3, 5, 6 and 7 belong to the *tt* process corner, while chip number 4, 8, 9 and 10 belong to the *ss* corner.

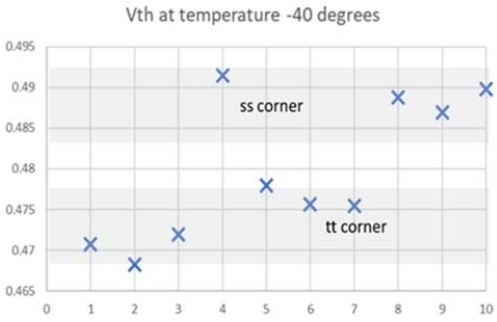

Fig. 5 (a) Vout of Vth extracted circuit for 10 chips at cold temperature

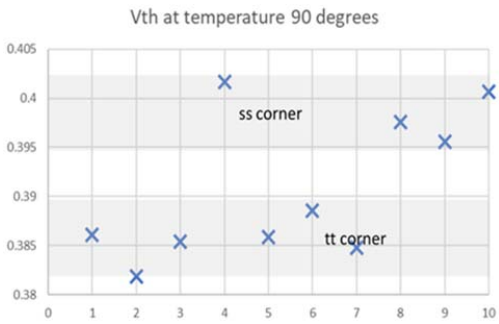

Fig. 5 (b) Vout of Vth extracted circuit for 10 chips at hot temperature

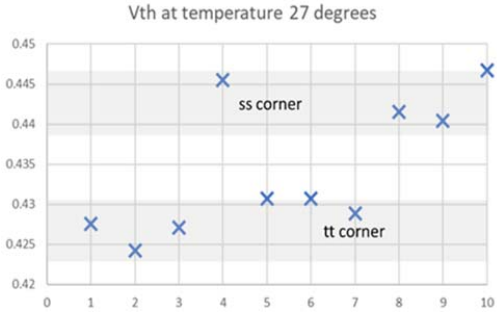

Fig. 5 (c) Vout of Vth extracted circuit for 10 chips at room temperature

TABLE V
RING OSCILLATOR MEASUREMENT RESULTS

Chip Number	Measurement (MHz)	Process Corner
1	21.18	tt
2	21.13	tt
3	21.15	tt
4	20.92	ss
5	21.12	tt
6	21.11	tt
7	21.16	tt
8	20.99	ss
9	21.07	ss
10	21.09	ss

Fig. 6 illustrates the comparison between simulated and measured output voltage for 10 chips of the V_{th} extractor circuit across a temperatures range of -40 °C to 90 °C. It shows that the average temperature coefficient for both simulated and measured results are close to -0.7 mV/°C. Fig. 7 plots the simulated and measured output voltages using three different supply voltages 1.62 V, 1.8 V, and 1.98 V.

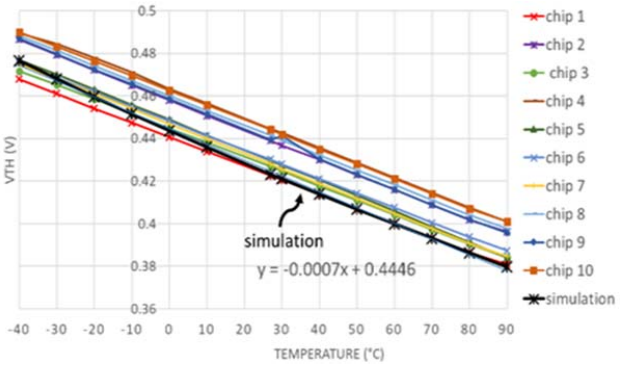

Fig. 6 Vth distribution across temperature at nominal condition

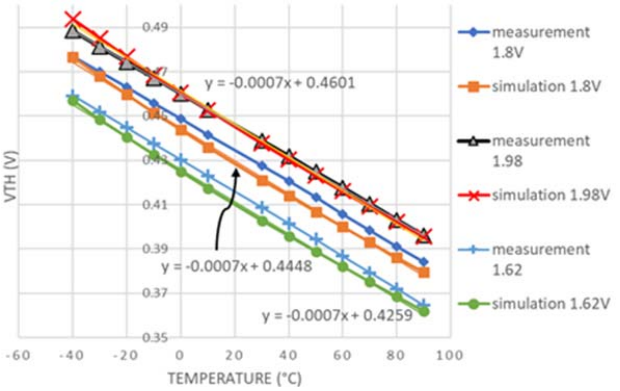

Fig. 7 Temperature coefficient for one chip at different supply voltages

IV. CONCLUSION

The design and characterization of a CMOS process sensor utilizing the V_{th} extracted circuit has been presented in this paper. The V_{th} extracted circuit has been implemented using Silterra's 180 nm CMOS process technology with 10 chips tested. The tested circuit produced an output voltage in the

range of 401 mV to 443 mV and drew a current of 3.5 µA with 1.8 V supply voltage. The power consumption for this circuit is 6.3 µW. Measurement results across a temperature range of -40 °C to 90 °C confirm the simulated temperature coefficient of -0.7 mV/°C and we were able to successfully predict the process corner of the 10 chips tested. The silicon area size for the designed V_{th} extractor is 190 µm X 60 µm.

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