

Optimizing the Performance of Thermoelectric for Cooling Computer Chips Using Different Types of Electrical Pulses

Saleh Alshehri

Abstract—Thermoelectric technology is currently being used in many industrial applications for cooling, heating and generating electricity. This research mainly focuses on using thermoelectric to cool down high-speed computer chips at different operating conditions. A previously developed and validated three-dimensional model for optimizing and assessing the performance of cascaded thermoelectric and non-cascaded thermoelectric is used in this study to investigate the possibility of decreasing the hotspot temperature of computer chip. Additionally, a test assembly is built and tested at steady-state and transient conditions. The obtained optimum thermoelectric current at steady-state condition is used to conduct a number of pulsed tests (i.e. transient tests) with different shapes to cool the computer chips hotspots. The results of the steady-state tests showed that at hotspot heat rate of 15.58 W (5.97 W/cm²), using thermoelectric current of 4.5 A has resulted in decreasing the hotspot temperature at open circuit condition (89.3 °C) by 50.1 °C. Maximum and minimum hotspot temperatures have been affected by ON and OFF duration of the electrical current pulse. Maximum hotspot temperature was resulted by longer OFF pulse period. In addition, longer ON pulse period has generated the minimum hotspot temperature.

Keywords—Thermoelectric generator, thermoelectric cooler, chip hotspots, electronic cooling.

I. INTRODUCTION

THE thermoelectric technology is currently being used in many industrial and medical applications. One of these applications is to generate electricity from different sources of thermal energy for both space and terrestrial applications (see Fig. 1 (a)). Fig. 1 (b) shows another type of thermoelectric application in which thermoelectric unicouple is used to convert electrical power to thermal energy for both cooling (the case of thermoelectric coolers) and heating (the case of thermoelectric heat pumps). Examples of products using thermoelectric coolers include CCD (charge coupled device) cameras, laser diodes, microprocessors, blood analyzers and portable picnic coolers.

The focus of this research study is continuation of a previous effort in which the thermoelectric devices are used in cooling hotspots of high-speed computer chips. Thermoelectric coolers are based on the Peltier Effect, discovered in 1834, by which applied DC electrical current across two dissimilar materials creates a temperature difference [1].

Saleh Alshehri is with the Jubail University College, Saudi Arabia (e-mail: shehri@ucj.edu.sa).

A typical thermoelectric module is manufactured using two thin ceramic wafers with a series of Positive (P) and Negative (N) doped semiconductor material (e.g. P- and N-Bismuth-Telluride, P- and N-Silicon-Germanium, etc.) sandwiched between them. The ceramic material is attached on both sides. It acts as electrical insulation and gives rigidity to the assembly. One P-type and one N-type make up a unicouple as shown in Figs. 1 (a) and (b). The thermoelectric unicouples are electrically in series and thermally in parallel.

The Very-Large-Scale Integration (VLSI) is the process of integrating millions of transistors into a single silicon chip. Currently, 1000 million transistors can be built in an area less than 1 mm². One of the main challenges in chip design is that the local heat generation is not uniform which forms what is called hotspots. Modern chips can generate a heat flux of more than 100 W/cm² while local heat fluxes of the hotspots can be over 1000 W/cm² [1].

For IC thermal managements, many active and passive cooling systems are currently being used [2]-[4]. Among these systems are heat sink air cooling, two-phase heat pipes, microchannel liquid heat removal and thermoelectric [5]-[9]. Each of these cooling systems has advantages and disadvantages. Thermoelectric devices are promising technology towards effective electronic cooling. There have been many attempts to use thermoelectric to cool electronic devices with various types of heat sinks [10]-[15]. Cooling systems could be in microscale and macroscale [16]-[19]. Hotspots cooling is a major challenge [20]-[22].

The main objectives of this study are to:

- (1) Use the previously developed and validated three-dimensional thermoelectric model [23]-[25] to investigate the effect of using pulsed technique for reducing the temperature of computer hotspot below the optimum value at steady-state condition.
- (2) Conduct steady-state testing using a commercially available thermoelectric module for cooling hotspot.
- (3) Use the optimum thermoelectric current obtained in (2), to conduct transient tests with pulses having different shapes for cooling hotspot.

This research represents phase – I for pulsed thermoelectric cooling. In this phase, experimental tests are conducted to investigate the effect of the key parameters for maximizing the thermal performance of the pulsed thermoelectric cooling. A commercially available thermoelectric module is used in these experimental tests. Fig. 2 shows an example of Pulsed Thermoelectric Cooling for computer chip with background

heat flux of 40 W/cm^2 and hotspot heat flux of 1000 W/cm^2 .

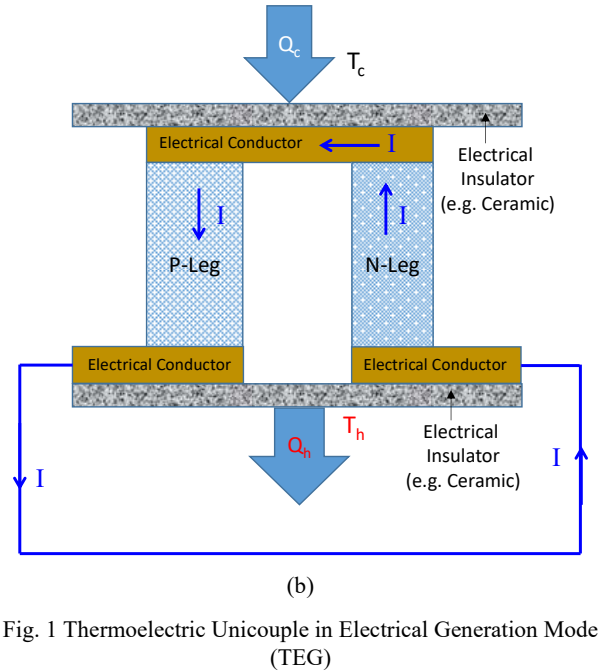
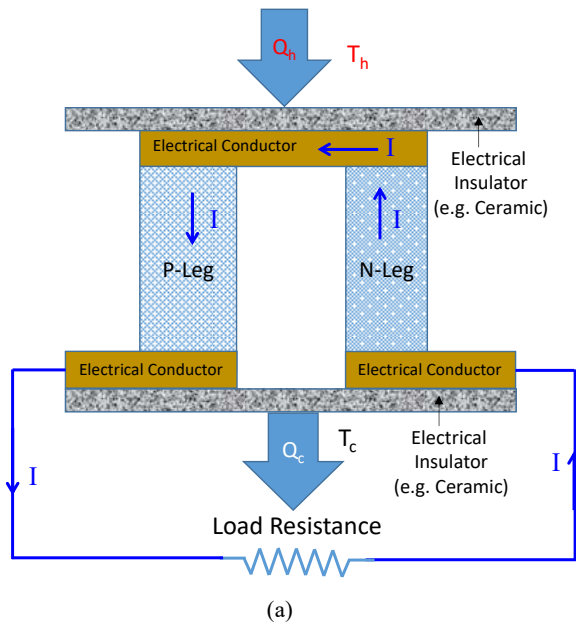


Fig. 1 Thermoelectric Unicumple in Electrical Generation Mode (TEG)

Chip heat dissipation rate per TEM = 24.367 W , $q''_{\text{NHS}} = 40 \text{ W/cm}^2$, $q''_{\text{HS}} = 1000 \text{ W/cm}^2$,
 heat sink surface temperature = 85°C , $I_{\text{opt}} @ \text{ss} = 2.416 \text{ A}$

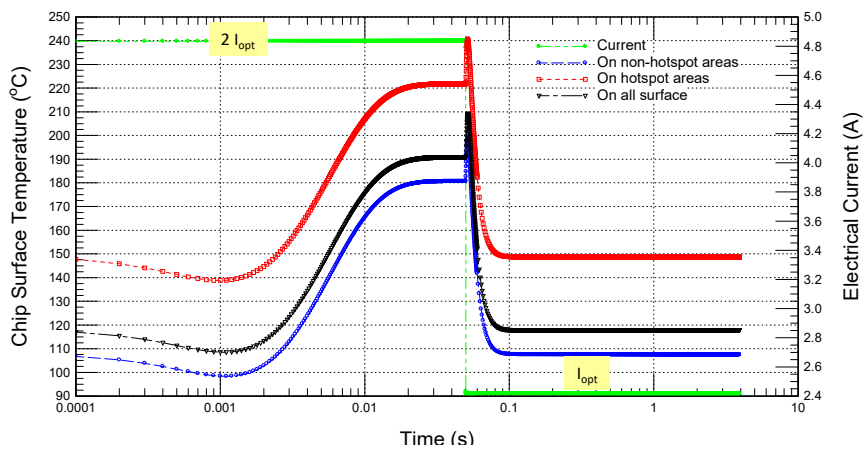


Fig. 2 Example of Pulsed Thermoelectric Cooling for computer chip with background heat flux of 40 W/cm^2 and hotspot heat flux of 1000 W/cm^2

II. EXPERIMENTAL TESTS

Initially the experimental tests were conducted in the study at steady-state condition as in [23]. A few setup parameters were slightly changed because of the environment control. Two tests were conducted, namely: (I) steady-state tests, and (II) transient tests with pulsed electrical power. The main setup components are shown in Fig. 3. The obtained test results are discussed next.

A. Results of Steady-State Condition

As indicated earlier, an individual power supply was used to power each test component. The test parameters for the different power supplies include the following:

- The power supply connected to the patch (background) heater: Voltage = 8.49 V , Current = 0.41 A (3.48 W).

- The power supply connected to the ceramic (hotspot) heater: Voltage = 7.18 V , Current = 2.17 A (15.58 W).
- The power supply connected to the mechanical fan: Voltage = 9.6 V , Current = 0.23 A (2.3 W).

For the power supply that is connected to the thermoelectric module, the electrical current was gradually increased from 0 A (open circuit condition) to 8.0 A with an incremental step of 0.5 A . In each current step, the collected data were carefully monitored until the steady-state condition was achieved in which the change of the temperatures with time was less than $\pm 0.2^\circ\text{C}$. The result is shown in Fig. 4.

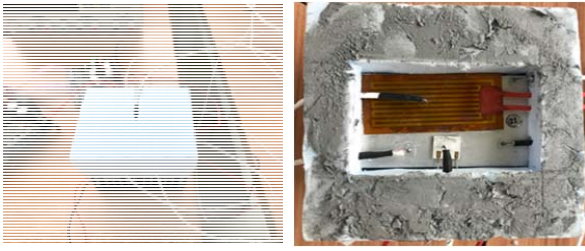


Fig. 3 Main components of the experimental setup

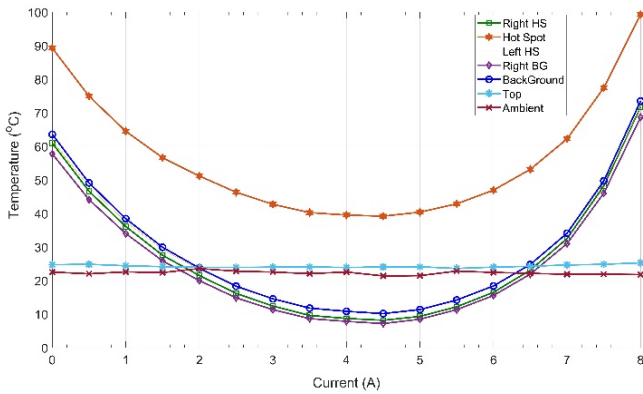


Fig. 4 Effect of thermoelectric current on the temperatures at different locations for the case of hotspot heat rate (QHS) of 15.58 W and background heat rate (QBG) of 3.48 W

B. Transient Mode

Similar experimental setup for steady-state tests was used to conduct experimental tests in the transient mode. As indicated earlier for the steady-state tests, the optimum thermoelectric current for obtaining the lowest hotspot temperature was 4.5 A. This optimum current was used to conduct three different shapes of pulsed thermoelectric cooling for computer chip with background heat flux of 0.73 W/cm^2 (3.48 W) and hotspot heat flux of 5.97 W/cm^2 (15.58 W). In each pulsed test, the thermoelectric current was set to 0 for a period of time called in this study “OFF”. The OFF period was followed by another period called “ON” in which the thermoelectric current was set to be the same as the optimum thermoelectric current at steady-state condition (i.e. 4.5 A). Each pulsed thermoelectric current was repeated several times so as to determine the number of pulses that are needed to obtain the minimum hotspot temperature.

1) First Pulsed Test

The shape of the pulse in the first test is “15 s OFF and 15 s ON at 4.5 A”. By applying this pulse, the obtained time dependent temperatures at different locations are shown in Fig. 5.

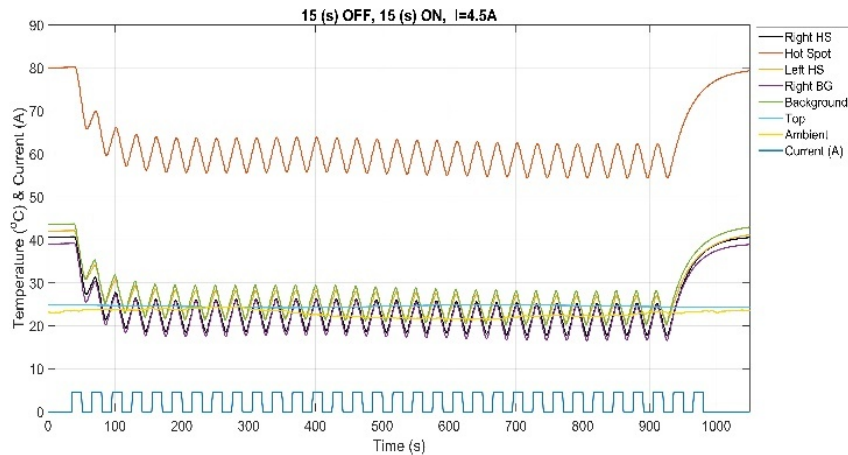


Fig. 5 Effect of the pulsed thermoelectric current of 15 s OFF and 15 s ON at 4.5 A on the temperatures at different locations for the case of hotspot heat rate (QHS) of 15.58 W and background heat rate (QBG) of 3.48 W

2) Second Pulsed Test

The shape of the pulse in the second test is “30 s OFF and 30 s ON at 4.5 A”. By applying this pulse, the obtained time dependent temperatures at different locations are shown in Fig. 6.

3) Third Pulsed Test

The shape of the pulse in the third test is “15 s OFF and 45 s ON at 4.5 A”. By applying this pulse, the obtained time dependent temperatures at different locations are shown in Fig. 7. Fig. 8 shows a comparison of the three different pulses.

III. SUMMARY AND CONCLUSION

This study was conducted to investigate the potential of thermoelectric technology in cooling hotspots at different conditions. In the first part of this study, the previously developed and validated three-dimensional model for cascaded thermoelectric and non-cascaded thermoelectric [23]-[25] was used to conduct numerical simulations for a specified pulsed shape. The obtained results are provided in Fig. 4. The obtained numerical results showed that the hotspot temperature of computer chip can be further decreased below that at steady-state condition by using the pulsed technique.

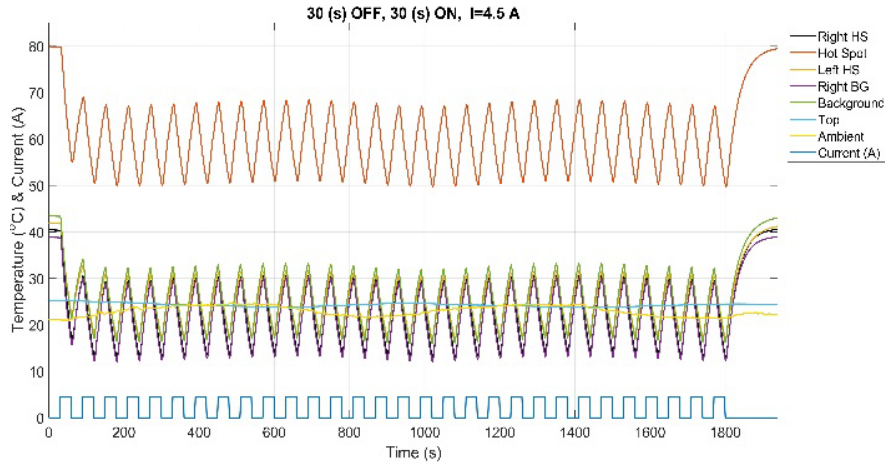


Fig. 6 Effect of the pulsed thermoelectric current of 30 s OFF and 30 s ON at 4.5 A on the temperatures at different locations for the case of hotspot heat rate of (QHS) of 15.58 W and background heat rate (QBG) of 3.48 W

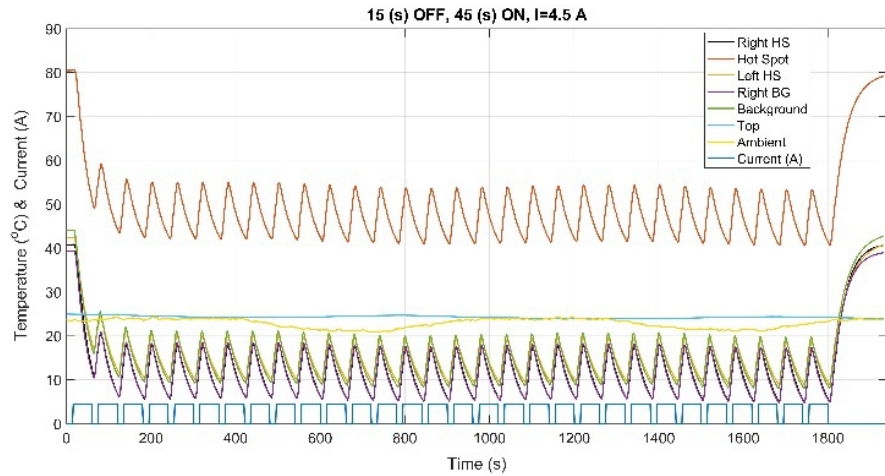


Fig. 7 Effect of the pulsed thermoelectric current of 15 s OFF and 45 s ON at 4.5 A on the temperatures at different locations for the case of hotspot heat rate of (QHS) of 15.58 W and background heat rate (QBG) of 3.48 W

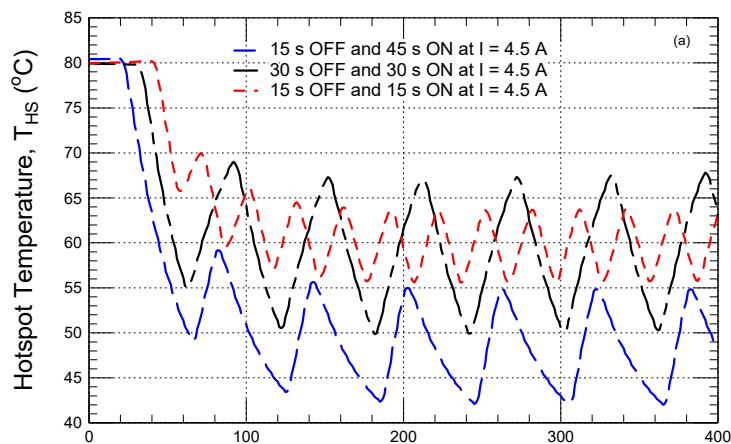


Fig. 8 Comparison of the hotspot temperature of different pulsed shapes for the case of hotspot heat rate of (QHS) of 15.58 W and background heat rate (QBG) of 3.48 W

In the second part of this study, experimental tests were conducted at steady-state condition (background heat flux of 0.73 W/cm^2 and a hotspot heat flux of 5.97 W/cm^2), in which

an aluminum sheet was used to mimic the computer chip, and heated by ceramic heater to provide hotspot heat rate at 15.58 W and a patch heater to provide the background heat rate at

3.48 W. A commercial thermoelectric module attached to heat sink and mechanical fan was used to cool down the aluminum sheet at different thermoelectric currents. Results showed that at the open circuit condition, the hotspot temperature was 89.3 °C. As well, at the lowest hotspot temperature (39.2 °C) was obtained at thermoelectric current of 4.5 A. This represents a reduction of the hotspot temperature by 50.1 °C as a result of operating the thermoelectric module at the optimum current condition (i.e. at 4.5 A). The hotspot temperature at the optimum condition is 44% of that at the open circuit condition.

In the third part of this study, three pulsed tests having different shapes were conducted to investigate the effect of pulsed technique for cooling hotspot at specified heat rate. The same experimental setup of the steady-state tests was used to conduct the pulsed tests. The results showed that both durations of the OFF period (i.e. zero thermoelectric current) and ON period (i.e. with specified thermoelectric current, which is 4.5 A in this study) have affected not only the minimum hotspot temperature, but also the maximum hotspot temperature. As well, the pulsed shape with longest OFF duration has resulted in the highest maximum hotspot temperature. Additionally, the pulsed shape with longest ON duration has resulted in the lowest minimum hotspot temperature. Last but not the least, the number of pulses needed to obtain the minimum hotspot temperature depended on the shape of the pulse.

ACKNOWLEDGMENT

The financial contributions from Jubail University College are greatly appreciated.

REFERENCES

- [1] ITRS, International Technology Roadmap for Semiconductors, 2004.
- [2] R. Viswanath, W. Vijay, A. Watweand V. Lebonheur, "Thermal performance challenges from silicon to systems," *Intel Technol. J.*, 4 (3), pp. 1–16, 2000.
- [3] B. Goplen and S. S. Sapatnekar, "Placement of thermal vias in 3D ICs using various thermal objectives," *IEEE Trans. Comput. Aided Design Integ. Circuits Syst.*, 26 (4), pp. 692–709, 2006.
- [4] H. F. Hamann, A. Weger, J. A. Lacey, Z. Hu, P. Bose, E. Cohen and J. Wakil, "Hotspot limited microprocessors: Direct temperature and power distribution measurements," *IEEE J. Solid-State Circuits*, 42 (1), pp. 56–65, 2007.
- [5] I. Chowdhury, R. Prasher, K. Lofgreen, G. Chrysler, S. Narasimhan, R. Mahajan, D. Koester, R. Alley and R. Venkatasubramanian, "On-chip cooling by superlattice-based thin-film thermoelectrics," *Nature Nanotechnol.*, 4 (4), pp. 235–238, 2009.
- [6] S. V. Garimella, V. Singhal and D. Liu, "On-chip thermal management with microchannel heat sinks and integrated micropumps," *Proc. IEEE*, 94 (8), pp. 1534–1548, 2006.
- [7] C. Green, A. G. Fedorov and Y. K. Joshi, "Fluid-to-fluid spot-to-spreader (F2/S2) hybrid heat sink for integrated chip-level and hotspot level thermal management," *ASME J. Ele. Packag.*, 131 (2), pp. 025002-1–025002-10, 2009.
- [8] V. Sahu, Y. Joshi and A. Fedorov, "Hybrid solid state/fluidic cooling for hot spot removal," *Nanoscale Microscale Thermophys. Eng.*, 13 (3), pp. 135–150, 2009.
- [9] N. Putra, Yanuar and F. N. Iskandar, "Application of nanofluids to a heat pipe liquid-block and the thermoelectric cooling of electronic equipment," *Experimental Thermal and Fluid Science*, vol. 35, pp. 1274–1281, 2011.
- [10] P. Wang, A. Bar-Cohen, B. Yang, G. L. Solbrekken and A. Shakouri, "Analytical Modeling of Silicon Thermoelectric Microcooler," *J. Appl. Phys.*, 100, p. 014501, 2006.
- [11] V. Litvinovitch and A. B. Cohen, "Effect of Thermal Contact Resistance on Optimum Mini-contact TEC Cooling on On-chip Hot Spots," *Proceedings of InterPACK09*, San Francisco, CA, 2009.
- [12] Y. S. Ju, "Impact of Interface Resistance on Pulsed Thermoelectric cooling," *J. Heat Trans.*, 130, p. 014502, 2008.
- [13] O. Sullivan, M. P. Gupta, S. Mukhhopadhyay and S. Kumar, "Array of Thermoelectric Coolers for On-Chip Thermal Management," *Journal of Electronic Packaging*, 134, pp. 1-8, 2012.
- [14] R. Chein and G. Huang, "Thermoelectric cooler application in electronic cooling," *Applied Thermal Engineering*, vol. 24, p. 2207–2217, 2004.
- [15] *Thermoelectrics Handbook: Macro to Nano*, Edited by D.M. Rowe, CRC Press, Taylor & Francis Group, ISBN 0-8493-2264-2, 2006.
- [16] R. S. Prasher, J. -Y. Chang, I. Sauciu, S. Narasimhan, D. Chau, G. Chrysler, A. Myers, S. Prstic and C. Hu, "Nano and micro technology based next-generation package-level cooling solutions," *Int. Technol. J.*, 9 (4), pp. 285–296, 2005.
- [17] S. V. Garimella, "Advances in Mesoscale Thermal Management Technologies for Microelectronics," *Microelectron. J.*, 37, pp. 1165–1185, 2006.
- [18] L. M. Goncalves, J. G. Rocha, D. Couto, P. Alpuimand J. H. Correia, "On-chip Array of Thermoelectric Peltier Microcoolers," *Sens. Actuators*, A145-146, pp. 75–80, 2008.
- [19] M. P. Gupta, M. S. Sayer, S. Mukhhopadhyay and S. Kumar, "Ultrathin Thermoelectric Devices for On-chip Peltier Cooling," *IEEE Trans. Compon., Packag. Manuf. Technol.*, 1(9), pp. 1395–1405, 2011.
- [20] A. Bar-Cohen and P. Wang, "On-chip hot spot remediation with miniaturized thermoelectric coolers," *Micrograv. Sci, Technol*, 21 (1), pp. 351–359, 2009.
- [21] M. Redmond, K. Manickaraj, O. Sullivan and S. Kumar, "Hotspot Cooling in Stacked Chips Using Thermoelectric Coolers," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, 3 (5), pp. 759-767, 2013.
- [22] G. J. Snyder, M. Soto, R. Alley, D. Koester and B. Conner, "Hot Spot Cooling using Embedded Thermoelectric Coolers," in *Twenty-Second Annual IEEE Semiconductor Thermal Measurement and Management Symposium*, Dallas, TX USA, 2006.
- [23] S. A. Alshehri and H. H. Saber, "Experimental investigation of using thermoelectric cooling for computer chips", *Journal of King Saud University – Engineering Sciences*, <https://doi.org/10.1016/j.jksues.2019.03.009>, 2019 (in press).
- [24] S. A. Alshehri, "Cooling Computer Chips with Cascaded and Non-Cascaded Thermoelectric Devices", *Arabian Journal for Science and Engineering*, <https://doi.org/10.1007/s13369-019-03862-2>, 2019.
- [25] H. H. Saber, S. A. Alshehri and W. Maref, "Performance optimization of cascaded and non-cascaded thermoelectric devices for cooling computer chips", *Journal of Energy Conversion and Management*, <https://www.sciencedirect.com/science/article/pii/S0196890419304406>, 191, p. 174–192, 2019.