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PSRR Enhanced LDO Regulator Using Noise Sensing Circuit

Min-ju Kwon, Chae-won Kim, Jeong-yun Seo, Hee-guk Chae, Yong-seo Koo

***Abstract*—**In this paper, we presented the LDO (low-dropout) regulator which enhanced the PSRR by applying the constant current source generation technique through the BGR (Band Gap Reference) to form the noise sensing circuit. The current source through the BGR has a constant current value even if the applied voltage varies. Then, the noise sensing circuit, which is composed of the current source through the BGR, operated between the error amplifier and the pass transistor gate of the LDO regulator. As a result, the LDO regulator has a PSRR of -68.2 dB at 1k Hz, -45.85 dB at 1 MHz and -45 dB at 10 MHz. the other performance of the proposed LDO was maintained at the same level of the conventional LDO regulator.

***Keywords*—**LDO regulator, noise sensing circuit, current reference, pass transistor.

I. Introduction

With the advanced IC technology, the manufacturers have attention to PMIC (Power Management IC) due to the increase of the supply for the portable devices such as the cell phone, notebook using the lithium battery. Recently, the market customers require the portable devices of low power and high performance. Then, by using the only limited battery, the devices must take the functional action at the stable state for most of the operation time. Therefore, the R&D process about the high stability is necessary for the steady states using the power supply [1]-[11]. Generally, the LDO regulator is used for the stable output voltage. The linear regulator such as LDO regulator has the advantage of the low noise and the output stability. However, due to the some inevitable noise of the voltage source, LDO regulators must have the high PSRR (Power Supply Rejection Ratio).

In this paper, we proposed the LDO regulator with the enhanced PSRR using the constant current source and the noise sensing circuit.

II. The LDO Regulator with the Noise Sensing Circuit

A. LDO Regulator

Fig. 1 shows the structure of conventional LDO regulator. The LDO regulator is composed of the five elements: BGR, Error Amplifier, Pass transistor, Feedback Resistor and Load [12]-[14].

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The BGR provides the constant output voltage to the input of the error amp. The error amp adjusts the gate voltage of the pass transistor with the output through the feedback for the operation as a switch. Then, the pass transistor provides the constant voltage to the load through the low voltage drop from the incoming supply voltage. Consequently, the feedback resistor senses the voltage applied to the load and feeds the error amp according to the voltage magnitude [15], [16].

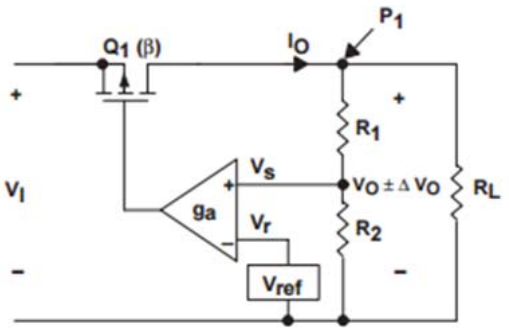


Fig. 1 Structure of conventional LDO regulator

B. Noise Sensing Circuit

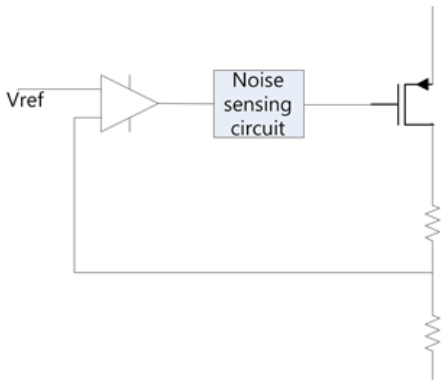


Fig. 2 Proposed LDO regulator block diagram

When the supply voltage fluctuates, the conventional LDO of Fig. 1 has the output voltage fluctuation causing the unstable voltage supply. For the stable power supply, the LDO regulator with the noise sensing circuit is proposed as shown in Fig. 2. The LDO regulator is composed of a reference voltage generator, an error amplifier, a pass transistor, a feedback resistor and a noise sensing circuit. The noise sensing circuit is located between the output of the error amplifier and the gate of the pass transistor. When the supply voltage is changed, the gate voltage of the pass transistor is adjusted by detecting the magnitude of the voltage difference. Then, the gate-source voltage of the pass transistor sustains the constant value and the

LDO regulator provides a stable output voltage [17], [18].

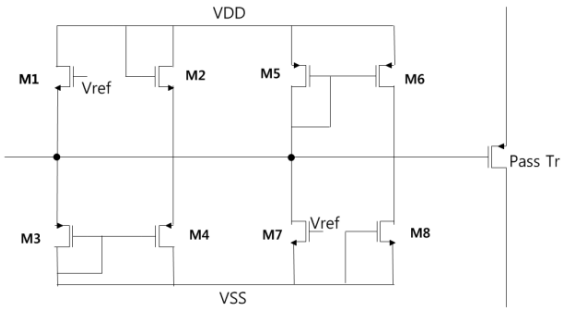


Fig. 3 Schematic of the proposed noise sensing circuit

Fig. 3 shows the circuit diagram of the noise sensing circuit. The circuit consists of 8 transistors. The M1 and M7 transistors receive the input voltage from the BGR and operate as a constant current source under no influence of the temperature and the supply voltage. When noise occurs in the power supply, the M2 and M8 detect the noise and the current values in M2 and M8 are changed. Then, the changed values are mirrored to the diodes connected to the M4 and M6 transistors and are compared to the reference currents of the M1 and M7 through the M3 and M5 transistors. Through a comparison process, the gate voltage of the pass transistor is changed back to the initial value. The method can rapidly adjust the gate voltage by sensing the noise.

III. Simulation Results

A. Basic Properties

The LDO regulator was simulated by the Cadence Schematic Tool. The simulation is conducted with the CMOS process. As shown in Fig. 4, the proposed LDO regulator has the same properties of the conventional LDO regulator such as the phase margin, the load transient and the load regulation.

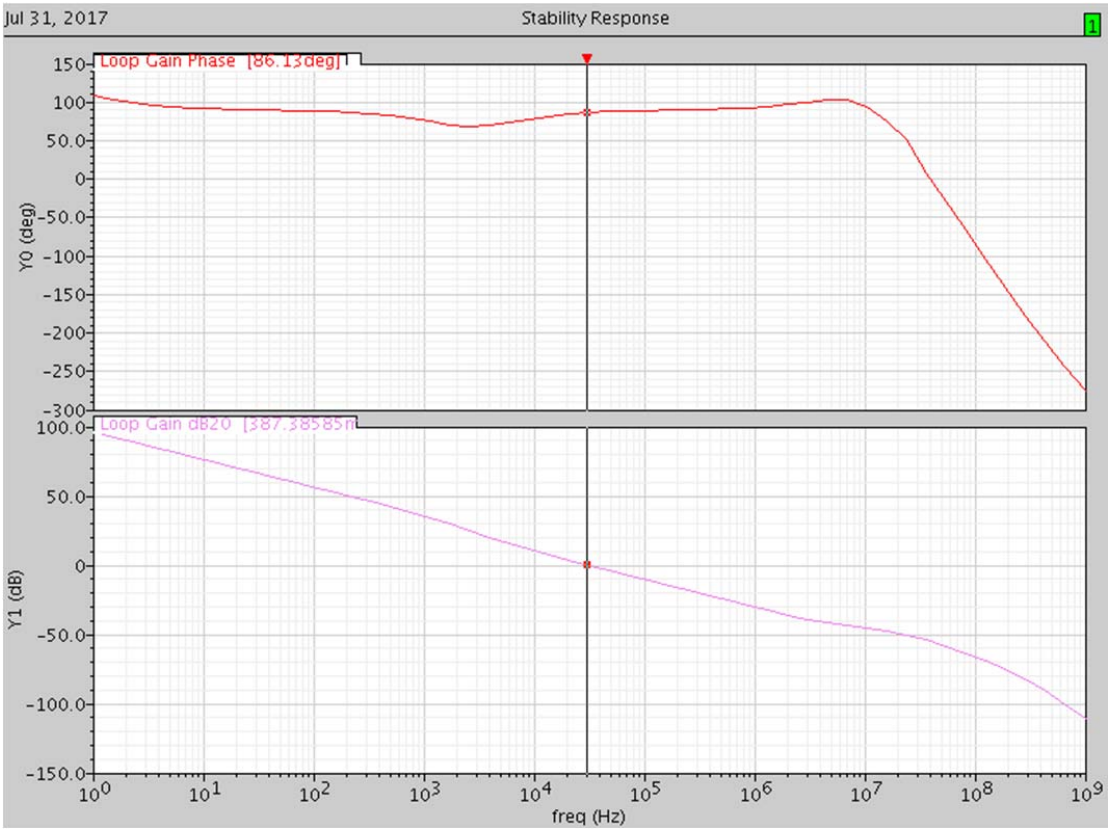
B. PSRR Property

Fig. 5 shows the PSRR simulation results of the proposed LDO regulator and the conventional LDO regulator. The proposed LDO regulator has the PSRR of -74.6 dB at 3.3 supply voltage, which is higher than that of the conventional LDO by -15.1 dB.

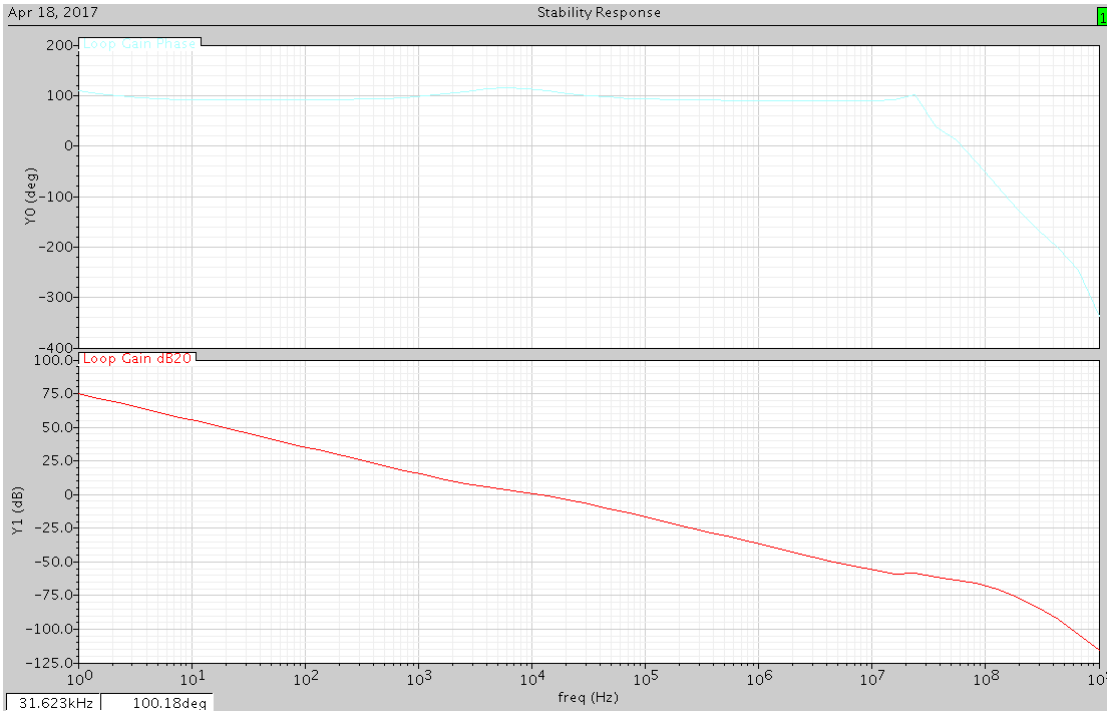
TABLE I
PSRR at the Operational Primary Frequency

Frequency	Conventional LDO	Proposed LDO
1 Kilo Hz	-59.16 dB	-68.20 dB
1 Mega Hz	-41.03 dB	-45.85 dB
10 Mega Hz	-36.41 dB	-45.00 dB

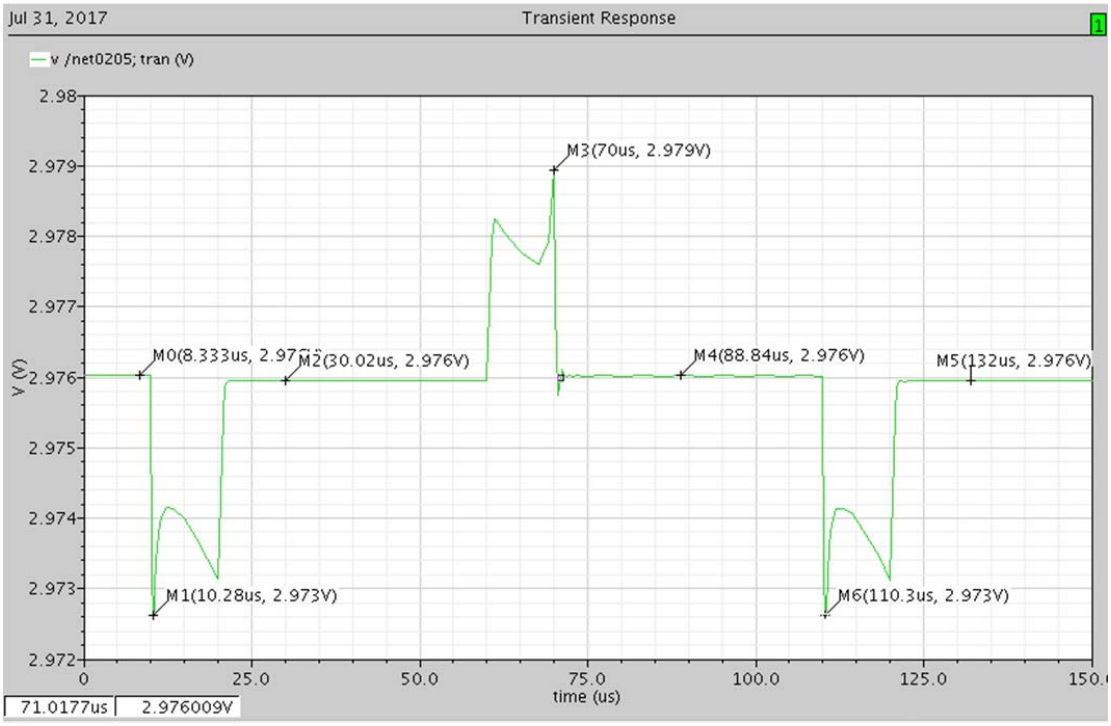
As the simulation results in various primary frequencies, the proposed LDO regulator has the PSRR of -68.2 dB at 1 kilo Hz, -45.85 dB at 1 MHz, and -45 dB at 10 MHz. The values are higher than that of the conventional LDO regulator of -59.16 dB at 1 kHz, -41.03 dB at 1 MHz, and -36.41 dB at 10 MHz.



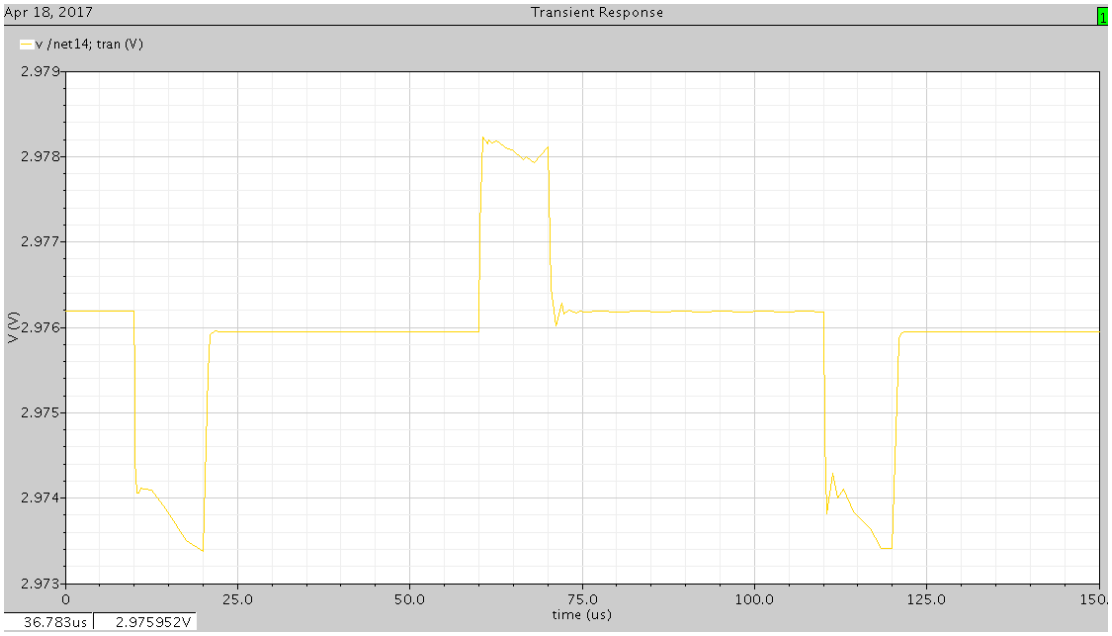
(a)



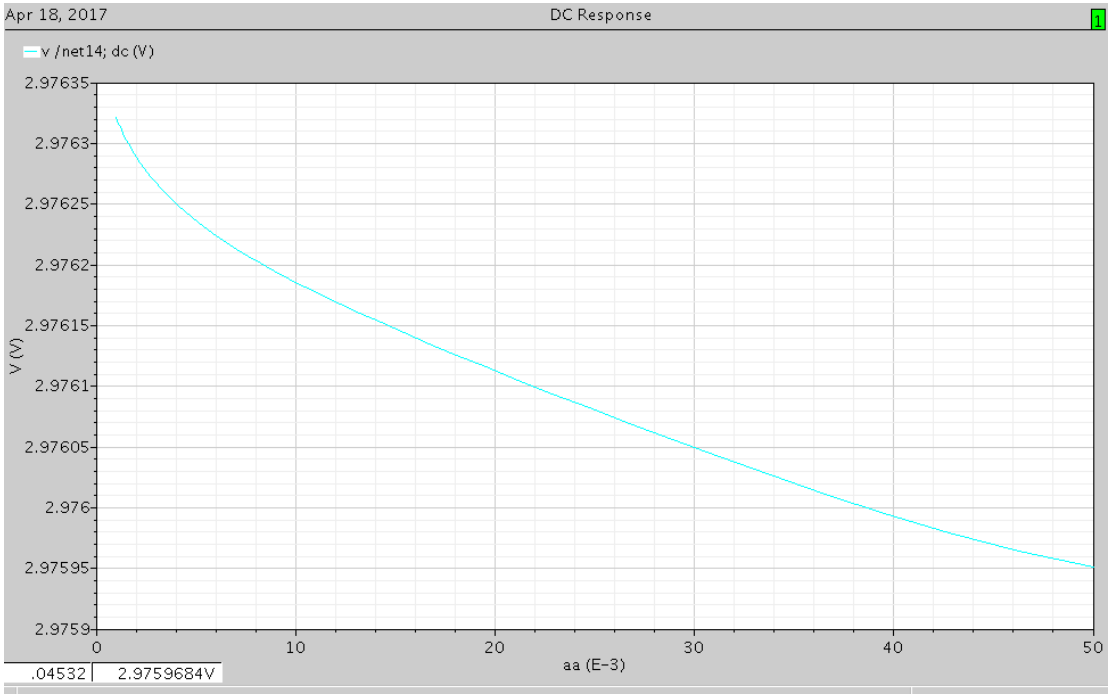
(b)



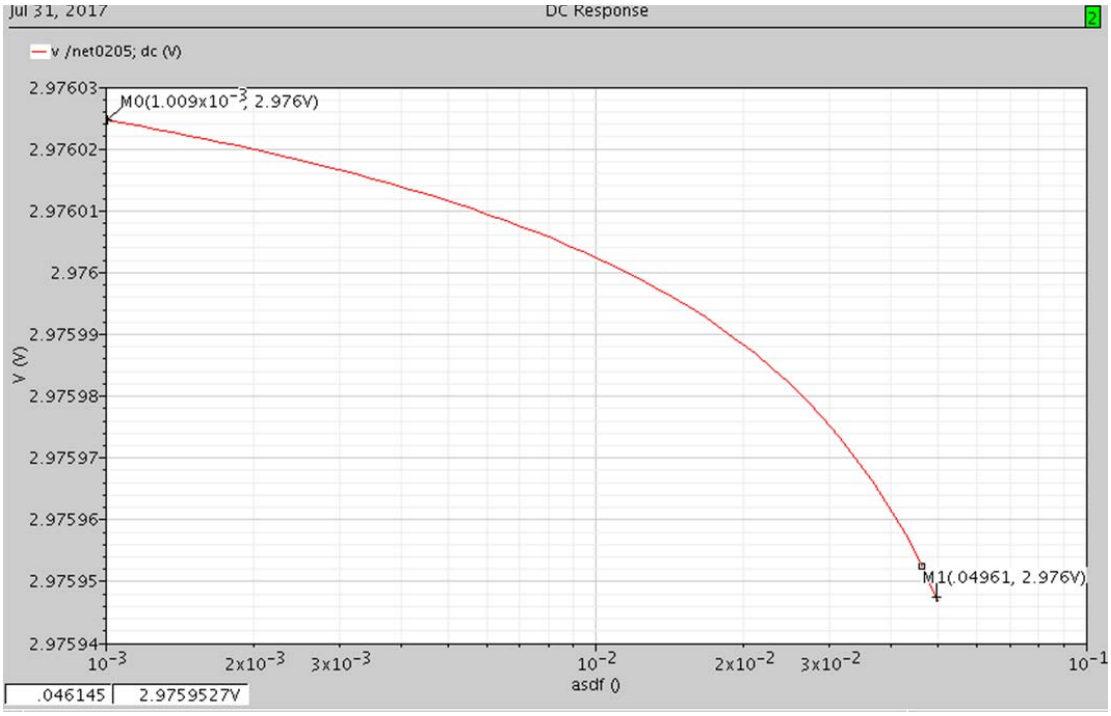
(c)



(d)

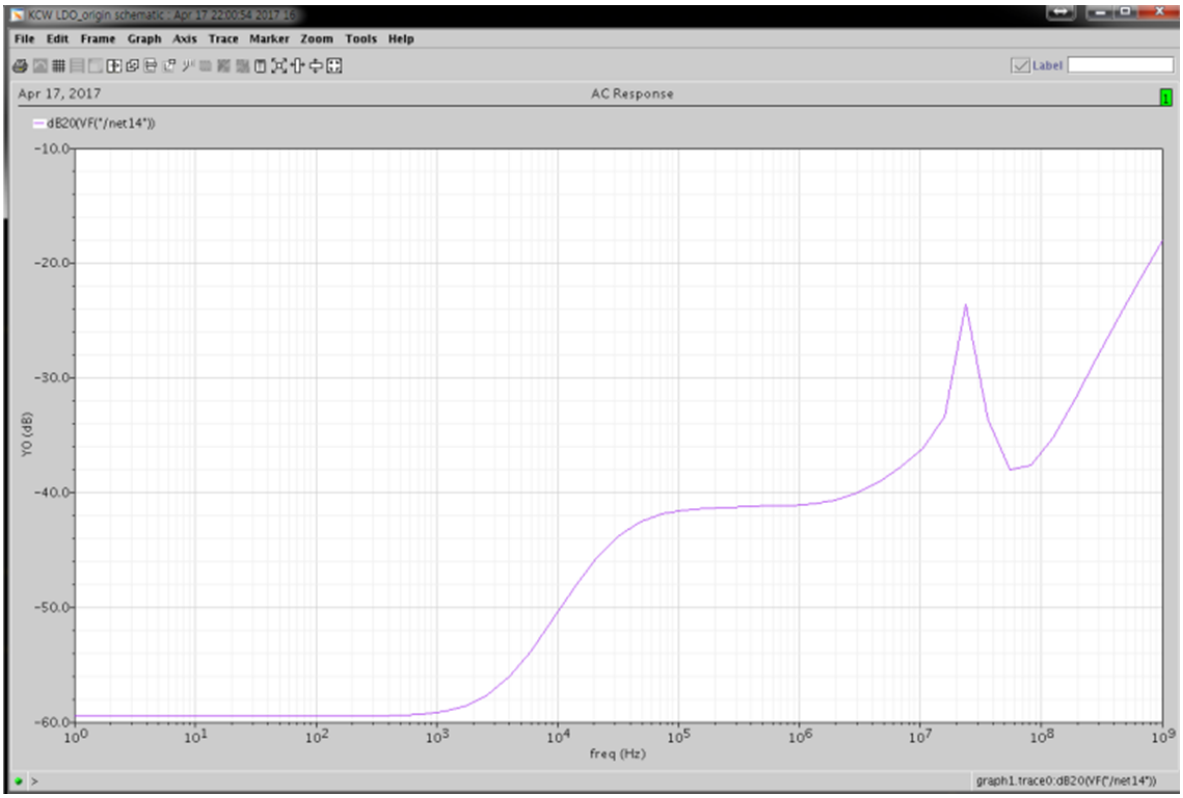


(e)

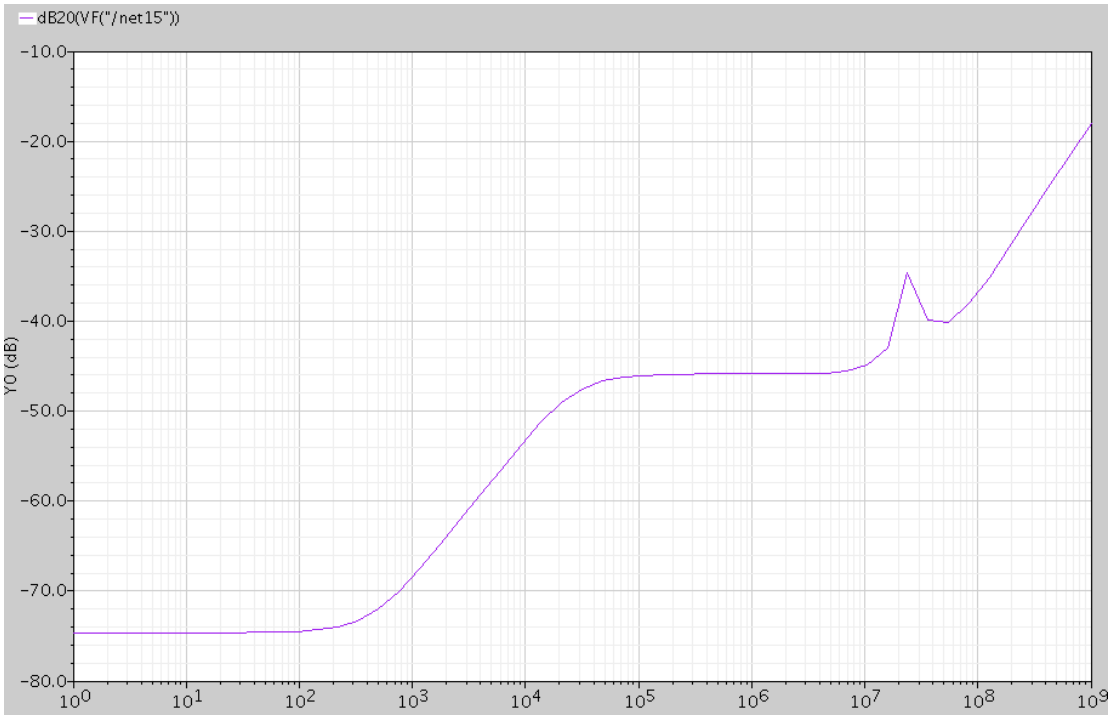


(f)

Fig. 4 Basic properties: Phase margin, load transient, load regulation of (a), (c), (e) proposed LDO and (b), (d), (f) conventional LDO



(a)



(b)

Fig. 5 (a) PSRR of the conventional LDO (b) PSRR of the proposed LDO

IV. Conclusion

In this paper, the LDO regulator with the noise sensing circuit is proposed. The noise sensing circuit can effectively control the gate biasing of the pass transistor by sensing the induced current value from the supply voltage fluctuation. The simulation is conducted with the CMOS process. As a result, the PSRR is changed from -15.1 dB to -74.6 dB, and the other properties are maintained at the same level. Therefore, the proposed circuit can supply the stable output voltage with the enhanced PSRR. In addition, the enhanced PSRR is sustained in the high frequency band.

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References

[1] Al-Shyoukh, M.; Hoi Lee; Perez, R, “A Transient-Enhanced Low-Quiescent Current Low-Dropout Regulator with Buffer Impedance Attenuation,” Solid-State Circuits, IEEE Journal of, vol. 42, pp. 1732–1742, Aug. 2007.

[2] Pui Ying Or and Ka Nang Leung, “An Output-Capacitorless Low-Dropout Regulator With Direct Voltage-Spike Detection”, IEEE J. Solid-State Circuits , vol. 45, no. 2, pp. 458-466, Feb. 2010.

[3] X. Ming, Q. Li, Z. Zhou and B. Zhang, “An ultrafast adaptively biased capacitorless LDO with dynamic charging control,” IEEE Tran. Circuits, Syst. II, vol. 59, no. 1, pp. 40-44, Jan. 2012.

[4] Leo, C.J., M.K. Raja, and J. Minkyu, "An ultra low-power capacitor-less LDO with high PSR," Microwave Workshop Series on RF and Wireless Technologies for Biomedical and Healthcare Applications (IMWS-BIO), 2013 IEEE MTT-S International, 2013.

[5] Chang-Joon Park, “External Capacitor-less low drop-out regulator with 25 dB superior power supply rejection in the 0.4-4MHz range,” IEEE J. Solid-State Circuits, vol. 49, no. 2, pp. 486-501, Feb. 2014.

[6] Zishen, L., H. Lenian, and C. Chen, "A novel low-dropout regulator with large load current and high stability," Advanced Research and Technology in Industry Applications (WARTIA), 2014 IEEE Workshop, 2014.

[7] Saurabh Kumar Singh and Gautam Dey Kanungo, "Ultra-fast Cap-less LDO for Dual Lane USB in 28FDSOI," VLSI Design (VLSID), 2015 28th International Conference, 2015

[8] Kim, D. and M. Seok. "8.2 Fully integrated low-drop-out regulator based on event-driven PI control," 2016 IEEE International Solid-State Circuits Conference (ISSCC), 2016.

[9] Vaisband, I. and E.G. Friedman, "Stability of Distributed Power Delivery Systems With Multiple Parallel On-Chip LDO Regulators," IEEE Transactions on Power Electronics, Vol. 31, Issue:8, pp. 5625-5634, Aug. 2016

[10] Zarate-Roldan, J., et al., "A Capacitor-Less LDO With High-Frequency PSR Suitable for a Wide Range of On-Chip Capacitive Loads," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol.24, Issue:9, pp. 2970-2982, Sept. 2016

[11] Mohamed M. Elkhatib, "A capacitor-less LDO with improved transient response using neuromorphic spiking technique," Microelectronics (ICM), 2016 28th International Conference, 2016

[12] Jungeui Park; Wooju Jeong; Junsang Lee; Seok Lee; Jayang Yoon; Jaehoon Kim; Joongho Choi, “Design of LDO linear regulator with ultra low-output impedance buffer,” SoC Design Conference (ISOCC), 2009 International, pp. 420–423, Nov. 2009.

[13] Yongsheng Wang; Mingyan Yu; Xiaoxiong Feng; Fengchang Lai, “Frequency compensation scheme for LDO regulator operated under wide power supply range in smart battery system,” Electron Devices and Solid-State Circuits (EDSSC), 2011 International Conference of, pp. 1-2, Nov. 2011.

[14] Yong-Seo Koo; Kang-Yoon-Lee; Jae-Hwan Ha; Yil-Suk Yang. "A Design of Power Management IC for CCD Image Sensor" IKEEE, vol 13, no.4, pp. 63-68, 2009.

[15] Seong-Mok Yu; Joon-Ho Park; Jong-Tae Park; Chong-Gun Yu, "Design of Tripple-Mode DC-DC Buck Converter" IKEEE, vol 15, no.2, pp. 134-142, 2011.
[16] Xuguang Zhang; El-Masry, E.I., "A regulated body-driven CMOS current mirror for low-voltage applications," Circuits and Systems II: Express Briefs, IEEE Transactions on, vol. 51, pp. 571-577, Oct. 2004.
[17] Rui He; Lihong Zhang, "Evaluation of modern MOSFET models for bulk-driven applications," Circuits and Systems, 2008. MWSCAS 2008. 51st Midwest Symposium on, pp. 105-108, Aug. 2008.
[18] Khateb, F.; Biolek, D.; Khatib, N.; Vavra, J., "Utilizing the Bulk-driven technique in analog circuit design," Design and Diagnostics of Electronic Circuits and Systems (DDECS), 2010 IEEE 13th International Symposium on, pp. 16-19, Apr. 2010.