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Improving the Voltage Level in High Voltage Direct Current Systems by Using Modular Multilevel Converter

G. Kishor Babu, B. Madhu Kiran

Abstract**—**This paper presented an intend scheme of Modular-Multilevel-Converter (MMC) levels for move towering the practical conciliation flanked by the precision and divisional competence. The whole process is standard by a Thevenin-equivalent 133-level MMC model. Firstly the computation scheme of the fundamental limit imitation time step is offered to faithfully represent each voltage level of waveforms. Secondly the earlier industrial Improved Analytic Hierarchy Process (IAHP) is adopted to integrate the relative errors of all the input electrical factors interested in one complete virtual fault on each converter level. Thirdly the stable AC and DC ephemeral condition in virtual faults effects of all the forms stabilize and curve integral stand on the standard form. Finally the optimal MMC level will be obtained by the drown curves and it will give individual weights allowing for the precision and efficiency. And the competence and potency of the scheme are validated by model on MATLAB Simulink.

Keywords**—**Modular multilevel converter, improved analytic hierarchy process, ac and dc transient, high voltage direct current, voltage sourced converter.

I. Introduction

MMC converter based high voltage direct current (HVDC) transmission system is being widely used and has shown significant engineering prospects in the voltage source converter (VSC) fields [1], [4]. However, the large number of switching components in MMC makes detailed simulation on an Electromagnetic Transient (EMT) simulation program extremely slow [5], [6], and the interpolation function to precisely trigger the semiconductor devices will also increase the computational burden of the model [7], [8]. Recently, novel MMC models are proposed and they reduce the complexity [16].

The capability of admittance to the MMC's inner performances are left and the cell capability must be examined and the limitations must be cautiously intended to the strict AC and DC side errors such as the DC side ensuing storage element size of the automated valuation models [10]. Therefore the consumers could require a practical conciliation among the precision and competence of the MMC cells for EMT studies [15].

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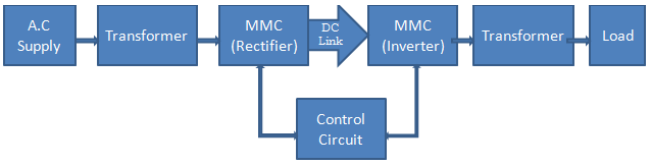


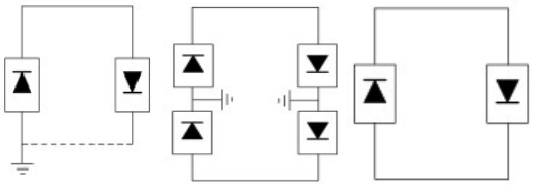
Fig. 1 Block diagram of HVDC system with MMC

Consequently, an additional vital topic must be dealt with the time step after creating MMC with an extra number of power levels. It is a MMC of level 133 created by ac MMC of level 11 and explains the performance of both the levels [7]. The 133-level MMC cannot explain the complete changing information and so cannot be observed as the target cell. The proposed solution in this paper has high computation efficiency almost close to the simplified averaged-value models, and the proposed optimal Thévenin equivalent MMC model can be a very good candidate for the design and simulation purposes in real HVDC papers. These unique features such as independent control of active and reactive power [2], operation in weak ac systems [3] have led to their increased adoption in modern schemes. Reduction of harmonics in the system is achieved with the PWM technique till now with the two/three level VSC topologies in the application of HVDC transmission. The power ratings are restricted up to 600 MW as losses towards switching are more for the ratings above 600 MW. Numerous multi-level topologies and inflection strategies have been introduced for machine force appliances [6], [8]. Diode clamped multilevel converters [7] produce a stepped AC waveform like a sine wave by mounding set scale voltage paces on crest of a piece further. The above mentioned topology has smaller losses than two-level pulse width modulation converter. Moreover it is restricted up to three levels due to the system complexity for the HVDC applications and balancing capacitor across voltage is a critical and challenging issue. MMC is most important tread advance in VSC equipment for HVDC [9], [11]. The ratings more than 1 GW are feasible with the MMC topology [10], and the exchange taking place in power schemes is small. It disputes power looms and studies their performance using EMT imitation and also investigates the run and piece of a HVDC.

II. Construction of HVDC Transmission

Depending on practical characteristics major HVDC constructions shown in Fig. 2 are used.

- Mono polar construction (a) - connects two converter stations via a single line with the prospect to control at both DC polarities. Marine performer can be used for come back path.
- Bipolar configuration (b) - connects both switching operating at reverse polarities. This results in two free DC charged at half power every one. For the duration of one pole, a mono polar function can be used [13].



(a) (b) (c)

Fig. 2 HVDC system constructions: (a) Mono polar, (b) Bipolar, (c) Back-to-back

- Back-to-Back construction (c) - the DC sides of two converters are unswervingly connected having no DC transmission line. This preparation is used for the interconnection of asynchronous AC systems.

While conventional CSC-HVDC transmission is well recognized for high power and voltage ratings (typically up to several GW and ±800 kV), it is expected that from now on the VSCs will be foremost in the potential high power HVDC interconnections due to several advantages in financial and technical description. The main advantages of VSC-HVDC over CSC-HVDC are plotted below

- Observing four quadrant operation and voltage & current in paths (Fig. 3). The removals of reactive power return effect the step drop.
- Prospect of relationship to the feeble and submissive networks. For the A.C networks, short circuit aptitude for grounding is necessity prospect of protected error ride through and ability.
- Prospect of protected error ride through and ability.
- Fast-active-power-reversal.
- Fast operating and control.

The emblematic construction of present HVDC with VSC system is shown in Fig. 4. Both DC performers of converse division connect two switching control. The direction of the power transform should be changed whenever the DC current is reversed to get the DC link voltage residue.

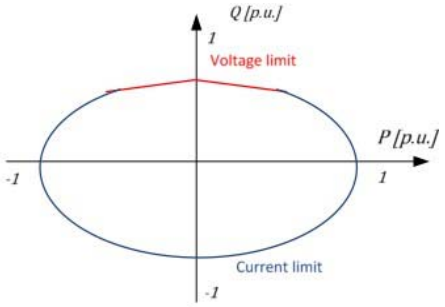


Fig. 3 Diagram of VSC with HVDC

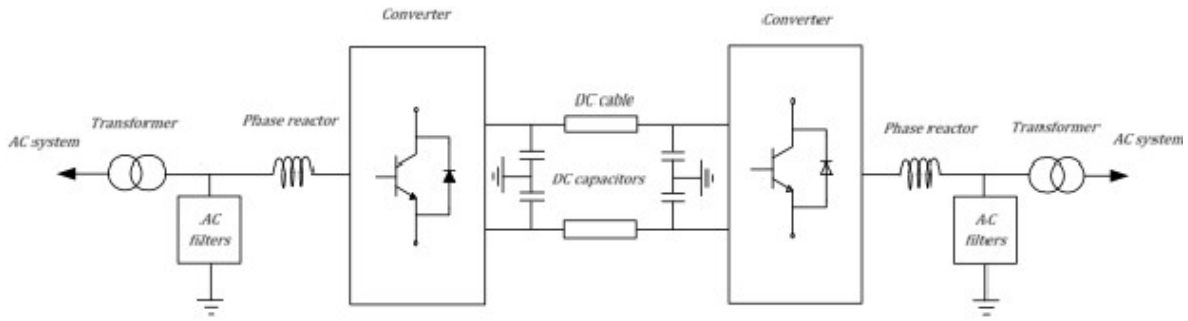


Fig. 4 VSC with HVDC system configuration

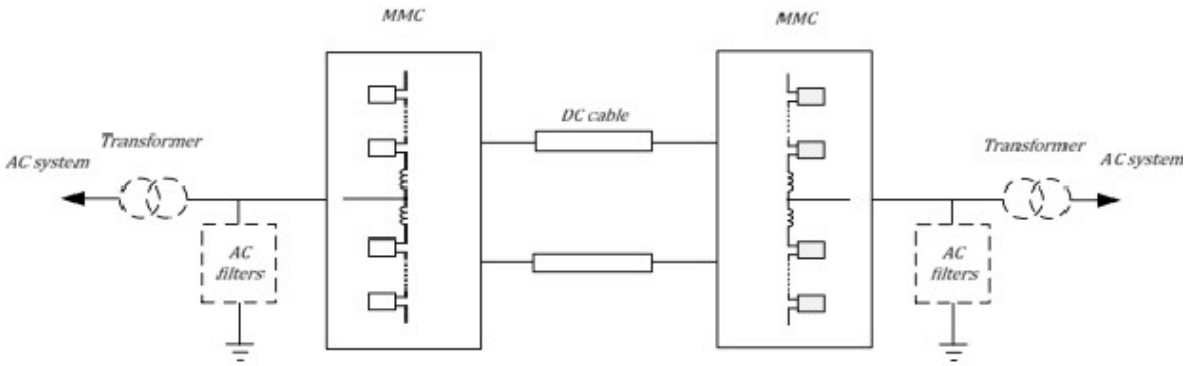


Fig. 5 MMC with HVDC system configuration

The DC voltage is filtered with help of capacitors placed on DC side. The phase reactors control the swap of power between the converter and AC system and also control the fault currents. The AC filters decrease harmonics pleased on the AC bus voltage. Power transformers are used to adjust converter and AC system voltages and also take part in power regulation.

III. MMC

The MMC topology is based on a series connection of equal elements called sub-modules or cells. Each sub module symbolizes the fundamental component of the MMC shown in Fig. 6. Given that the segment capacitors distribute a regular DC link electrical energy around is not require of large DC link capacitors as in crate of two-level NPC [12], [14]. Inductors are placed in the arms to boundary transient currents.

Different cell topologies can be pertinent to the MMC depending on the function. The difference in the system arrangement affects the practical voltage level of the sub module. The time sub module delivers to a half bridge produced by both converter switches with anti-parallel diodes and a DC capacitor as shown in Fig. 8. The capacitor works as voltage barrier and phase-A. The controls carry out the supplement of the sub-module into the limb circuit while the anti-parallel diodes guarantee uninterruptable current flow.

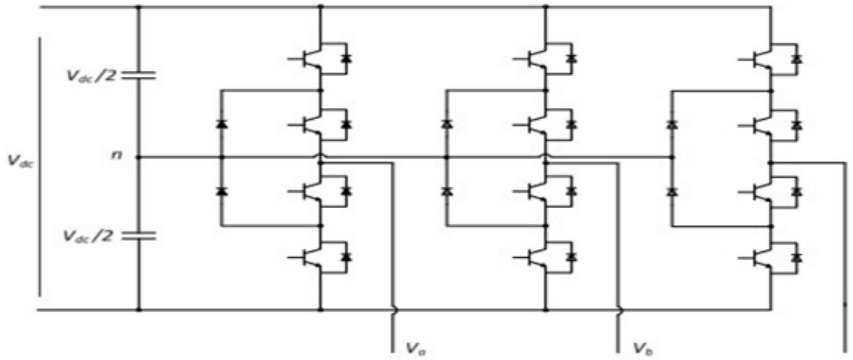


Fig. 6 Topology of three levels NPC converter

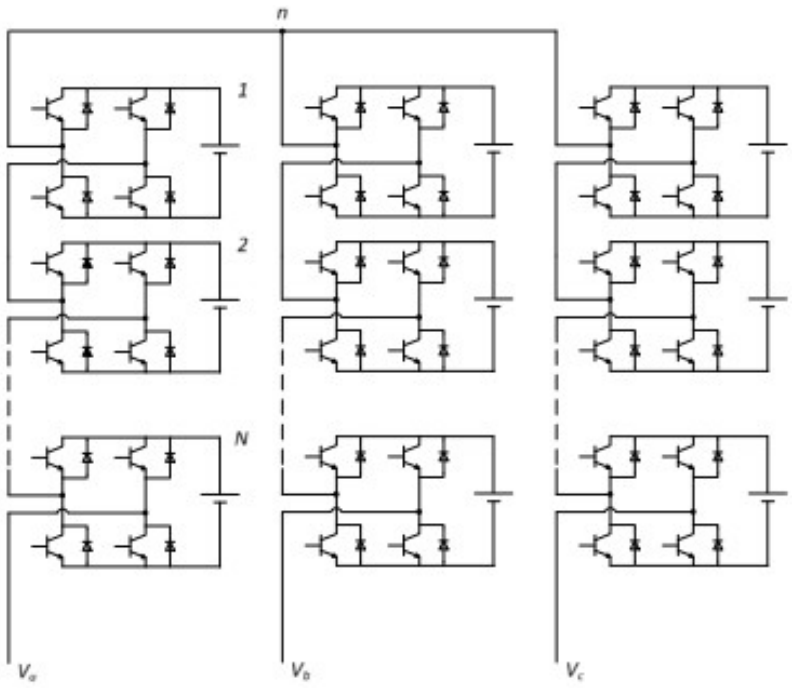


Fig. 7 Topology of cascaded H-bridge inverter

By cascading bridge, the level of harmonics will reduce with the MMC method. All sub modules have both statuses depending on the control locations. In topology S1 is on and s is off, so the terminal voltage is the same as the capacitor across voltage in Fig. 7.

When the lower switch is ON and the upper is OFF the sub-module is bypassed and the terminal voltage is zero. As it can be received from the cell topology the switches have to function in corresponding approach in order open the capacitor.

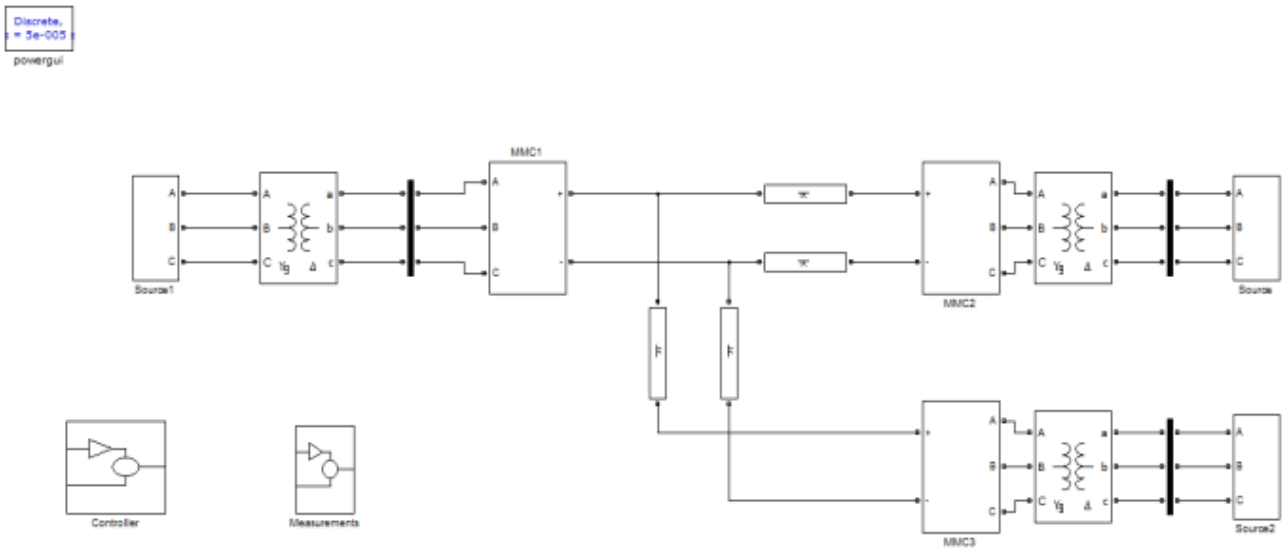


Fig. 9 Simulation diagram of single terminal MMC

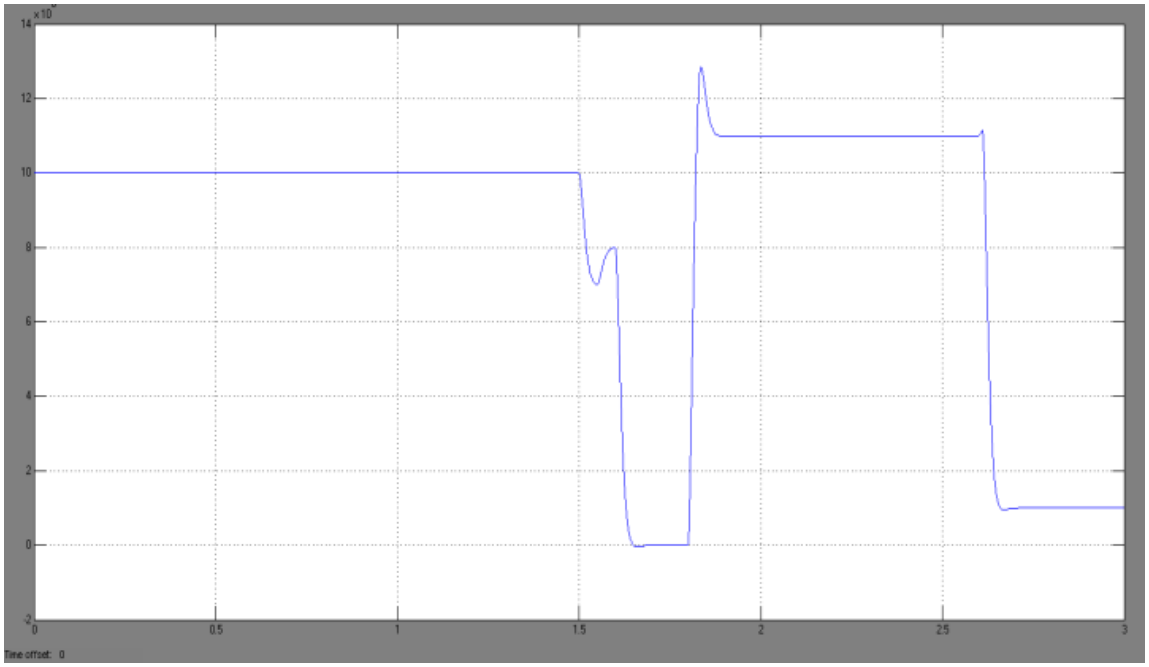


Fig. 10 Waveform of active power

TABLE I
PARAMETERS OF THE MMC SYSTEM

A.C-system	
A.C-voltage U-bus (L-L-rms)	= 230kV
Real-power	*P* = 1000MW
Transformer-capacity	*S*TN = 1060MVA
Winding type Y/Δ turn ratio	*k* = 230 kV/333.14 kV
Leakage-reactance	LT= 0.15p.u.
MMC	
Arm-reactance	*L*0 = 0.085H
Capacitance	C = 11250μF
Sub module number	N = 450
Level-reduction-principle	C/N = 25μF
DC system	
DC voltage	U-dc = 320kV

The course of the limb current influences the capacitor voltage summary. When the cell is inserted, the positive current will charge the capacitor passing through the upper diode. The main benefits of the MMC can be concise as follows:

- Modularity
- Increased output quality
- Reliability
- Increased competence
- Reduced footstep

A. Half Bridge Sub Module

The half bridge sub module includes two IGBT/diode switches and capacitor C as shown in Fig. 8. The power loss

of the half bridge sub-module capacitor is characterized by the resistor. In regular function precisely one of S1 and S2 is active at an instant time. The charge of Vc is taken as a constant and the output voltage for each half-bridge model can be taken as one of two different levels i.e., Vc or zero. With S1 in the 'ON' state, voltage V_{hb} is equal to V_c, and when S2 is 'ON', Vhb is zero. Therefore, it is probable to selectively and independently control each of the being half-bridge cells in the converter to supply a voltage which is either Vc or zero.

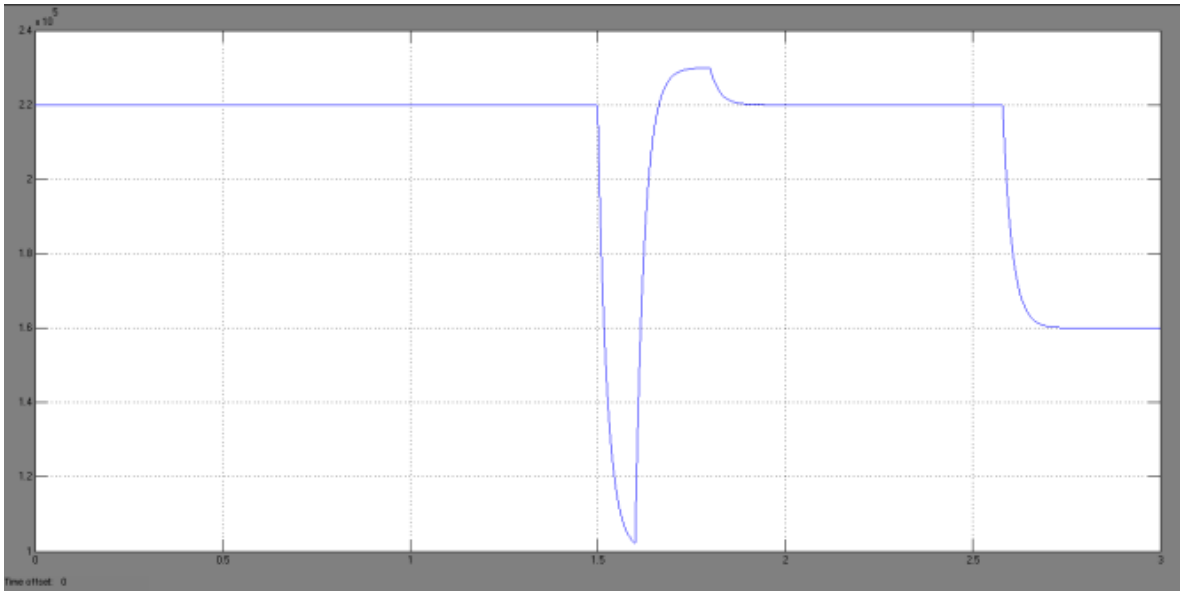


Fig. 11 Waveform of the ac phase voltage

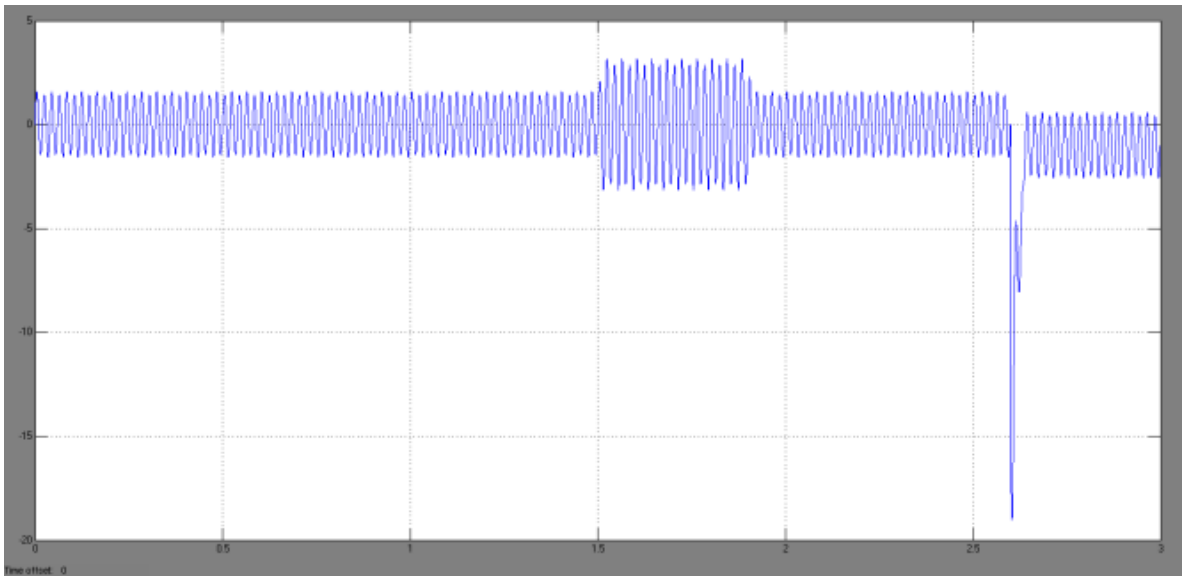


Fig. 12 Waveform of top limb current in phase-A

B. Modulation Techniques of MMC

Multilevel modulation schemes can be split into two categories: space-vector-modulation and voltage-level-based-modulation i.e. Carrier PWM and nearest-level-modulation.

IV. Analysis of Simulation Results

In order to authorize the precision of the optimal MMC model in full setting, the inclusive optimal 25-level MMC model with $w = 1$ is simulated and compared with the standard 133-level MMC model. The reproductions embrace three states: first single-terminal MMC test; second three-terminal MMC-HVDC test with hereditary parameters; third single terminal MMC test with new parameters. All of the tests are following the time logics below:

1) The MMC with HVDC attains stable at t = 1.2 s.
2) A 100 ms LLLG short circuit fault arises at time t = 1.5s.

3) The AC switches turn off disturbance line at time t = 1.58 s, that is allowing for 80 ms exposure and angle.
4) The AC switches turn on productively at time t = 1.8 s as the provisional AC short circuit fault is left at time t = 1.6 s.
5) The MMC with HVDC get well to typical action at time t = 2.4 s.
6) A stable DC extremity disturbance take places at time t = 2.6 s. Switches are uncreative at time t = 2.603 s, that is allowing for 3 ms delay.

B. Single Terminal MMC Test System

The simulated model of the active power and MMC internal upper and lower arm currents are respectively shown in Figs. 9-12. It can be observed that the relative faults connecting 133 level MMC and the standard 133 level are acceptably diminutive to development of investigate the full state. Therefore if uses the Thévenin equivalent model the 133-level MMC should be the optimal MMC model in full states to alternative the 133-level MMC if the magnitude of the model precision and efficiency is set to be the same.

C. Three Terminal MMC-HVDC Systems

In the three terminals MMC with HVDC can be utilized as observed in Fig. 13. MMC controls the DC link voltage and the reactive power. In model, the active power and upper arm currents of MMC are correspondingly exposed in Figs. 14 and 15. From the below virtual effects, it shows that the maximum faults do not adjust a lot and a practical and suitable transmission systems also turn off single terminal MMC trial with new values. It demonstrates that the recommend scheme can be comprehensive from single terminal test to multi-terminal MMC models.

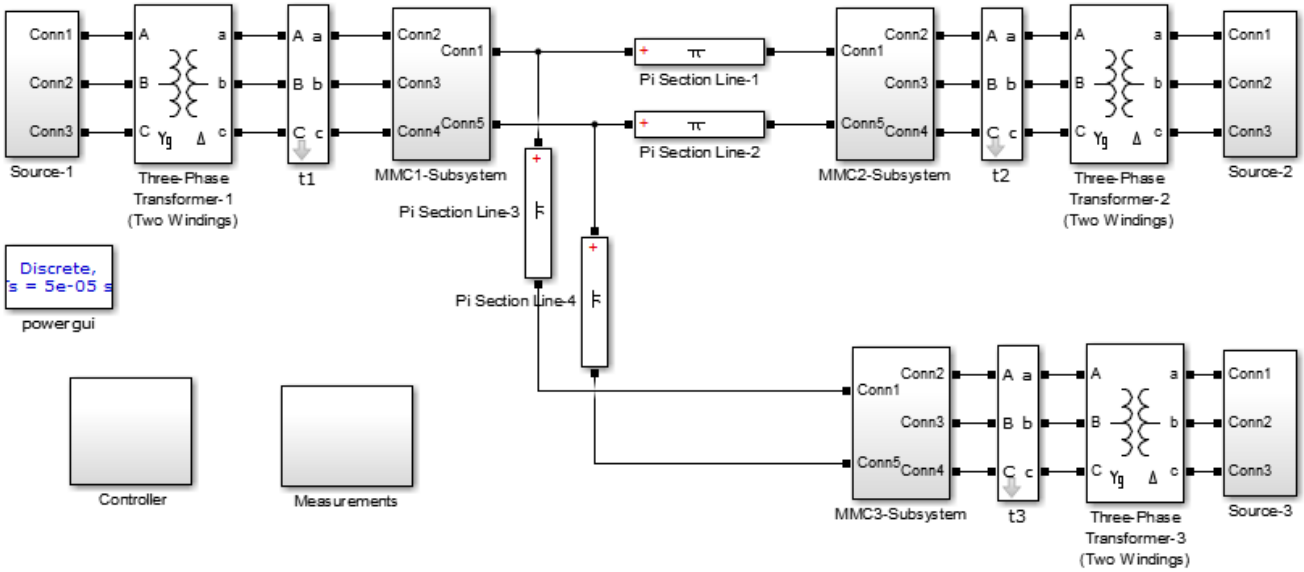


Fig. 13 Simulation diagram of three terminals MMC

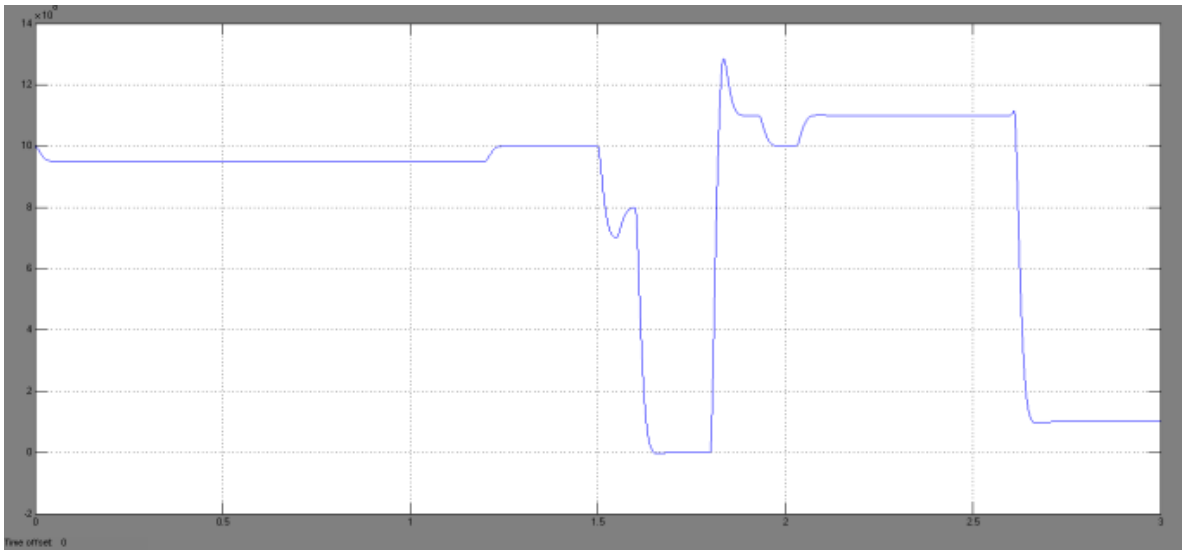


Fig. 14 Waveform of active power

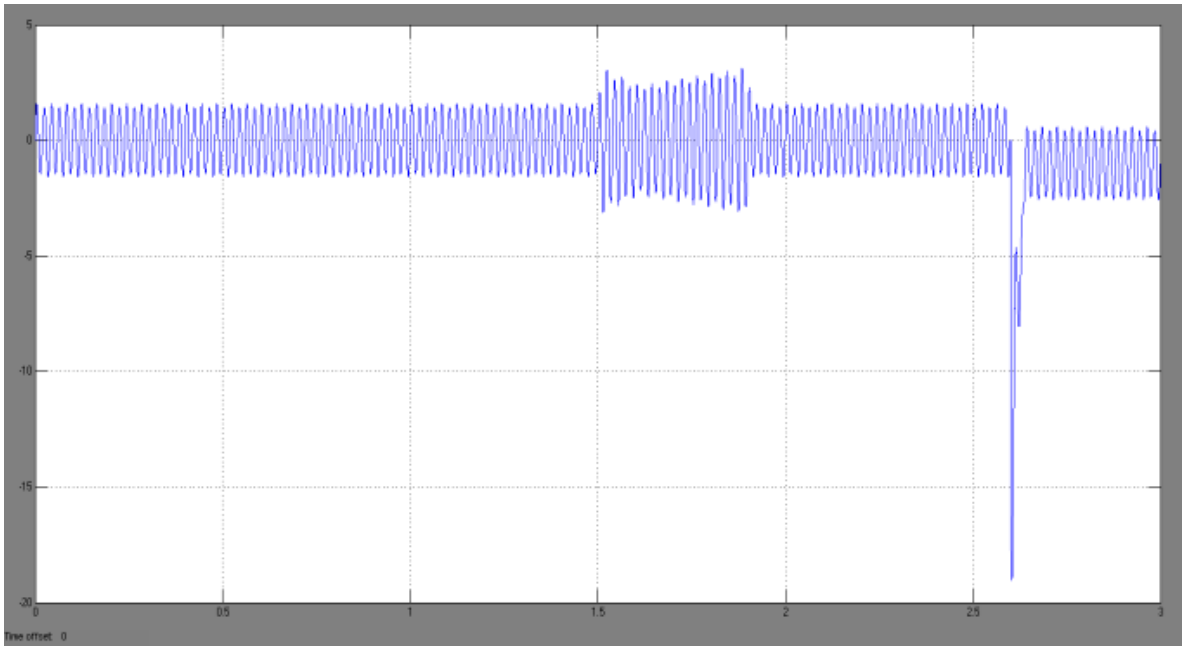


Fig. 15 Waveform of top limb current in phase-A

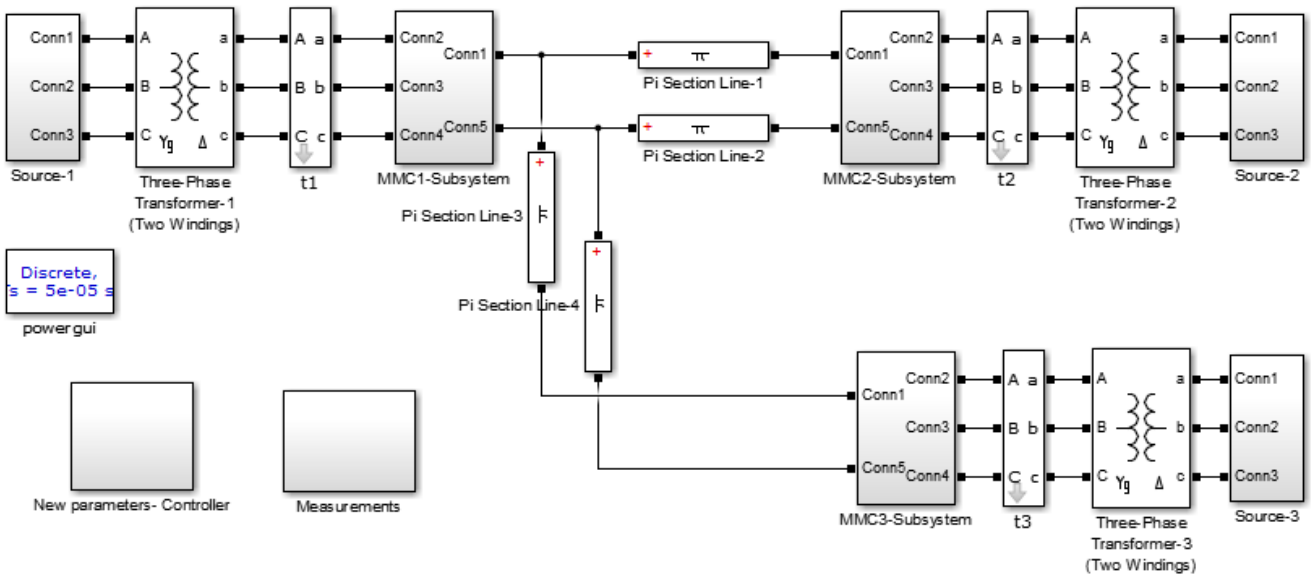


Fig. 16 Simulation diagram of single terminal MMC system with new parameter

TABLE II
PARAMETERS OF THE MMC SYSTEM

A.C-system	
A.C-voltage U-bus (L-L-rms)	= 230kV
Real-power	P = 1600MW
Transformer-capacity	STN = 1800MVA
Winding type Y/Δ turn ratio	k = 230 kV/341.3 kV
Leakage-reactance	LT= 0.15p.u.
Arm-reactance	$L0$ = 0.096H
Capacitance	C = 30μF
D.C system	
D.C voltage	U-dc = 320kV

D.Single Terminal MMC-HVDC Systems with New Parameter

MMC inside factor is top limb phase current correspondingly exposed in Fig. 16. From Figs. 17 and 18, it can be observed that the virtual errors between 133-level MMC and the standard 133-level are acceptably diminutive to development of investigate the full state.

V. CONCLUSION

The proposed scheme comprises the primary division of the vital model time step for MMC and the complete propose scheme of finest MMC levels for EMT reading. The anticipated period choice scheme can authentically illustrate

the entire N + 1 MMC potential intensity with modulation ratio k = 1 and the time step cannot be numerous peak to outwit fall voltage; it is the initial involvement of scheme. Observed finest MMC levels are designed by arc normalized from the purpose virtual faults of stable, AC and DC transient confiscations with the individual user given consequence loads.

The Thevenin equivalent MMC cell used in the future elucidation will fulfill both the HVDC system and control design.

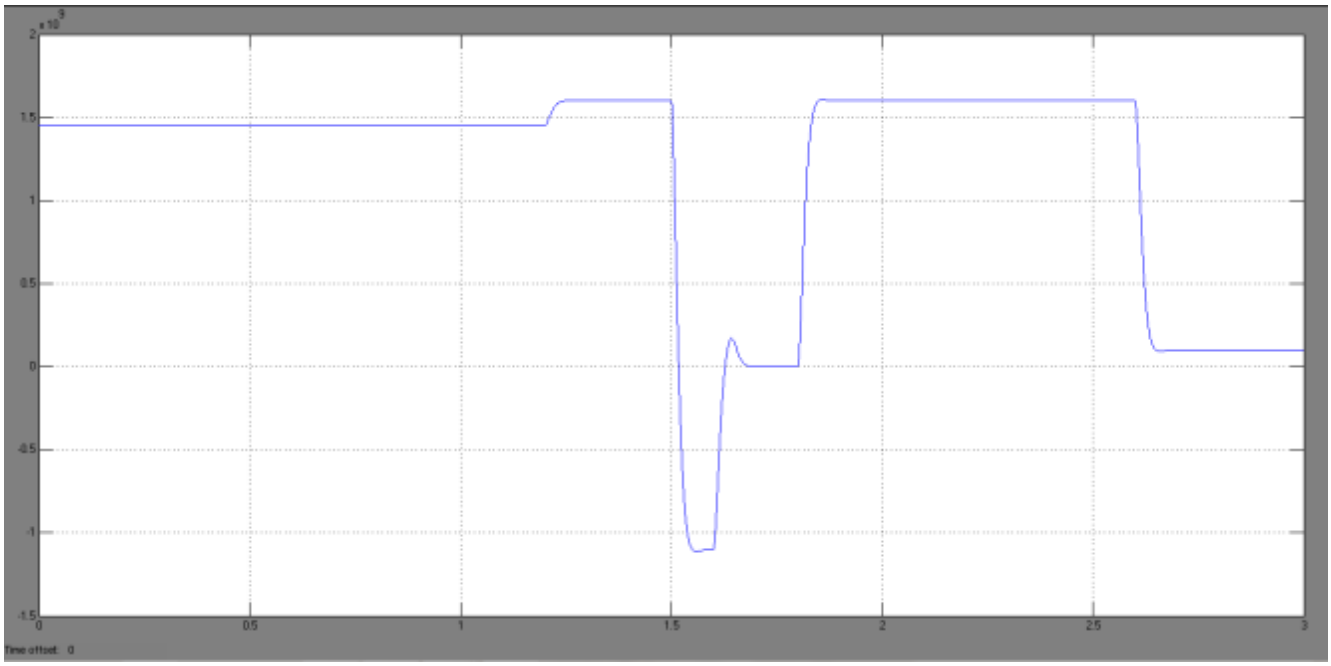


Fig. 17 Waveform of active power

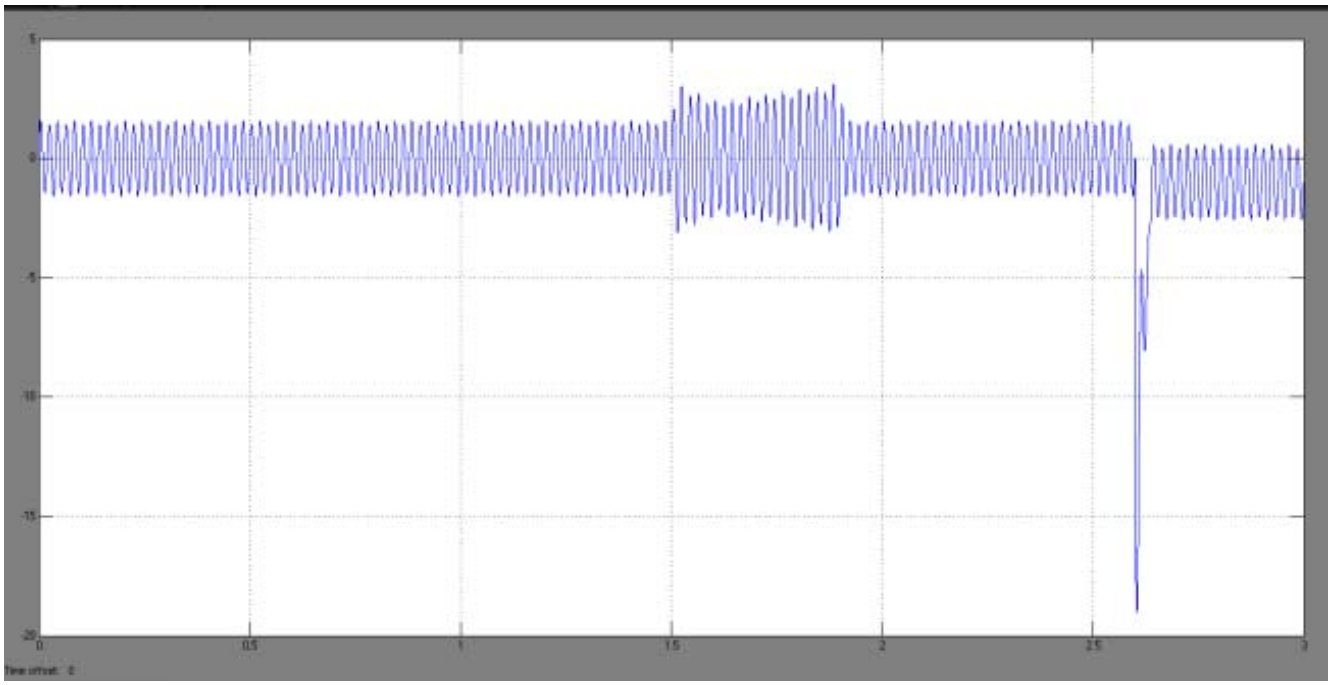


Fig. 18 Waveform of top limb current in phase-A

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